VMM3 Early Testing

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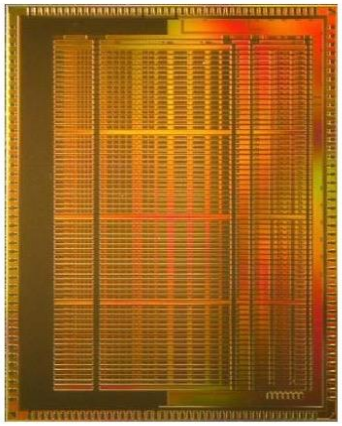
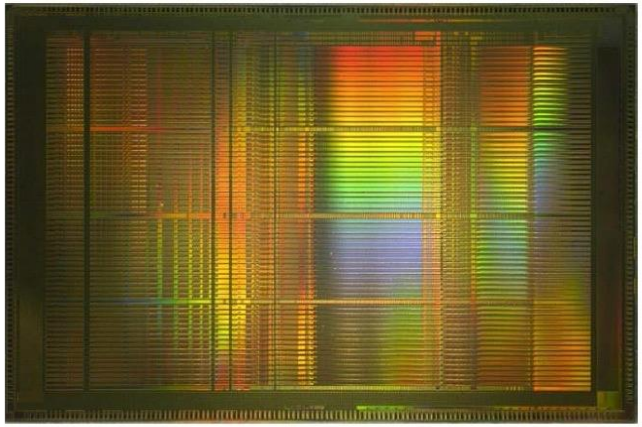
Path Towards VMM3



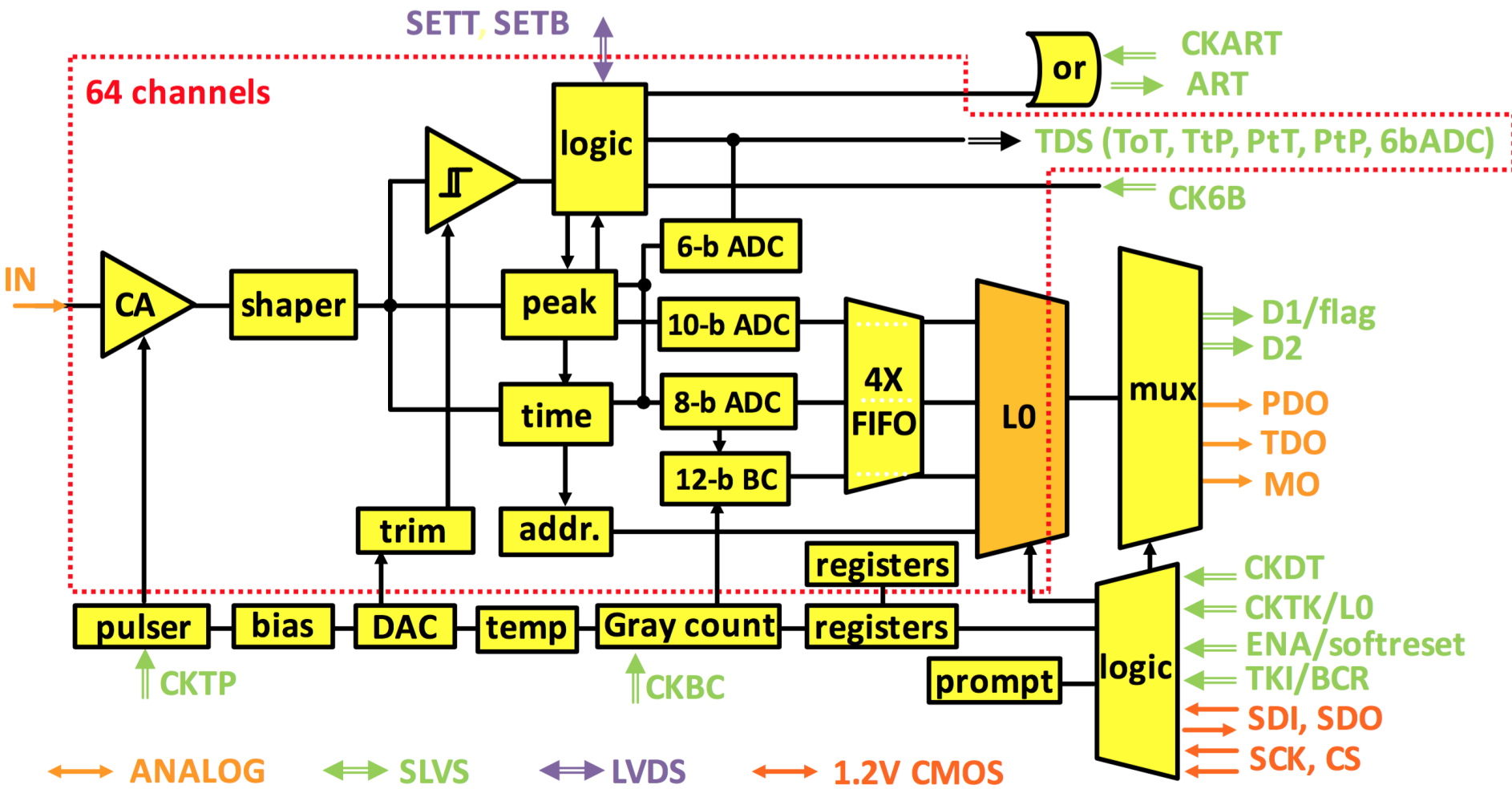
VMM1 (2012)
50 mm²
500k MOSFETs (8k/ch.)
- mixed-signal
- 2-phase readout



VMM2 (2014)
115 mm²
> 5M MOSFETs (>80k/ch.)
- planned deep re-design of VMM1
- much higher functionality and complexity than VMM1
- continuous fully-digital readout

VMM3 (2015-16)
130 mm²
> 6M MOSFETs
- **L0 handling, SEU-tolerant, SLVS IOs, deeply revised front-end for sTGC signals, various additional functions, various fixes**
- **input from many collaborating teams with broad range of expertise**
- **aims at pre-production**

VMM3 Block Diagram

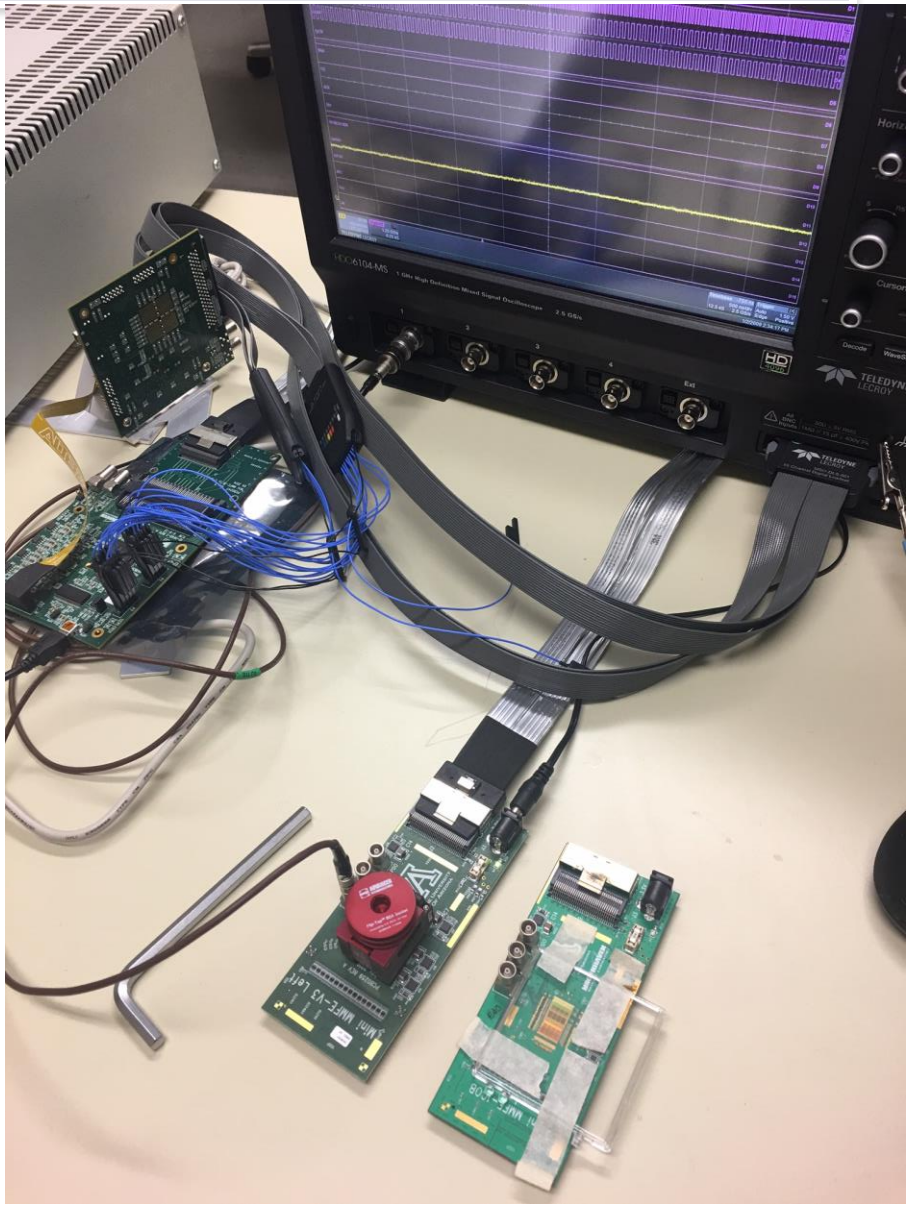


VMM3 in the Last few months

- Design submitted to MOSIS May 1, 2016
  - TDS and ART chips (ATLAS NSW) were included in the reticle
- 6 Engineering Wafers Received at MOSIS July 27
- Die Received at BNL in early August
  - Yield almost 100%
  - ~700 VMM3
- BGA Substrate layout completed in mid-September, checked and sent for fabrication
- 25 Production wafers were received at BNL end of September
  - Three wafers stolen on the way to a subcontractor in Marseille
  - Remaining are being packaged by Novapack (Grenoble, FR)
  - Received 150 packaged chips two weeks ago

• VMM3 Early Tests

- Received wire-bonded mini-one about a month ago (lab was being moved)
- Use LabView based system (CDAQ, J. Fried, W. Ding)
- VMM3 specific firmware mods
- UAz group assembled 2 boards with a socket base
- Brought one at CERN last week
- Same system but now many chips can be tested
- Testing here by G. Iakovidis (with Sorin for the L0 interface)
- Similar setup at BNL
- Work there by W. Ding, A. Gupta and Gianluigi
- A few more of these boards will be available (UAz) in a couple of weeks



Improvements

	Issue	Circuit	Solution	Status		Schedule
				sch	lay	
	Handling sTGC signals*	Analog front-end	Fbk time const., fbk capac, dyn. curr., tail-canc., …	✓	✓	✓
OK	**Early saturation***	Current-out peak detector	Matching, power distribution	✓	✓	✓
	MSB accumulation*	Current-out peak detector & ADC	Matching, optimization, parasitic reduction	in completion		Feb. 2016
OK	**Pulser DAC saturation**	DAC bias circuit	Optimization and biasing	✓	✓	✓
OK	**Pulser rise-time and noise**	Pulser circuit and injection switch	Redesign and switches optimization	✓	✓	✓
OK	**Prompt output disabled**	Control logic	Dedicated bit	✓	✓	✓
OK	**Event loss**	ADC reset logic	Logic fix	✓	✓	✓
OK	**Threshold bit error**	Discrimination logic	Logic fix	✓	✓	✓
OK	**BCID advance-latch issue**	Gray-code counter	Clock inversion	✓	✓	✓
OK	**Other data integrity issues***	Data, token & FIFO logic	Logic fixes and parasitic reduction	✓	✓	✓
OK	**Counter turnaround**	Counter logic	Logic fix	✓	✓	✓
	Front-end off w/SFM	Analog front-end	Fbk loop	✓	✓	✓
	Peak detect hold time*	Hold node	Dual input stage	✓	✓	✓
	Buffer float at bypass	Buffer input stage	Add switch	✓	✓	✓

*most demanding tasks

OK= Tested, no problems found but more detailed work needed to fully characterize it

OK = Verified OK

OK = Tested seems to work but observe issues that need to be understood or workaround available

MSB accumulation aka ADC problem shows similar behavior to the VMM2 but do not know extend

Additional Functions

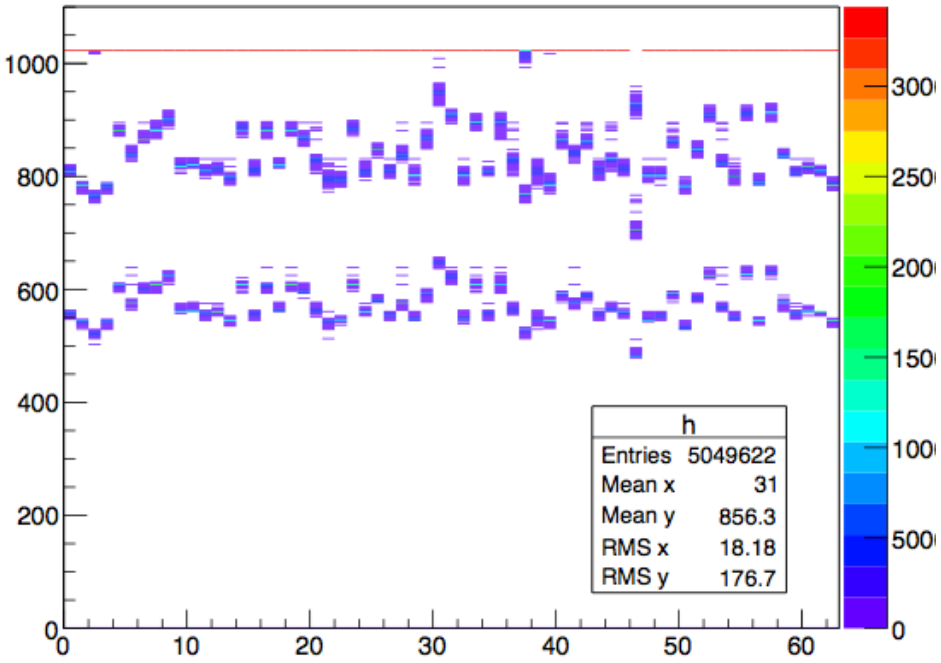
	Function	Circuit	Comment	Status		Expected Completion
				sch	lay	
	Handling sTGC capacitance*	Analog front-end	Fbk capac., dyn. current	✓	✓	✓
OK	**L0 handling logic***	Digital implementation	*Collab. w/ Sorin Martoiu*	in completion		Feb. 2016
OK	**Simultaneous high-res. & prompt readout***	Various logic changes	Programmable early stop also added	✓	✓	✓
OK	**Single-ended configuration and global reset**	Configuration logic and IOs	CS active low, high-Z SDO with CS	✓	✓	✓
OK	**SLVS-400 IOs**	IOs	Program. termination	✓	✓	✓
	Timing ramp optimization	Timing circuit	60, 100, 200, 400ns	✓	✓	✓
	Timeout ramp autoreset	Timing circuit	Programmable > 800ns	✓	✓	✓
OK	**Acquisition reset on ENA**	Control logic	Falling edge	✓	✓	✓
	32-channel skip	Inter-channel logic	Skip 17-48	✓	✓	✓
OK	**ART flag synchronization**	ART logic	Programmable synk/async	✓	✓	✓
	SEU tolerant registers	Configuration logic	DICE	✓	✓	✓
	SEU tolerant state logic	State logic	Redundant and locking	✓	✓	✓
OK	**Pulser range extension**	Injection circuit	Programmable capacitor	✓	✓	✓
	Timing ramp at threshold	Timing circuit	Programmable thr. vs peak	✓	✓	✓

*most demanding tasks

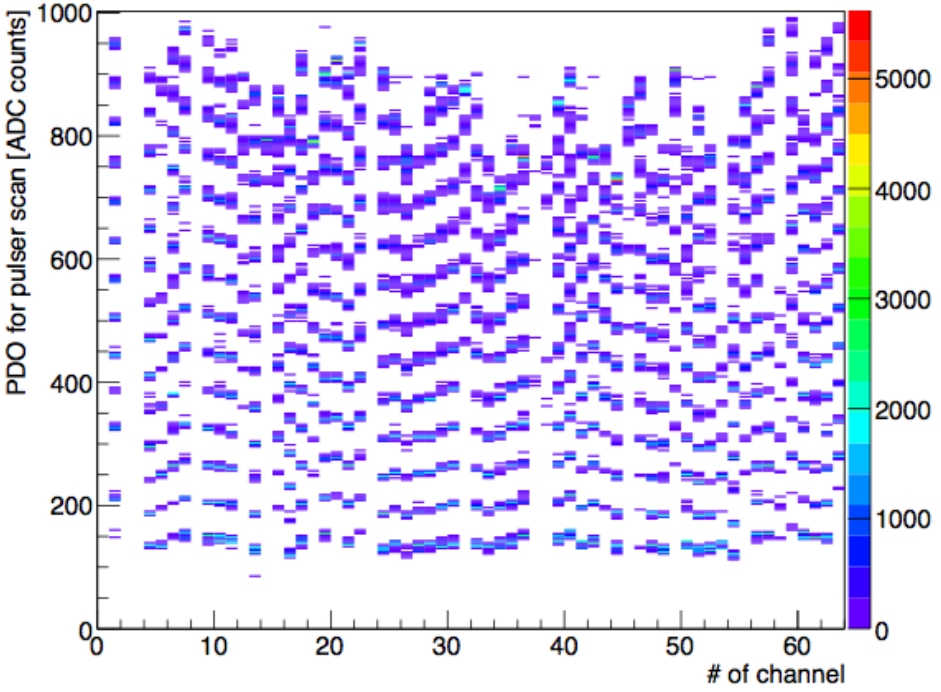
Early saturation comparison

- Distribution of PDO across all the channels, early saturation seems to be fixed.

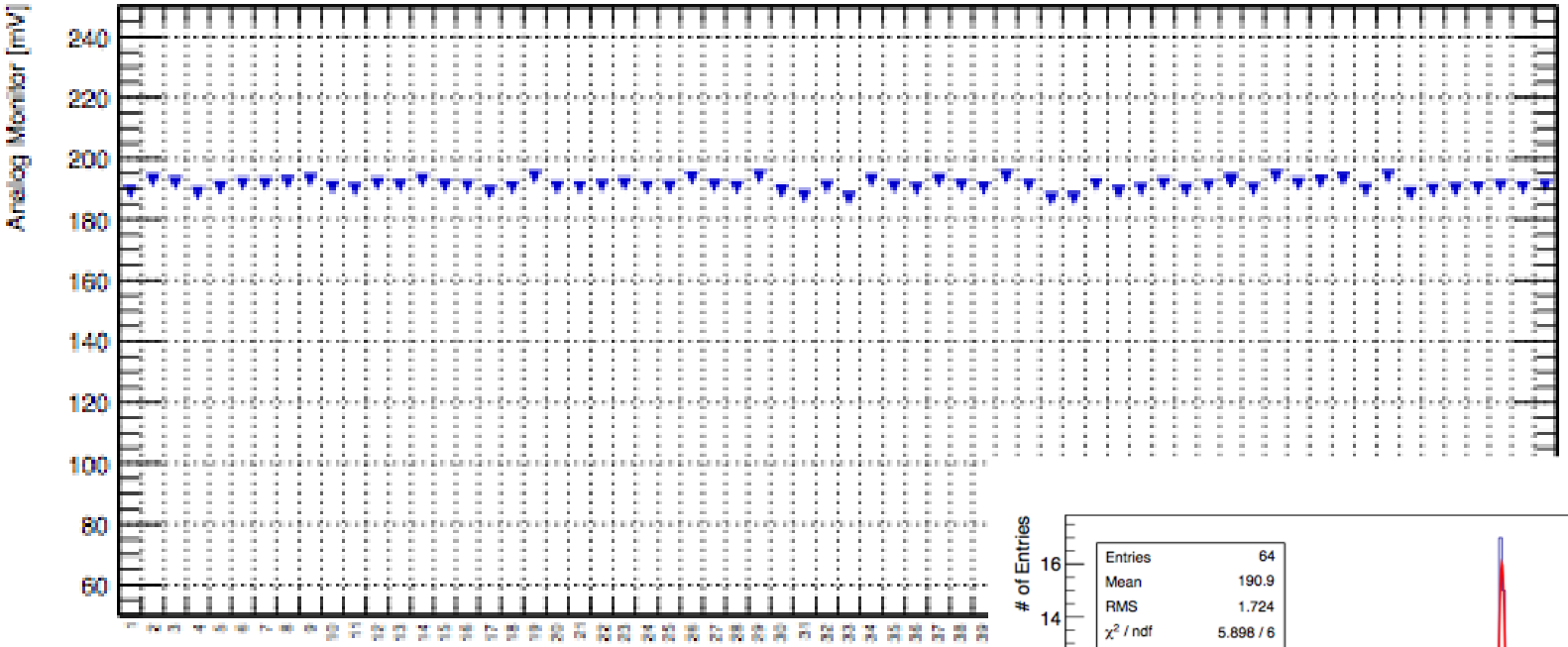
VMM3

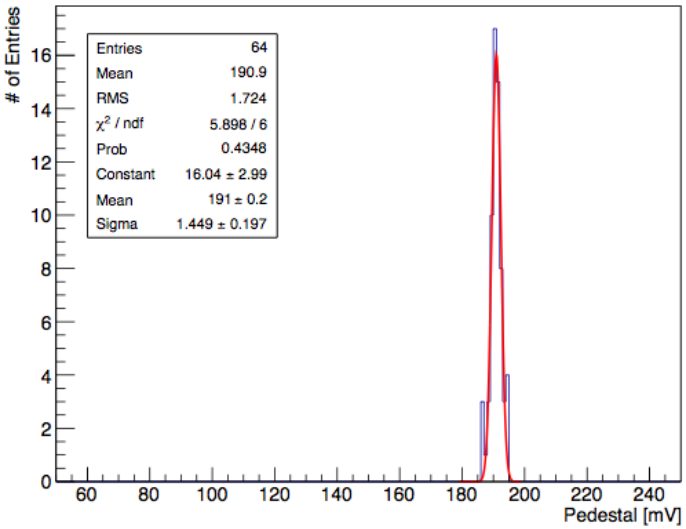


VMM2



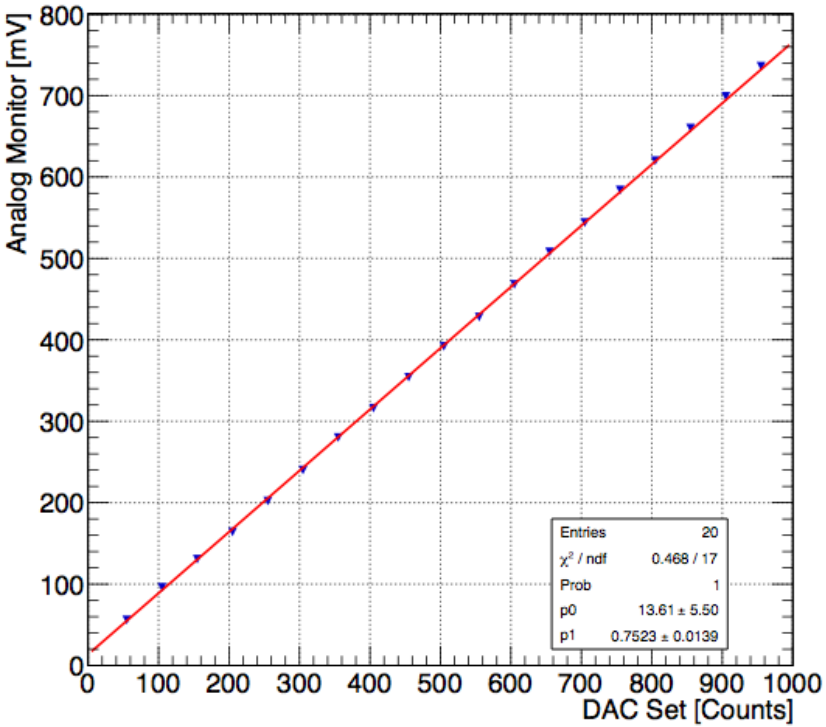
Pedestals


Analog Monitor [mV]
240
220
200
180
160
140
120
100
80
60

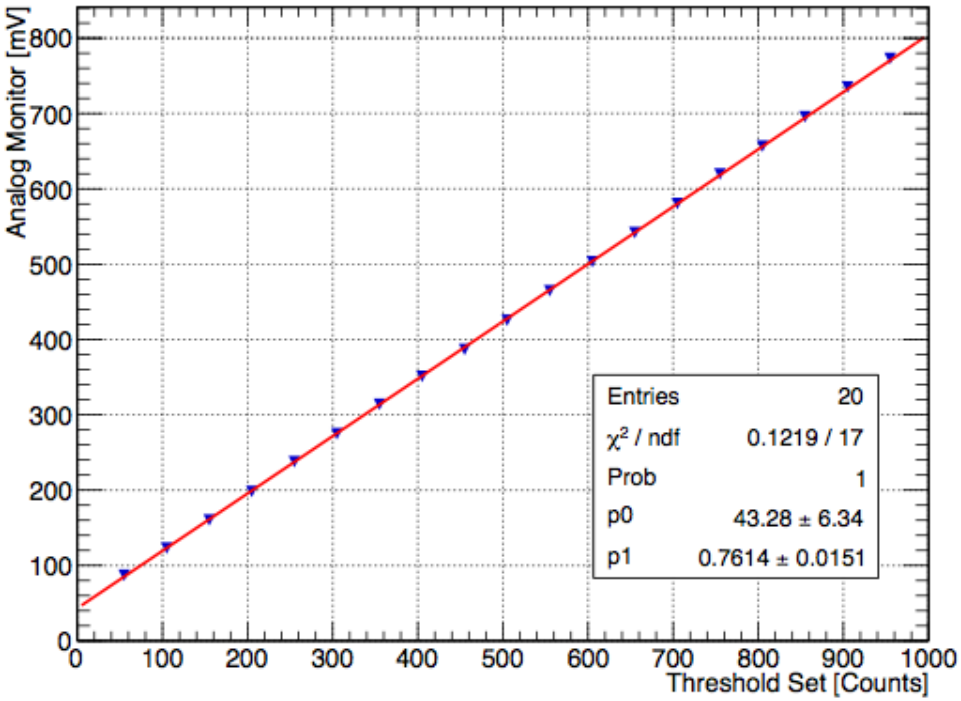

# of Entries
Entries 64
Mean 190.9
RMS 1.724
χ² / ndf 5.898 / 6
Prob 0.4348
Constant 16.04 ± 2.99
Mean 191 ± 0.2
Sigma 1.449 ± 0.197
0
2
4
6
8
10
12
14
16
60
80
100
120
140
160
180
200
220
240
Pedestal [mV]

DACs – VMM3

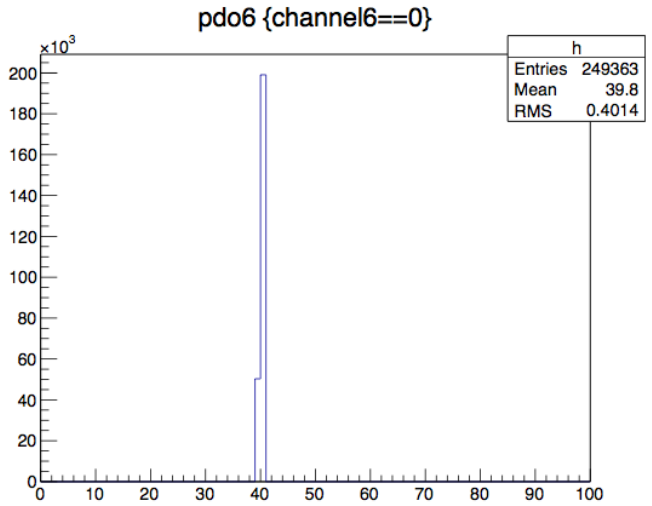
Pulser [mV] vs DAC count – VMM3

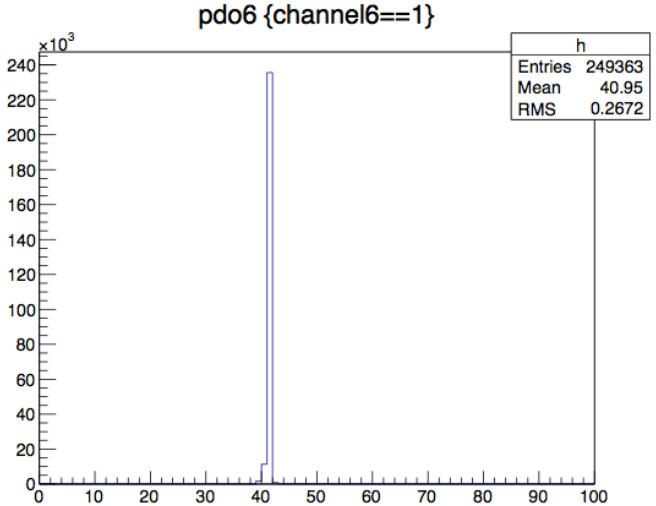


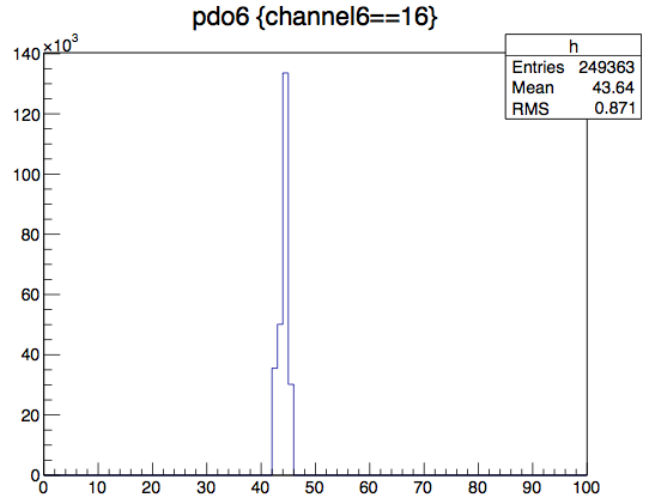
Threshold mV versus Counts - VMM3

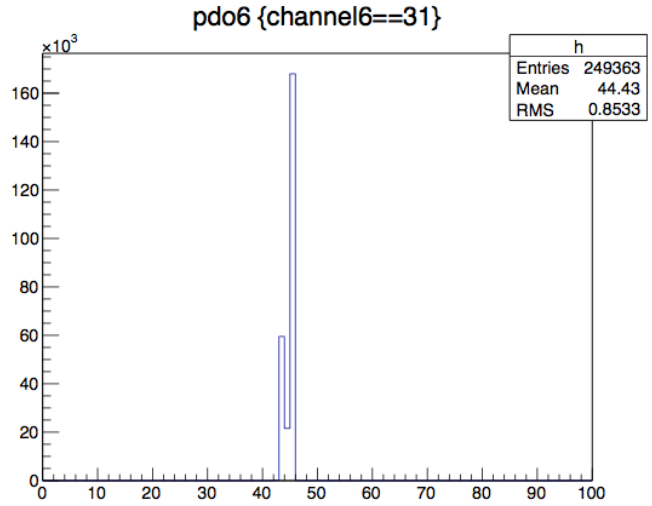


6-bit adc (sTGC direct outputs)









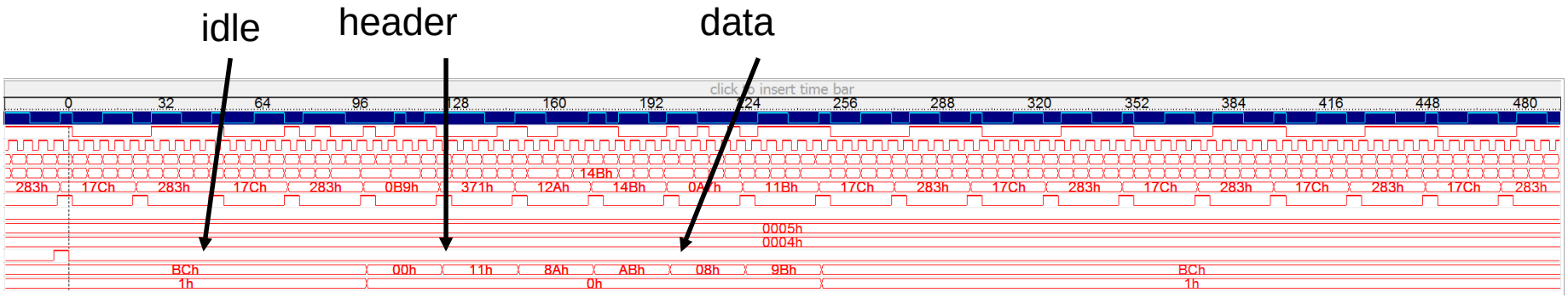
VMM3 Operating Modes

- There are basically four Data Acquisition modes
  - Analog Mode (with external Digitizer, e.g. SRS C-card)
  - Digital triggered mode (digital SRS card)
  - Continuous triggered deadtimeless mode (simultaneous read/write)
  - Continuous triggerless mode
- In the two continuous modes the digital output is in form of GBTx compatible e-links
  - Can handle up to 1 MHz trigger rate
- Two primitives can be used for Trigger
  - Fast OR with address of the first hit strip
  - Parallel prompt output of 6-bit amplitudes that can be used for a more complex trigger (50 ns digitization)

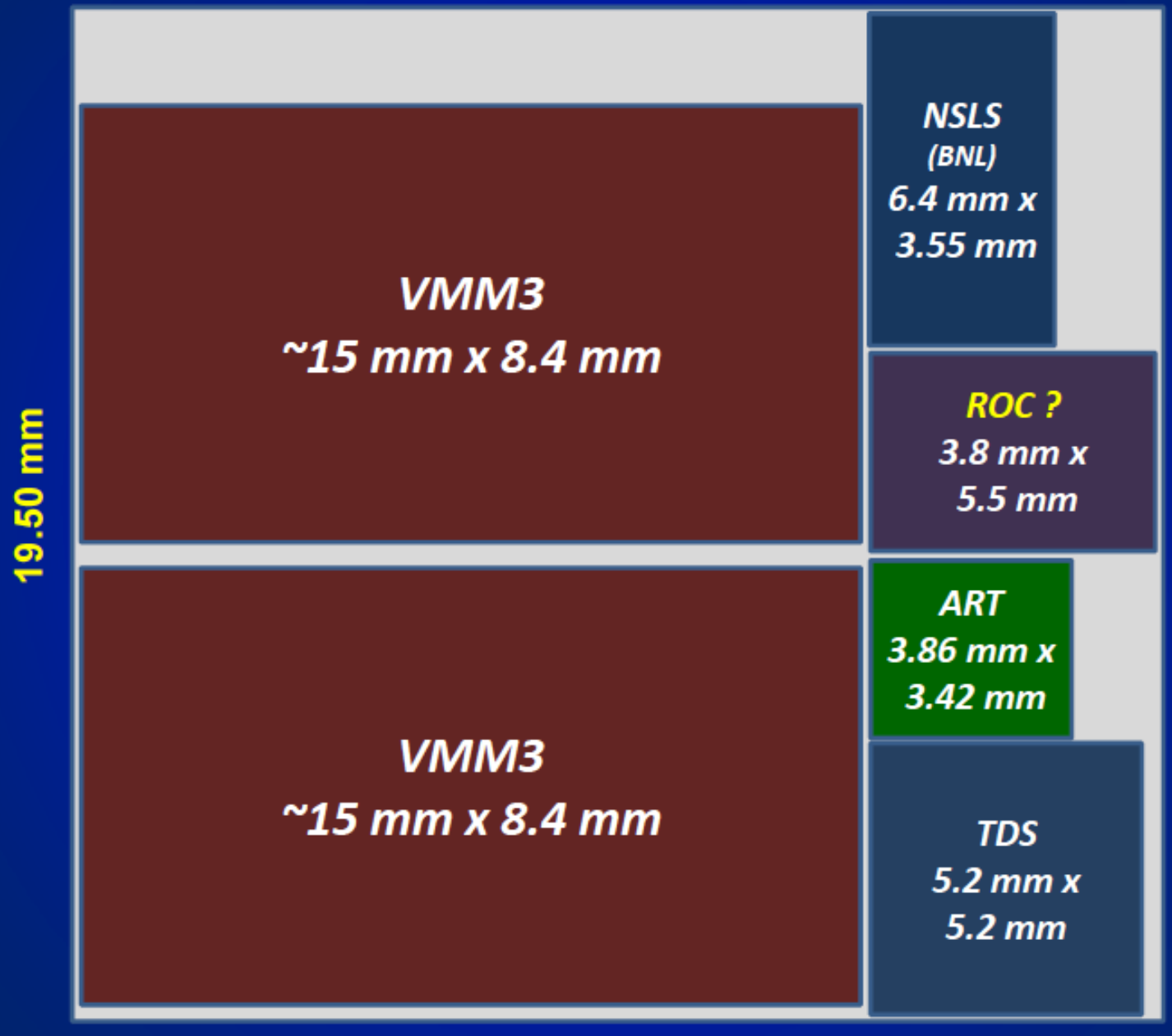
L0 testing - Screenshot from the scope

Continuous Triggered Readout

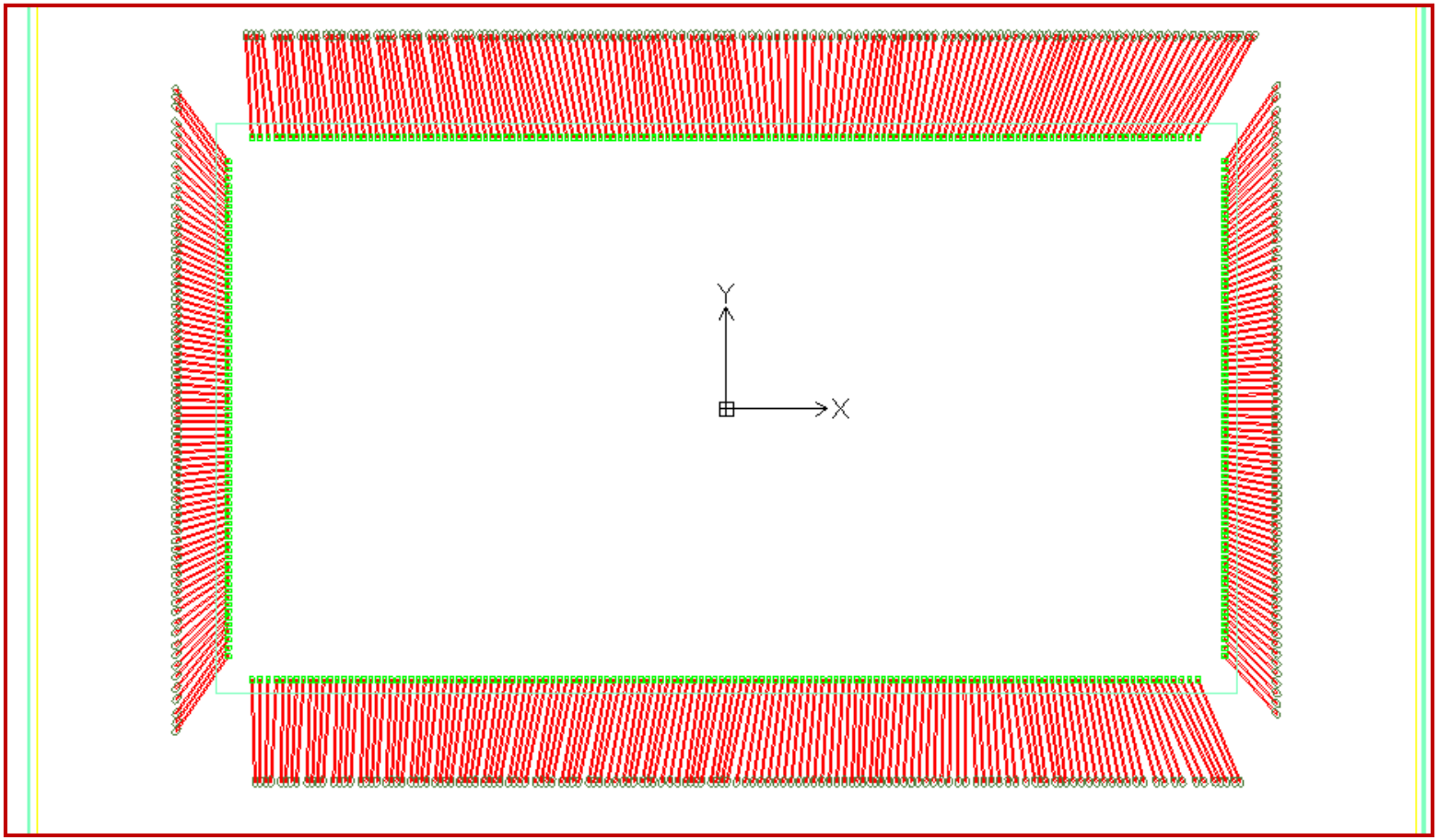
- L0 logic enable works correctly, the core is functioning
- IDLE state works (after swapping the DATA0/1 lines), comma character 0xBC is there (k28.5)
- OCR, BCR works correctly
- Header format is correct, BCID is identified correctly
- Data format is correct, relative BCID works correctly
- Multiple L0 give the correct amount of DATA
- Registers are handled correctly
- 8b/10b encoding works correctly
- Truncation works
- Stress tests will be performed to evaluate system performance on overflows



Wafer Reticle Occupancy

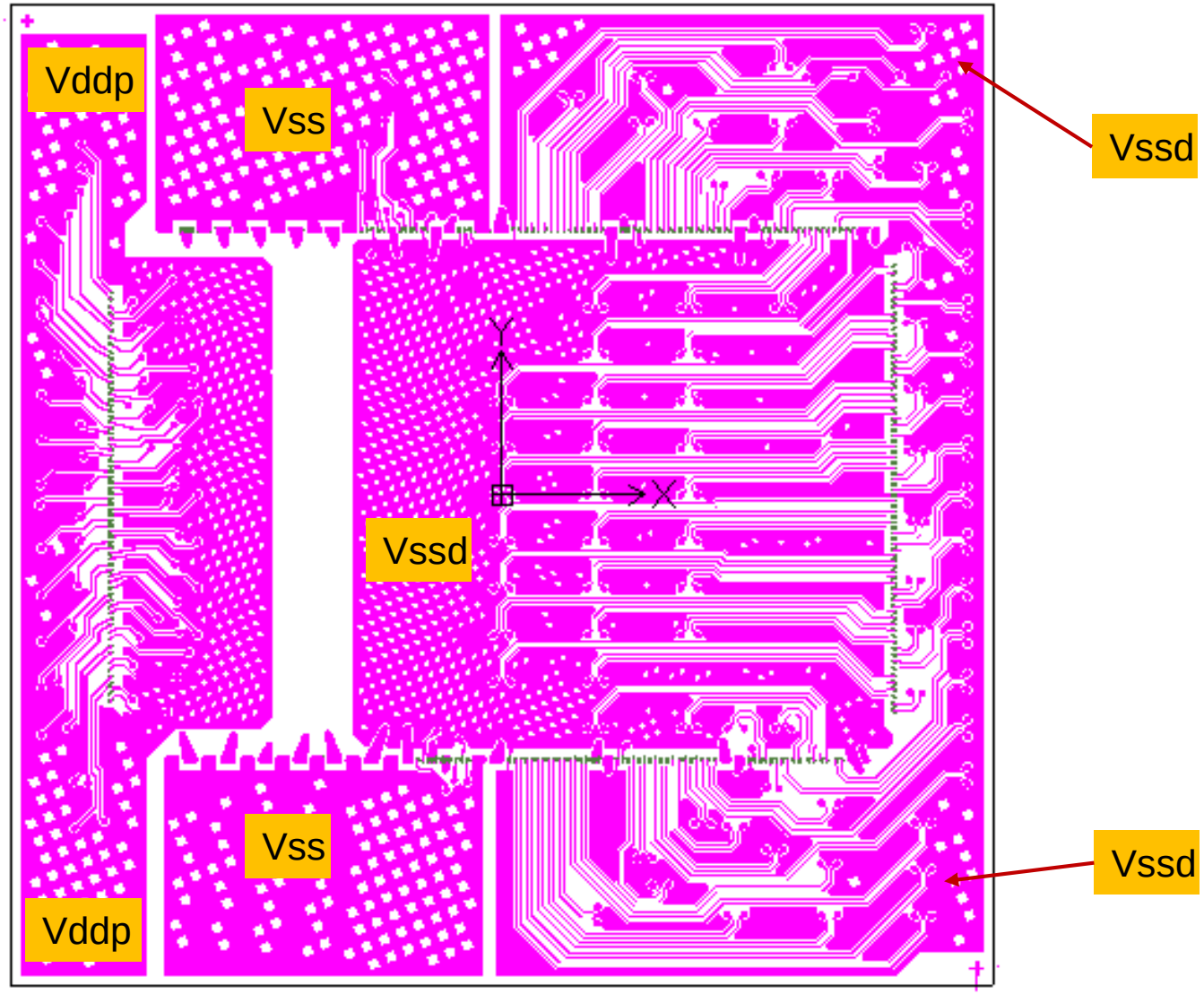


BONDING DIAGRAM

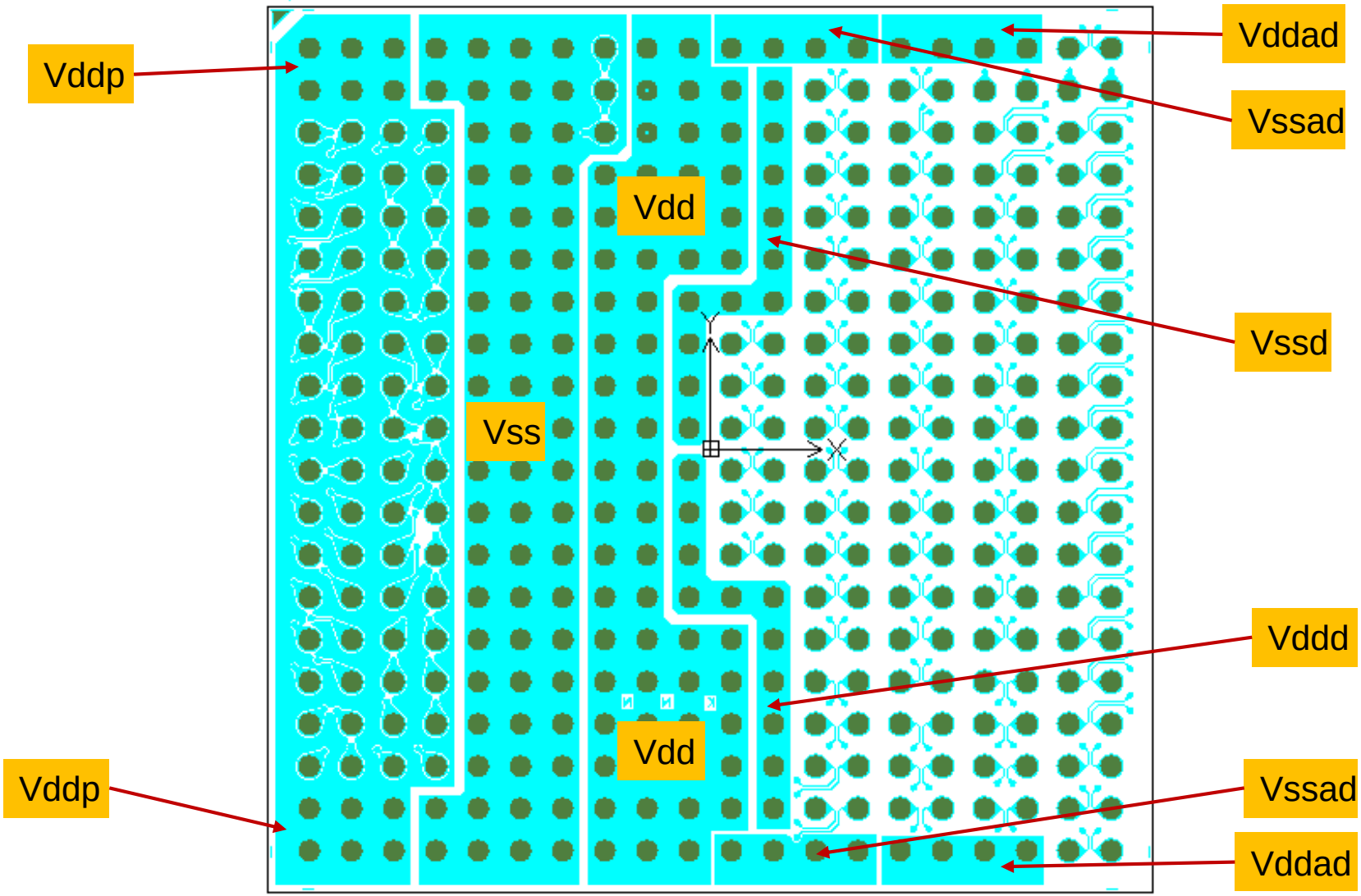


NOTE:
reduction of wire length Vs VMM2 design in order to keep a similar substrate routing (especially on East & West sides)

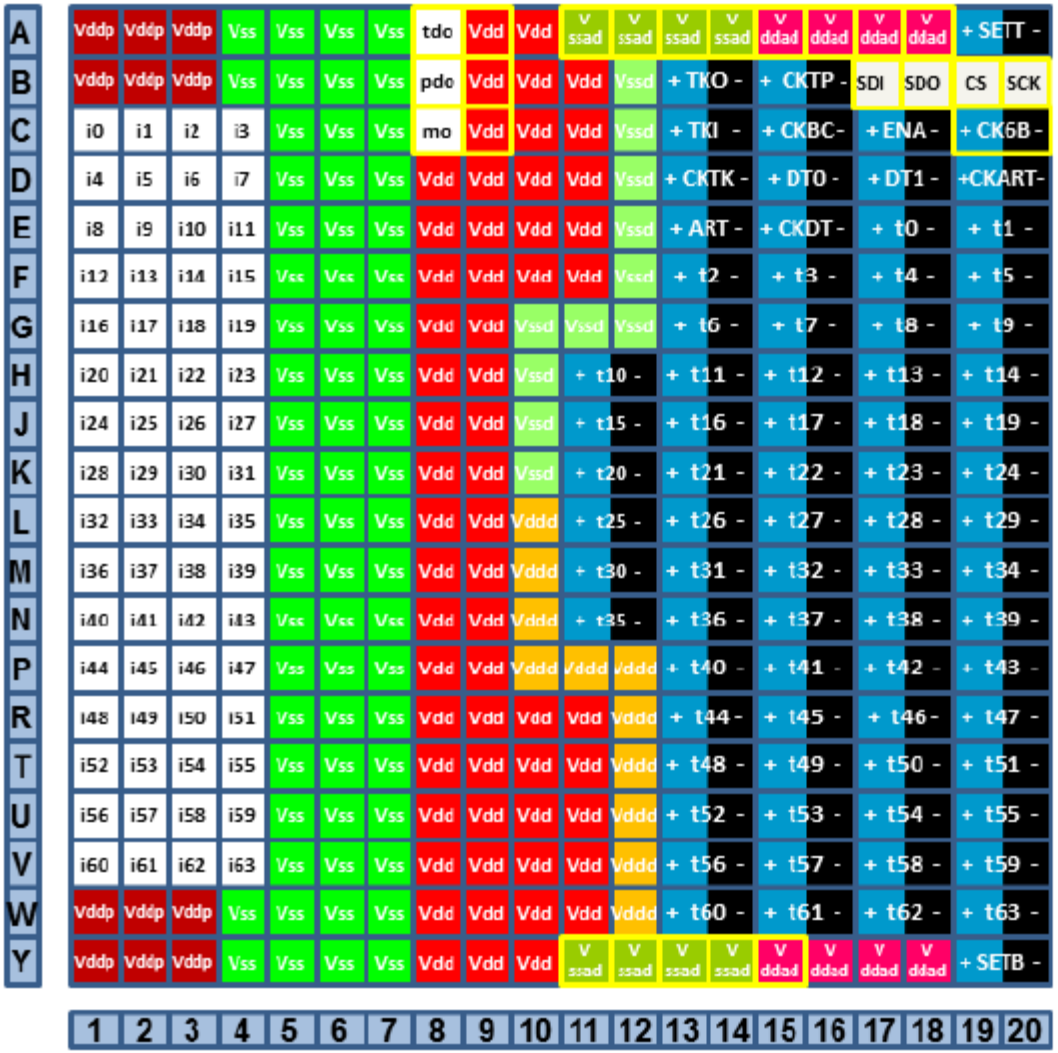
LAYER M1 (top layer)



LAYER M2 (bottom layer)



BALL-OUT BGA 21x21-400 balls
VMM3 DICE



NOTE: SLVS = differential pairs (100 Ohms)

Summary, Next Steps

- So far VMM3 seems to be mostly OK
- Differential nonlinearity of the 10-bit and 8-bit ADC still there but perhaps to a lesser extend, testing is on-going
- Analog mode (of interest perhaps to the RD51 community) is fine and can be used if desired
- Samples can be available to those interested
  - ~30 unpackaged dice reserved for RD51 tests
- If ADC performance is good enough for NSW a large order will be placed ~May 2017.
- We can add quantities for any group that may be interested
- No export license needed
  - CERN working for a universal license for all ASICs fabricated by Global Foundries, please check with P. Farthouat