Operational tools

Laurette Ponce
BE-OP

Context

- After the 19th September, a re-enforcement of access control during powering tests was requested
- Access system designed to cope with radiation hazard ONLY, not electrical or cryogenic risks
- Not possible to implement a “hardware” link between access system and converters during this shutdown)
- For personnel safety, 2 powering phases have been defined, with different access restrictions AND hardware/software limitations of the current
- In addition of these measures and the procedure, a SOFTWARE interlock has been implemented

Outlines

- Hardware and software limits
- Software interlock
  - Principle of the interlock
  - The tools used to build the logic
  - Consequences for PO
- How to switch from PO phase 1 to PO phase 2

Hardware and software limits

- To guarantee the safety of personnel during powering phase 1, current has to be limited in the main magnets as proposed to the safety Task-force (EDMS 1001985) :
  - RB - 100A
  - RQF/RQD - 800A
  - RQ4-RQ10 - 900A
  - IPD - 1000A
  - RQX - 800A
  - RQTX2 - 600A
  - RQTX1 - 132A
- 2 types of limitation on PC side:
  - For RB, RQF and RQD: hardware limits in the power converter
  - For IPQ, IPD : FGC software limits
- Another software limits in the operational database:
  - Redefinition of I_max in LSA
  - This is the max current used by the sequencer

Additional tools for OP

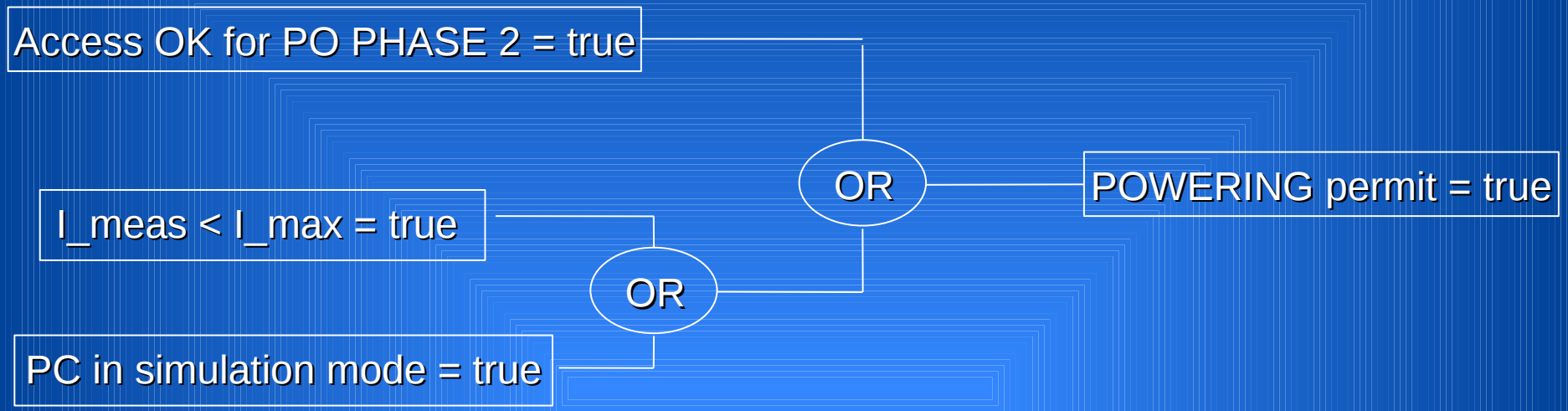
- A software interlock for checking access conditions versus current in the magnets
- Proposal for 2 fixed displays
- The software interlock is based on several different softwares to build the signals needed for the logic : more details in the following slides
- The main components are the LHC Software Interlock System, the LHC Access Control System and TIM (TI supervision tool)

Principle of the interlock

- The principle is to stop **all the power converters of a sector** in case the current level in one of them is not compatible with the actual access conditions in the sector:
  - to prevent powering above the defined level during powering phase 1
  - to stop the powering above so called “safe current level” in case of intrusion during powering phase 2

- The Interlock is on the PCs, not on the access system:
  - The access conditions (which zones are patrolled and empty) define the level of current allowed in the whole sector
  - No action on the access system, just reading of the status

The logic



- The logic is built inside the LHC Software Interlock System
- Origin of the signals:
  - PC OP mode and I_Meas are read and combined by the SIS
  - Access OK comes from a LASER alarm (via LACS and TIM software)
  - POWERING permit = false triggers on change from true to false a GLOBAL REMOVE_PERMIT to each PIC of the powering sector

The tools used to build the interlock

- PIC
  - To remove the PC permit of the PCs
  - Use the new GLOBAL REMOVE_PERMIT command
- The SIS:
  - To combine the signals and evaluate the powering permit
  - To export the slow power command to the PIC
- The LASS/LACS
  - To extract the patrol status
- TIM
  - To combine the individual signal form the LACS and export to LASER
- LASER
  - To publish access conditions readable from SIS

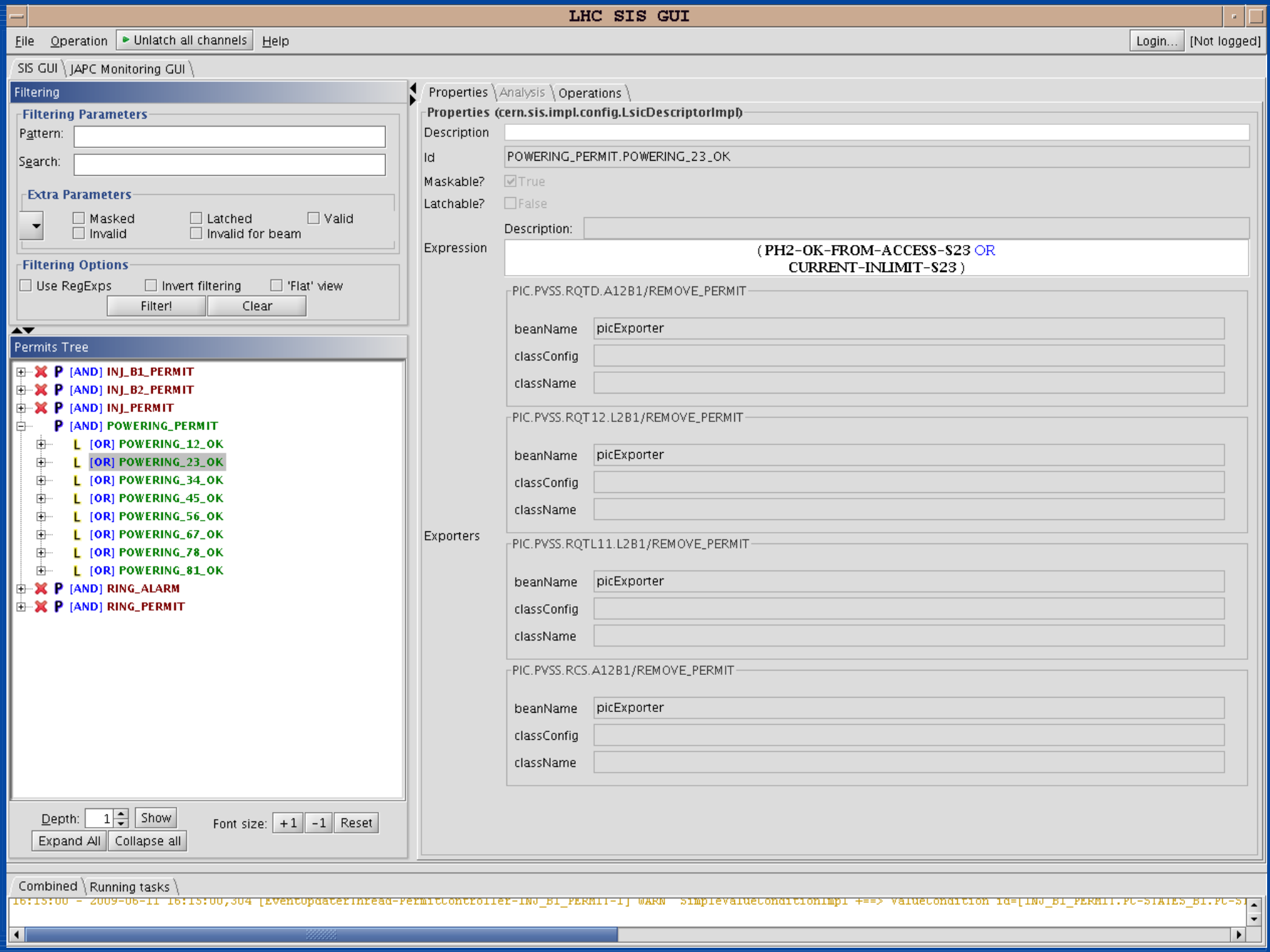
How it works

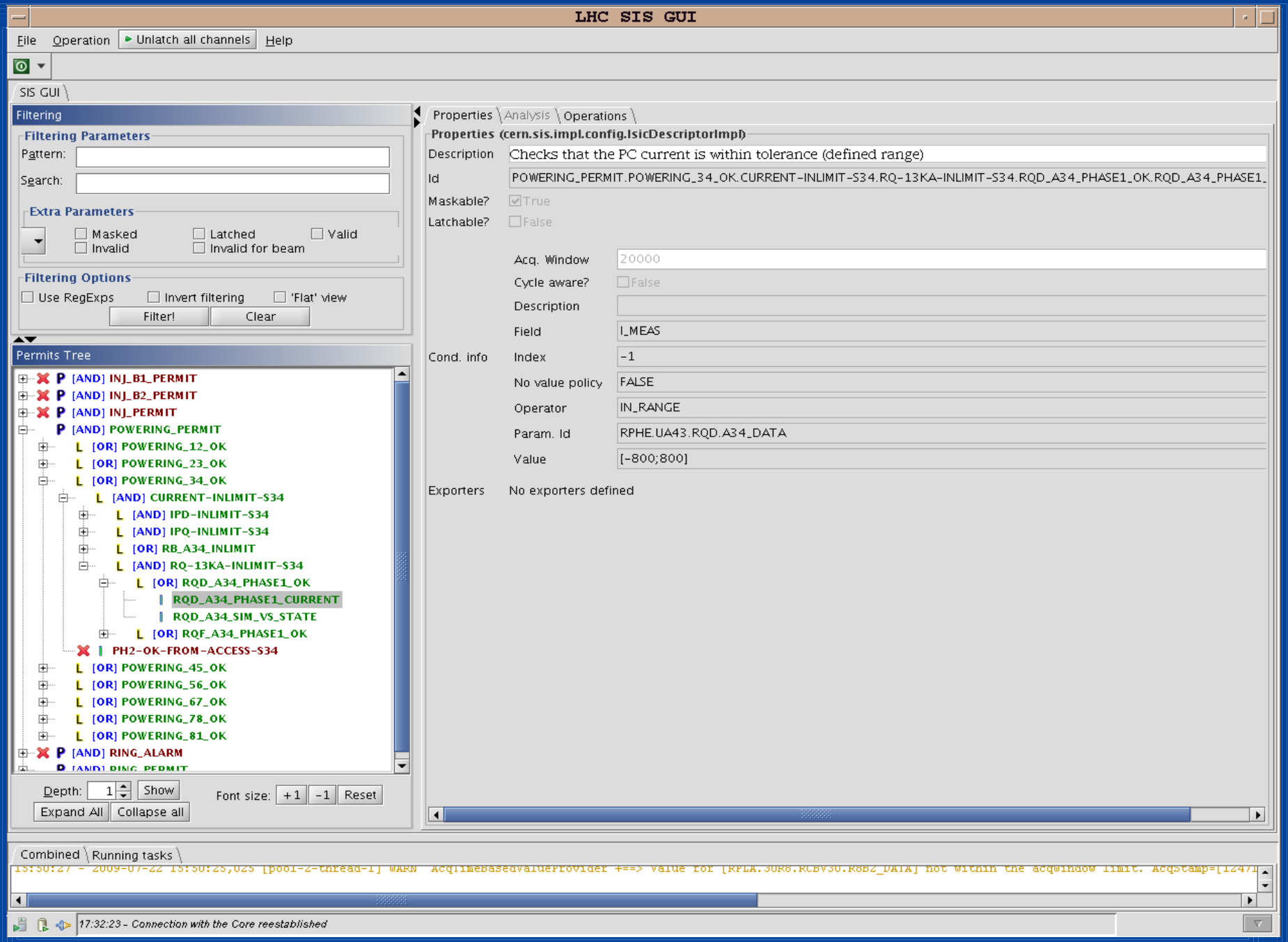
- There is one POWERING_permit per sector
- The GLOBAL REMOVE_PWRMIT is sent to all the PIC of the sector (LSS + arc)
- Constant monitoring of the measured current (I_meas) and the OP mode in the main circuits of the sector:
  - RB, RQD, RQF, IPQ, IPD, RQX are monitored
  - 600 A, 120A and 60A NOT monitored

    => CURRENT-INLIMIT-Sxx signal = true if all the I_meas < I_max or PC in simulation mode

- Constant monitoring of the access conditions for the concerned sector:
  - Status of the patrol
  - Just a concatenation of the LASS info

    => PH2-OK-FROM-ACCESS-Sxx signal = true if all the access sub-sectors defined according to the access matrix are SAFE


LHC SIS GUI
File
Operation
Unlatch all channels
Help
Login...
[Not logged]
SIS GUI
JAPC Monitoring GUI
Filtering
Filtering Parameters
Pattern:
Search:
Extra Parameters
Masked
Latched
Valid
Invalid
Invalid for beam
Filtering Options
Use RegExps
Invert filtering
'Flat' view
Filter!
Clear
Permits Tree
[AND] INJ_B1_PERMIT
[AND] INJ_B2_PERMIT
[AND] INJ_PERMIT
[AND] POWERING_PERMIT
[OR] POWERING_12_OK
[OR] POWERING_23_OK
[OR] POWERING_34_OK
[OR] POWERING_45_OK
[OR] POWERING_56_OK
[OR] POWERING_67_OK
[OR] POWERING_78_OK
[OR] POWERING_81_OK
[AND] RING_ALARM
[AND] RING_PERMIT
Depth:
Show
Expand All
Collapse all
Font size:
+1
-1
Reset
Properties
Analysis
Operations
Properties (cern.sis.impl.config.LsicDescriptorImpl)
Description
Id
POWERING_PERMIT.POWERING_23_OK
Maskable?
True
Latchable?
False
Description:
Expression
(PH2-OK-FROM-ACCESS-S23 OR
CURRENT-INLIMIT-S23)
Exporters
PIC.PVSS.RQTD.A12B1/REMOVE_PERMIT
beanName
picExporter
classConfig
className
PIC.PVSS.RQT12.L2B1/REMOVE_PERMIT
beanName
picExporter
classConfig
className
PIC.PVSS.RQTL11.L2B1/REMOVE_PERMIT
beanName
picExporter
classConfig
className
PIC.PVSS.RCS.A12B1/REMOVE_PERMIT
beanName
picExporter
classConfig
className
Combined
Running tasks


LHC SIS GUI
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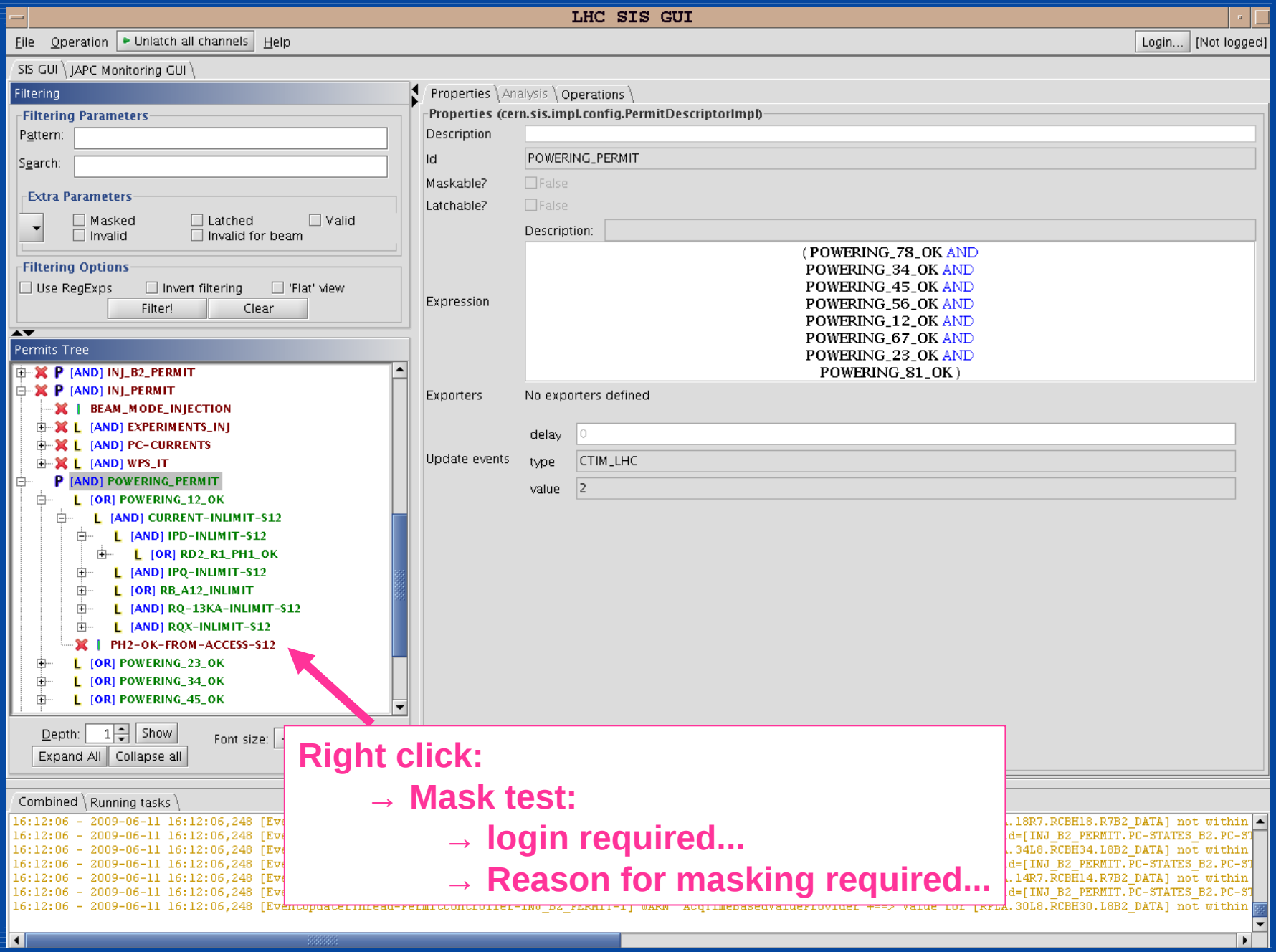
[AND] INJ_PERMIT
[AND] POWERING_PERMIT
[OR] POWERING_12_OK
[OR] POWERING_23_OK
[OR] POWERING_34_OK
[AND] CURRENT-INLIMIT-S34
[AND] IPD-INLIMIT-S34
[AND] IPQ-INLIMIT-S34
[OR] RB_A34_INLIMIT
[AND] RQ-13KA-INLIMIT-S34
[OR] RQD_A34_PHASE1_OK
RQD_A34_PHASE1_CURRENT
RQD_A34_SIM_VS_STATE
[OR] RQF_A34_PHASE1_OK
PH2-OK-FROM-ACCESS-S34
[OR] POWERING_45_OK
[OR] POWERING_56_OK
[OR] POWERING_67_OK
[OR] POWERING_78_OK
[OR] POWERING_81_OK
[AND] RING_ALARM
Depth:
Show
Expand All
Collapse all
Font size:
+1
-1
Reset
Properties
Analysis
Operations
Properties (cern.sis.impl.config.IsicDescriptorImpl)
Description
Checks that the PC current is within tolerance (defined range)
Id
POWERING_PERMIT.POWERING_34_OK.CURRENT-INLIMIT-S34.RQ-13KA-INLIMIT-S34.RQD_A34_PHASE1_OK.RQD_A34_PHASE1_
Maskable?
True
Latchable?
False
Acq. Window
20000
Cycle aware?
False
Description
Field
I_MEAS
Cond. info
Index
-1
No value policy
FALSE
Operator
IN_RANGE
Param. Id
RPHE.UA43.RQD.A34_DATA
Value
[-800;800]
Exporters
No exporters defined
Combined
Running tasks
17:32:23 - Connection with the Core reestablished

Reliability of the parameters

- Problem: numerous software for the access conditions evaluation:
  - LASS (Safety System) signals are exported to the LACS (Control System)
  - LACS is publishing the signals to TIM
  - TIM signals are combined in a rule to create an alarm
  - This alarm is published by LASER
  - SIS is reading LASER alarm
- The REMOVE_PERMIT is sent to the PIC via CMW
- Software has been tested during sector 23 tests :
  - The load on the PIC is OK, signals received within few seconds
  - Tests interrupted several times, but no unexplained triggers
  - We have identified PO procedures which are not compatible with the logic
- Note : the current measure is not latched anymore
- Systematic test are needed : to be defined within the DSO tests?

Consequences for PO

- During phase 1, access conditions are never met, so the current within limit = true is needed to have the PC permit
- If signals from the FGC are not arriving or the I_meas values published are above the limits during phase 1, PC permit is removed to all the PCs of the sector. Some exemples:
  - A restart of the FGC is stopping any ongoing tests
  - Same for calibration when I_meas is simulated
  - Maybe others...?
- When FGC restart or calibration are needed, PO expert should first contact the EiC so that he masks the concerned circuit :
  - Discipline is needed as soon as tests are starting in a sector
  - Masking is a fast procedure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Filtering Options
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Invert filtering
'Flat' view
Filter!
Clear
Permits Tree
[AND] INJ_B2_PERMIT
[AND] INJ_PERMIT
BEAM_MODE_INJECTION
[AND] EXPERIMENTS_INJ
[AND] PC-CURRENTS
[AND] WPS_IT
[AND] POWERING_PERMIT
[OR] POWERING_12_OK
[AND] CURRENT-INLIMIT-S12
[AND] IPD-INLIMIT-S12
[OR] RD2_R1_PH1_OK
[AND] IPQ-INLIMIT-S12
[OR] RB_A12_INLIMIT
[AND] RQ-13KA-INLIMIT-S12
[AND] RQX-INLIMIT-S12
PH2-OK-FROM-ACCESS-S12
[OR] POWERING_23_OK
[OR] POWERING_34_OK
[OR] POWERING_45_OK
Depth:
Show
Expand All
Collapse all
Font size:
Properties
Analysis
Operations
Properties (cern.sis.impl.config.PermitDescriptorImpl)
Description
Id
POWERING_PERMIT
Maskable?
False
Latchable?
False
Description:
Expression
(POWERING_78_OK AND
POWERING_34_OK AND
POWERING_45_OK AND
POWERING_56_OK AND
POWERING_12_OK AND
POWERING_67_OK AND
POWERING_23_OK AND
POWERING_81_OK)
Exporters
No exporters defined
Update events
delay
0
type
CTIM_LHC
value
2
Combined
Running tasks
16:12:06 - 2009-06-11 16:12:06,248
Right click:
→ Mask test:
→ login required...
→ Reason for masking required...

Switching from PHASE 1 to PHASE 2

- The complete procedure is described in a engineering specification under preparation LHC-MPP-ES-0003 (EDMS 1012328)
- During the whole procedure, no powering is allowed and all the PC of the sector should be LOCKED by PIC.
- The order of the actions are to be carefully followed :
  - Block the circuit
  - Proper information of the change (HW coordinator + LSA)
  - Establish access conditions (patrols)
  - Update the software limits in database
  - Remove the hardware limits
  - Synchronize FGC and careful check by PO expert
  - Final check of all is OK by EiC, helped by SIS and LASS
  - Unblock the circuits

Switching from PHASE 2 to PHASE 1

- When sector is defined in Phase 2, no powering is allowed in the sector when access is needed, even below the phase 1 current
- If required, then we will have to switch back to phase and re-establish the hardware and software limits

- For both switching, no change are needed for the SIS interlock: can be constantly running during the procedure
- Some questions:
  - The tracking of hardware/FGC limits is done by PO
  - Communication between HWC/OP and PO is crucial
  - Do we need more tools to ease the tracking? A kind of yellow paper for HW limits?

More tools

- The powering phases are now defined as a sector mode : this is published in LSA : sequence available to change it
- A fixed display will show the mode of each sector and the access conditions (still in preparation...)

			people in zone
Sector 12	PO phase 1	Access OK	0
Sector 23	Cool down	Access OK	0
Sector 34	PO phase 2	Access OK	0
Sector 45	Shutdown	Access OK	0
Sector 56	PO phase 1	Access OK	2
Sector 67	Cool down	Access OK	3
Sector 78	PO phase 1	Access OK	1
Sector 81	Cool down	Access OK	9

- Proposal for another fixed display, as help for volunteers giving access :

Zone	ITX 1R	LSS 1 R	Arc 12	LSS 2L	ITX 2L
People IN	UJ 16			UJ23	
PC ON	RQX	IPD/IPQ/corr	RB/RQ/600A	IPD/IPQ/corr	RQX

Summary

- The interlock is now deployed and constantly running
- We can try to improve the logic in order to allow calibration, but I would like to keep it as simple as possible
- Need to be tested with partial DSO tests before the start of the powering phase 2

- The interlock is stopping the Power Converter, not blocking the access...
- In case of doubt, the LASS gives the real status...

- Safety is guaranteed by:
  - Hardware and FGC software limits
  - Procedure to be apply for giving access
- SIS interlock is another independent way of checking that current is limited when people are accessing.