2nd review of the EuroCirCol WP5, 9-10 Oct. 2017

Dipole circuit layout and protection

M. Prioli and T. Salmi

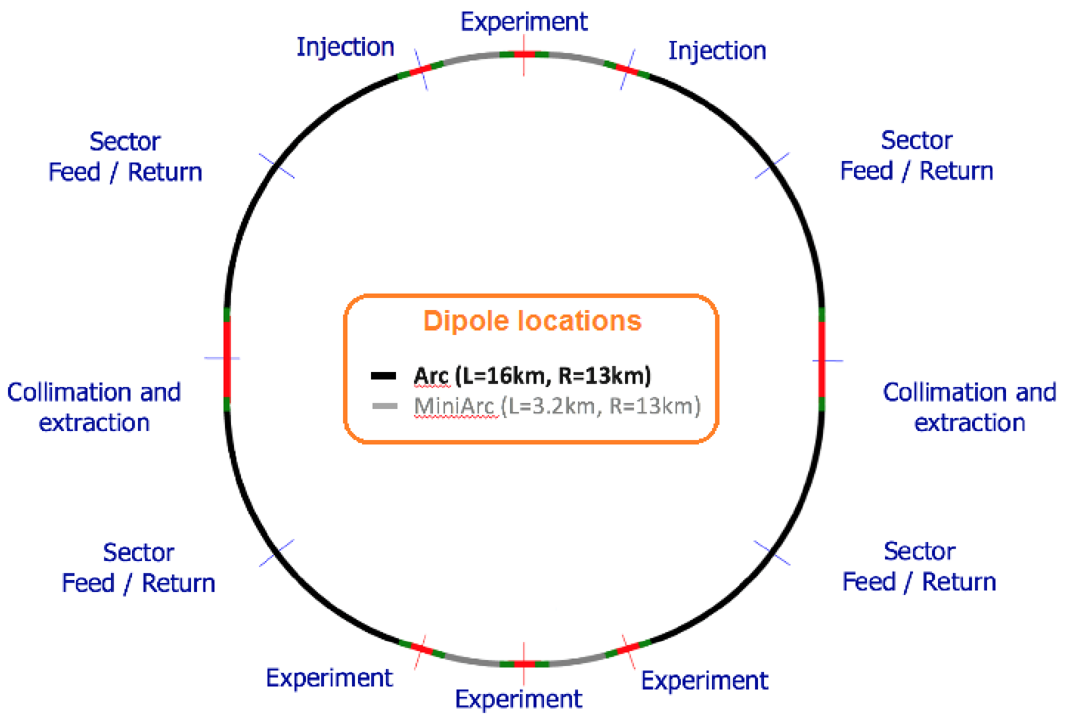
With contributions from: B. Auchmann, L. Bortot, M. Maciejewski, M. Mentink, E. Ravaioli, A. Verweij

FOR

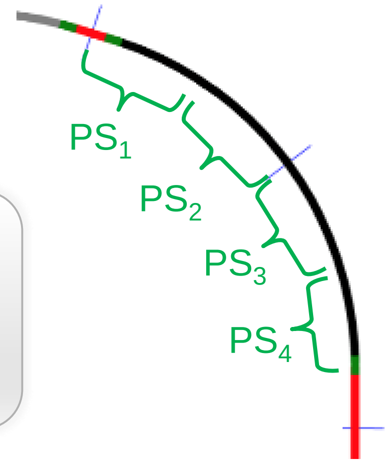
Motivation and input parameters

	Nominal current I_{nom} [kA]	Stored energy @ I_{nom} (2 ap.) [MJ]
Cos-theta	11.2	37
Block coil	10.0	38
Common coil	16.1	42
Canted cos-theta	18.0	46
LHC MB	11.9	7

	Number	Length [km]	Number of magnets
Arc	4	16	876
Mini-arc	4	3.2	180
LHC arc	8	3	154



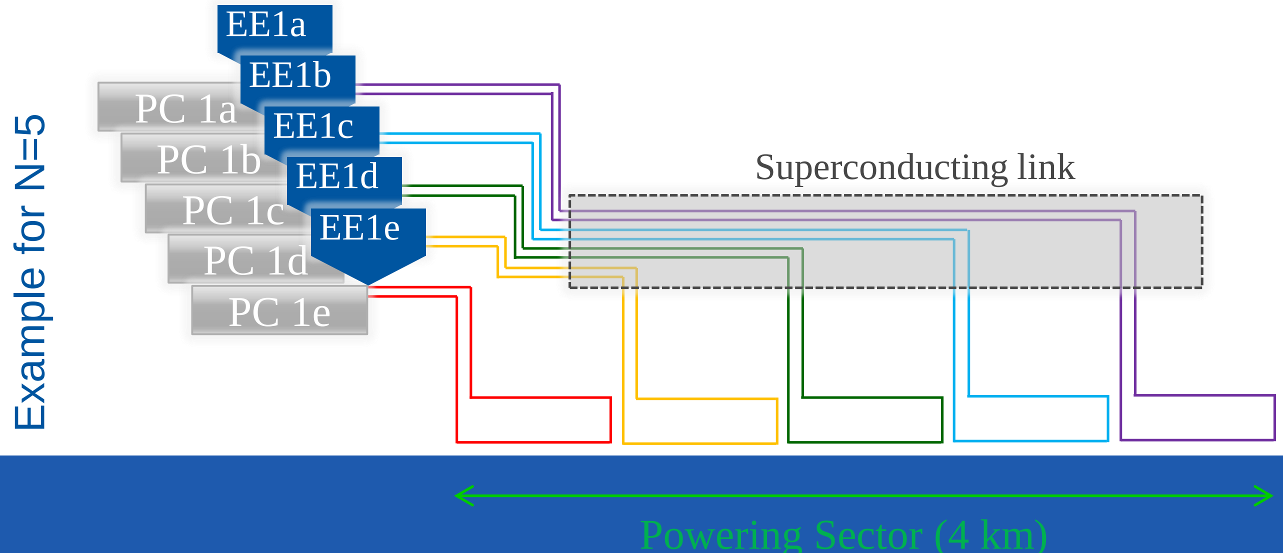
Circuit design strategy



Power converters (PC) and energy extractors (EE) close to access points

- ➢ Space optimization and easier maintenance

1. Subdivide the 16 km long arc in four powering sectors (PS) …
2. … and each sector in *N* circuits (20*N* circuits in total including mini-arcs)
3. Locate PC and EE close to access points
4. Power the circuits through a superconducting link
5. Equip each circuit with one EE system



Circuit design targets

1. Reduce the overall circuits complexity
   - Smaller impact on reliability
2. Limit the number of magnets in series in a circuit
   - Reduce the training time
3. Limit the energy of a circuit
   - Reduce the consequences of fault scenarios

Circuit design targets

1. Reduce the overall circuits complexity
   - Smaller impact on reliability
2. Limit the number of magnets in series in a circuit
   - Reduce the training time
3. Limit the energy of a circuit
   - Reduce the consequences of fault scenarios
4. Ramp-up and ramp-down time similar to LHC (20 minutes)
   - Limit the turnaround time
5. Limit the peak power of converters
   - Lower accelerator power demand

Circuit design targets

1. Reduce the overall circuits complexity
   - Smaller impact on reliability
2. Limit the number of magnets in series in a circuit
   - Reduce the training time
3. Limit the energy of a circuit
   - Reduce the consequences of fault scenarios
4. Ramp-up and ramp-down time similar to LHC (20 minutes)
   - Limit the turnaround time
5. Limit the peak power of converters
   - Lower accelerator power demand
6. Limit the required Voltage Withstand Level
   - 1.3 kV as voltage to ground budget for the circuit

$$VWL = f * (V_{Mag,\ quench} + 2.5 * V_{Cir,\ fault})$$

1.2 *1200* *1300*

7. Discharge time in fast power abort mode similar to LHC (100 s)
   - Limit the number of neighbouring quenching magnets to reduce the cryo-recovery time
8. Limit the busbars size
   - Easier layout inside the cryostat

Circuit design targets

1. Reduce the overall circuits complexity
   - Smaller impact on reliability
2. Limit the number of magnets in series in a circuit
   - Reduce the training time
3. Limit the energy of a circuit
   - Reduce the consequences of fault scenarios
4. Ramp-up and ramp-down time similar to LHC (20 minutes)
   - Limit the turnaround time
5. Limit the peak power of converters
   - Lower accelerator power demand
6. Limit the required Voltage Withstand Level
   - 1.3 kV as voltage to ground budget for the circuit

$$VWL = f * (V_{Mag,\ quench} + 2.5 * V_{Cir,\ fault})$$

1.2 1200 1300

7. Discharge time in fast power abort mode similar to LHC (100 s)
   - Limit the number of neighbouring quenching magnets to reduce the cryo-recovery time
8. Limit the busbars size
   - Easier layout inside the cryostat
9. Avoid spurious triggers of quench detection system (QDS)
   - Maximize availability

Circuit design targets

1. Reduce the overall circuits complexity
   - Smaller impact on reliability
2. Limit the number of magnets in series in a circuit
   - Reduce the training time
3. Limit the energy of a circuit
   - Reduce the consequences of fault scenarios
4. Ramp-up and ramp-down time similar to LHC (20 minutes)
   - Limit the turnaround time
5. Limit the peak power of converters
   - Lower accelerator power demand
6. Limit the required Voltage Withstand Level
   - 1.3 kV as voltage to ground budget for the circuit

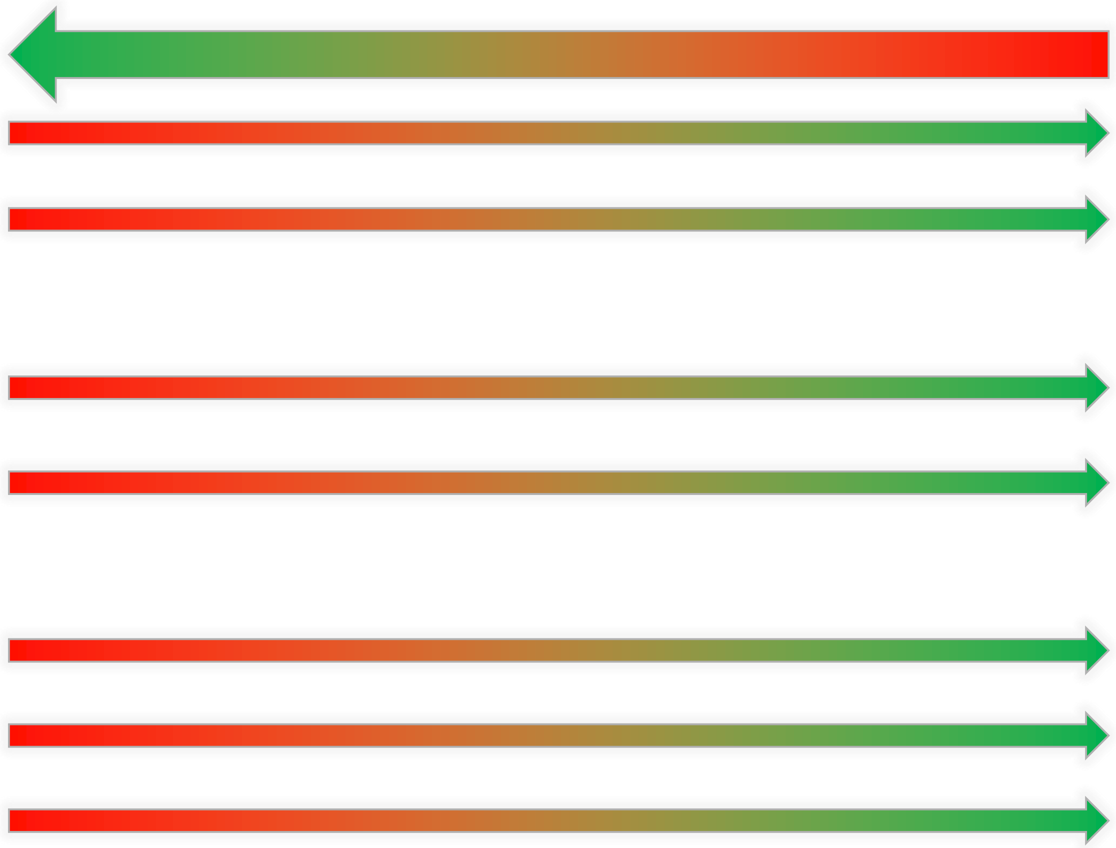
   $VWL = f * (V_{Mag,\ quench} + 2.5 * V_{Cir,\ fault})$

   1.2 1200 1300
7. Discharge time in fast power abort mode similar to LHC (100 s)
   - Limit the number of neighbouring quenching magnets to reduce the cryo-recovery time
8. Limit the busbars size
   - Easier layout inside the cryostat
9. Avoid spurious triggers of quench detection system (QDS)
   - Maximize availability

Circuit design targets

Number of circuits per PS (N)	1	2	3	4	5	6	7	8

1. Complexity
2. N magnets
3. Energy
4. Ramp-up time
5. PC peak power
6. Voltage to ground
7. FPA discharge
8. Busbar size



Circuit design

Number of circuits per PS (N)	1	2	3	4	5	6	7	8	LHC
Total number of circuits	20	40	60	80	100	120	140	160	8
Number of magnets per circuit	219	110	73	55	44	37	32	28	154
Circuit energy [GJ]	8.1	4.1	2.7	2.0	1.6	1.4	1.2	1.0	1.1

Circuit design

$t_{ramp} = 20$ min

Number of circuits per PS (N)	1	2	3	4	5	6	7	8	LHC
Total number of circuits	20	40	60	80	100	120	140	160	8
Number of magnets per circuit	219	110	73	55	44	37	32	28	154
Circuit energy [GJ]	8.1	4.1	2.7	2.0	1.6	1.4	1.2	1.0	1.1
PC max voltage [V]	1202	604	401	302	241	203	176	154	150
PC peak power [MW]	13.5	6.8	4.5	3.4	2.7	2.3	2.0	1.7	1.8

Circuit design

	Number of circuits per PS (N)	1	2	3	4	5	6	7	8	LHC
	Total number of circuits	20	40	60	80	100	120	140	160	8
	Number of magnets per circuit	219	110	73	55	44	37	32	28	154
	Circuit energy [GJ]	8.1	4.1	2.7	2.0	1.6	1.4	1.2	1.0	1.1
t_{ramp} = 20 min	PC max voltage [V]	1202	604	401	302	241	203	176	154	150
	PC peak power [MW]	13.5	6.8	4.5	3.4	2.7	2.3	2.0	1.7	1.8
V_{gnd} = 1.3 kV	Time to 37% of nominal current [s]	555	279	185	139	111	94	81	71	100
	MIITs [MA^2*s]	35E+3	18E+3	12E+3	9E+3	7E+3	6E+3	5E+3	5E+3	7E+3
	Busbar cross-section (ΔT=300K) [mm^2]	490	350	280	240	220	200	180	170	200

V_{gnd} = 450V

CERN

Circuit design

Number of circuits per PS (N)	1	2	3	4	5	6	7	8	LHC
Total number of circuits	20	40	60	80	100	120	140	160	8
Number of magnets per circuit	219	110	73	55	44	37	32	28	154
Circuit energy [GJ]	8.1	4.1	2.7	2.0	1.6	1.4	1.2	1.0	1.1
PC max voltage [V]	1202	604	401	302	241	203	176	154	150
PC peak power [MW]	13.5	6.8	4.5	3.4	2.7	2.3	2.0	1.7	1.8
Time to 37% of nominal current [s]	555	279	185	139	111	94	81	71	100
MIITs [MA^2*s]	35E+3	18E+3	12E+3	9E+3	7E+3	6E+3	5E+3	5E+3	7E+3
Busbar cross-section (ΔT=300K) [mm^2]	490	350	280	240	220	200	180	170	200

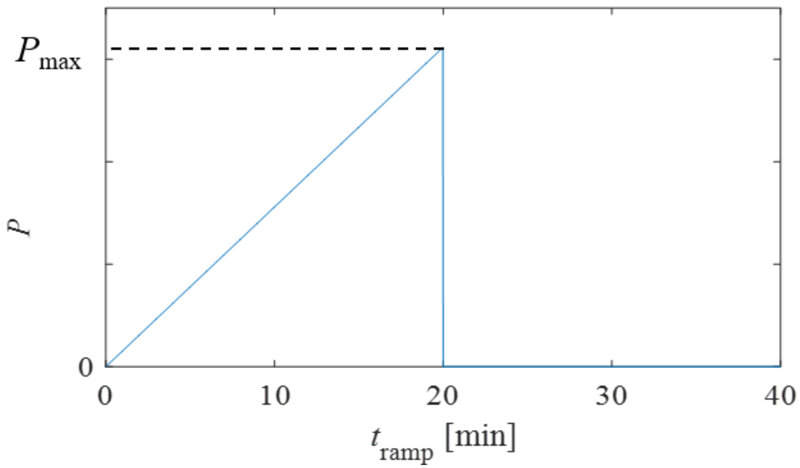
t_{ramp} = 20 min

V_{gnd} = 1.3 kV

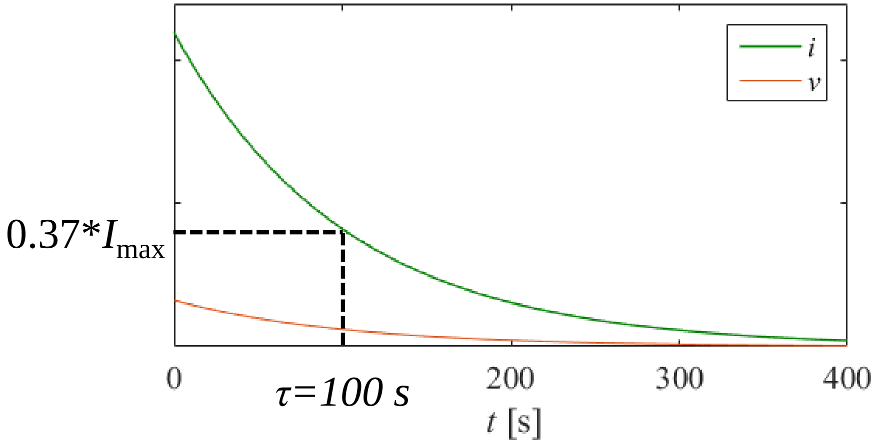
V_{gnd} = 450V

Different ramp-up and EE strategies

Ramp-up with constant voltage

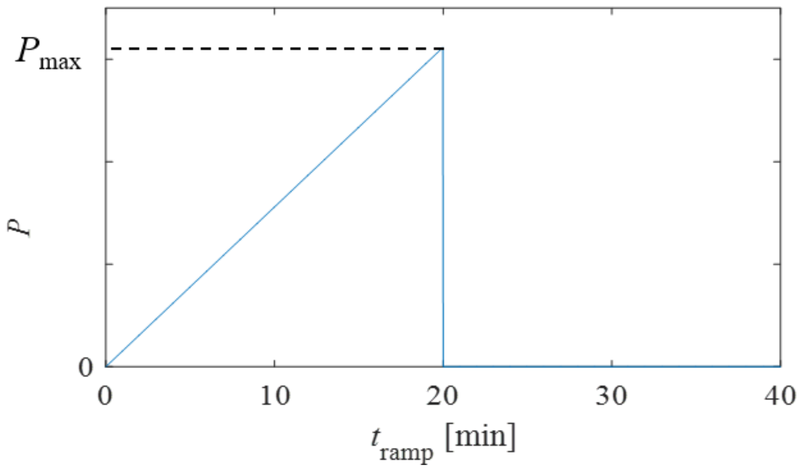


EE with resistor

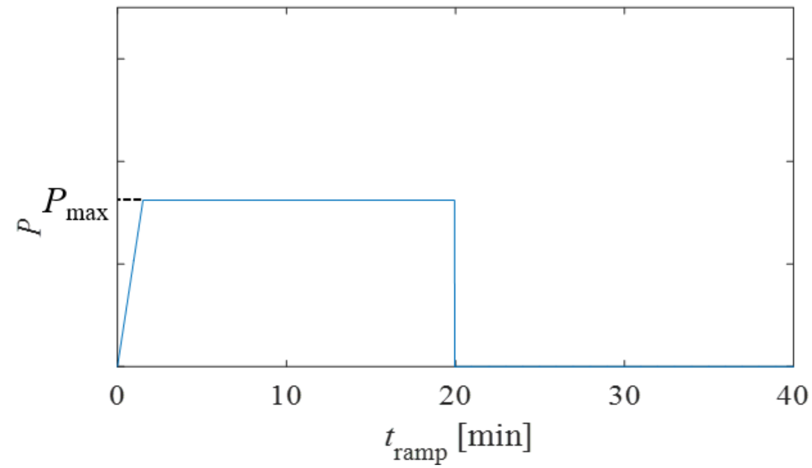


Different ramp-up and EE strategies

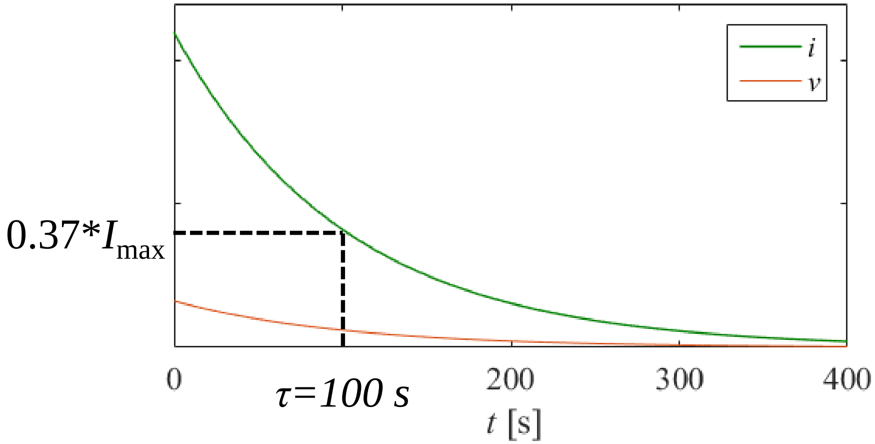
Ramp-up with constant voltage



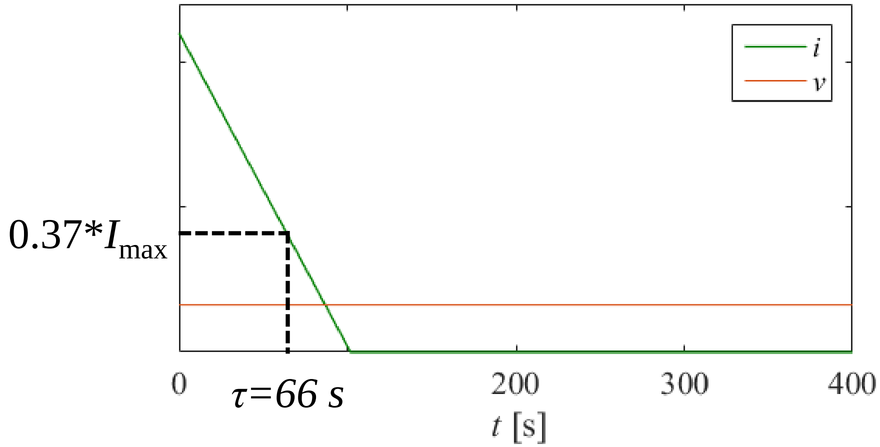
Ramp-up with constant power



EE with resistor



EE with constant voltage*



Circuit design

	Number of circuits per PS (N)	1	2	3	4	5	6	7	8
	Total number of circuits	20	40	60	80	100	120	140	160
	Number of magnets per circuit	219	110	73	55	44	37	32	28
	Circuit energy [GJ]	8.1	4.1	2.7	2.0	1.6	1.4	1.2	1.0
t_{ramp} = 20 min	PC max voltage [V]	2403	1207	801	603	483	406	351	307
	PC peak power [MW]	7.2	3.6	2.4	1.8	1.5	1.2	1.1	0.93
V_{gnd} = 1.3 kV	Time to 37% of nominal current [s]	351	176	117	88	70	59	51	45
	MIITs [MA^2*s]	23.4E+3	11.7E+3	7.8E+3	5.9E+3	4.7E+3	3.9E+3	3.4E+3	3.0E+3
	Busbar cross-section (ΔT=300K) [mm^2]	390	270	220	190	170	160	140	130

Circuit design

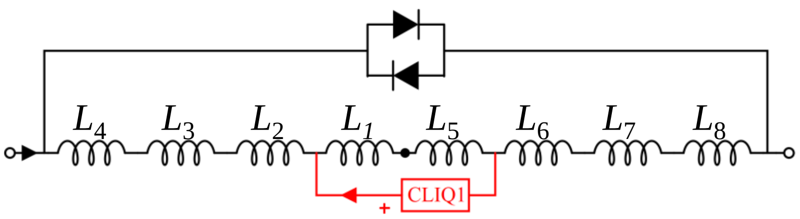
<table>
<tr><th></th><th>Number of circuits per PS (N)</th><th>1</th><th>2</th><th>3</th><th>4</th><th>5</th><th>6</th><th>7</th><th>8</th></tr>
<tr><td></td><td>Total number of circuits</td><td>20</td><td>40</td><td>60</td><td>80</td><td>100</td><td>120</td><td>140</td><td>160</td></tr>
<tr><td></td><td>Number of magnets per circuit</td><td>219</td><td>110</td><td>73</td><td>55</td><td>44</td><td>37</td><td>32</td><td>28</td></tr>
<tr><td></td><td>Circuit energy [GJ]</td><td>8.1</td><td>4.1</td><td>2.7</td><td>2.0</td><td>1.6</td><td>1.4</td><td>1.2</td><td>1.0</td></tr>
<tr><td rowspan="2">t_{ramp} = 20 min</td><td>PC max voltage [V]</td><td colspan="8">+100%</td></tr>
<tr><td>PC peak power [MW]</td><td colspan="8">-46%</td></tr>
<tr><td rowspan="3">V_{gnd} = 1.3 kV</td><td>Time to 37% of nominal current [s]</td><td colspan="8">-37%</td></tr>
<tr><td>MIITs [MA^2*s]</td><td colspan="8">-33%</td></tr>
<tr><td>Busbar cross-section (ΔT=300K) [mm^2]</td><td colspan="8">-21%</td></tr>
</table>

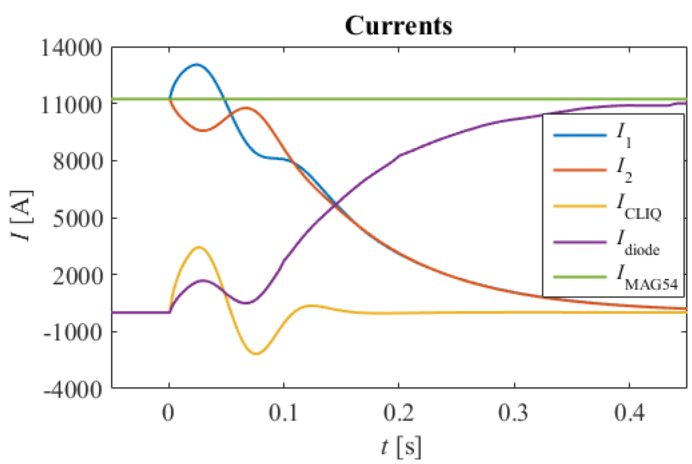
Circuit design

Number of circuits per PS (N)	1	2	3	4	5	6	7	8
Total number of circuits	20	40	60	80	100	120	140	160
Number of magnets per circuit	219	110	73	55	44	37	32	28
Circuit energy [GJ]	8.1	4.1	2.7	2.0	1.6	1.4	1.2	1.0
t_{ramp} = 20 min								
PC max voltage [V]	+100%							
PC peak power [MW]	-46%							
V_{gnd} = 1.3 kV								
Time to 37% of nominal current [s]	-37%							
MIITs [MA^2*s]	-33%							
Busbar cross-section (ΔT=300K) [mm^2]	-21%							

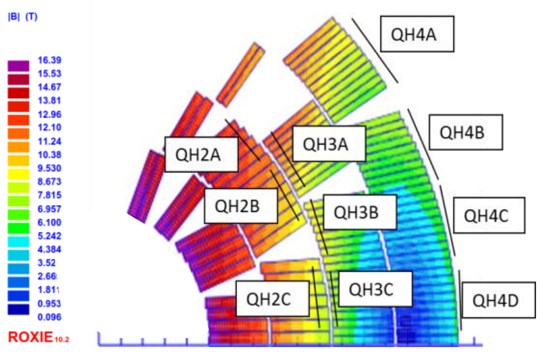
9. Avoid spurious triggers of QDS

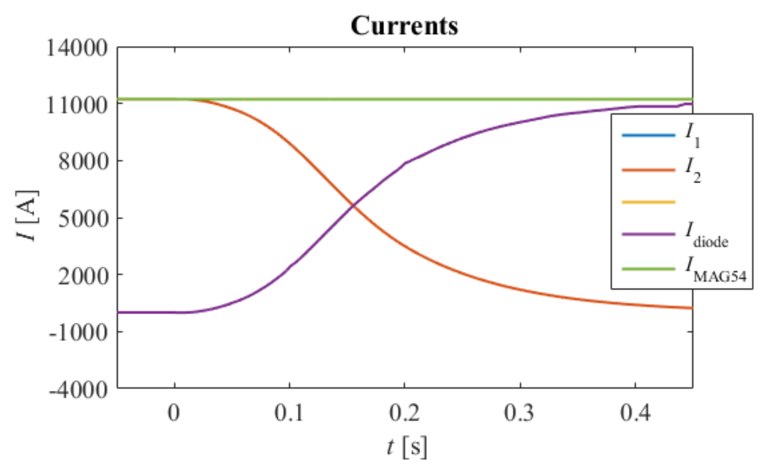
CLIQ protection





QH protection: delays from CoHDA (T. Salmi)

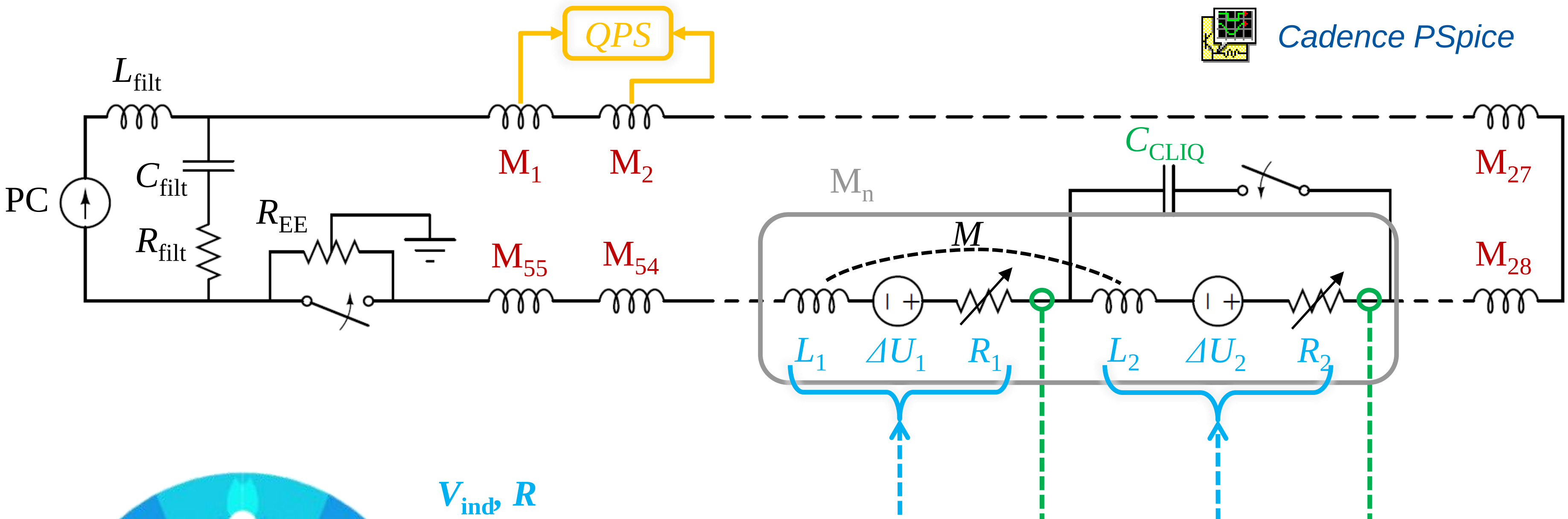


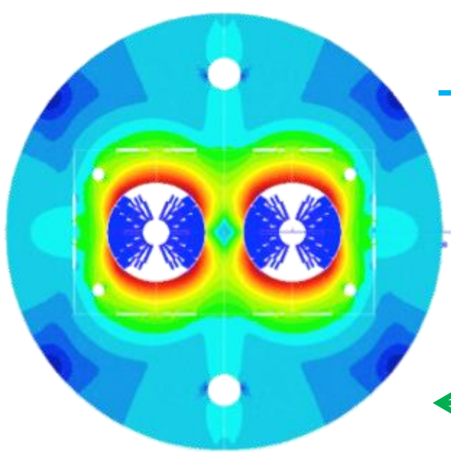


Magnet + circuit co-simulation

Circuit model
2800 components

Cadence PSpice



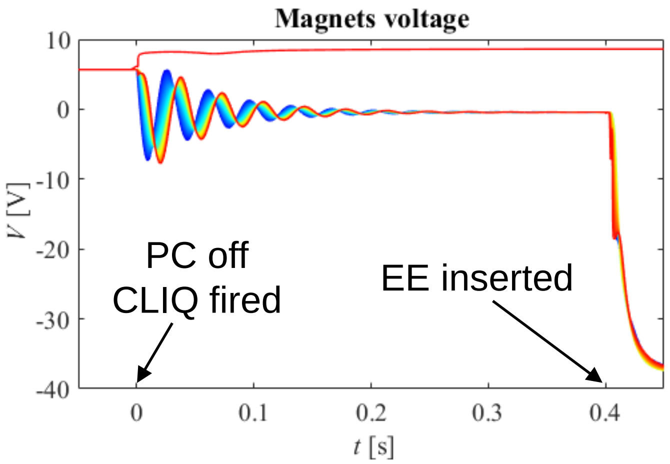


Electro-thermal magnet model
400 turns

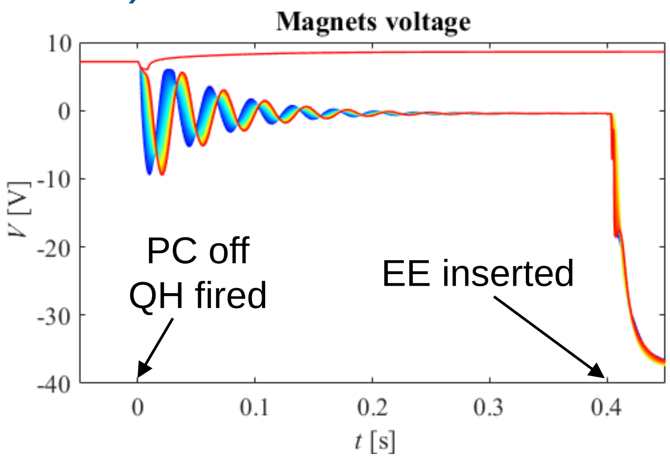
LEDET

9. Avoid spurious triggers of QDS

CLIQ protection



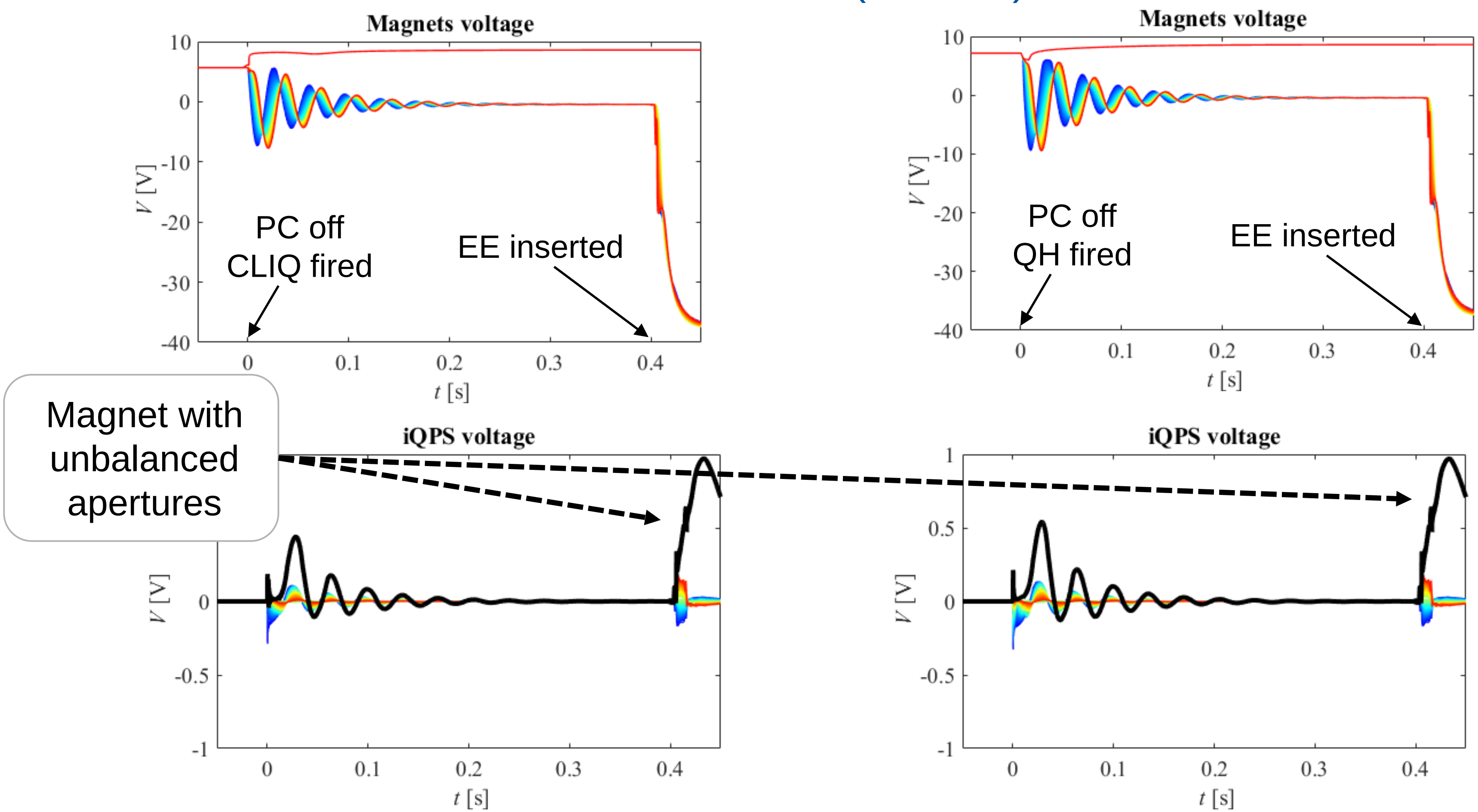
QH protection: delays from CoHDA (T. Salmi)



9. Avoid spurious triggers of QDS

CLIQ protection

QH protection: delays from CoHDA (T. Salmi)



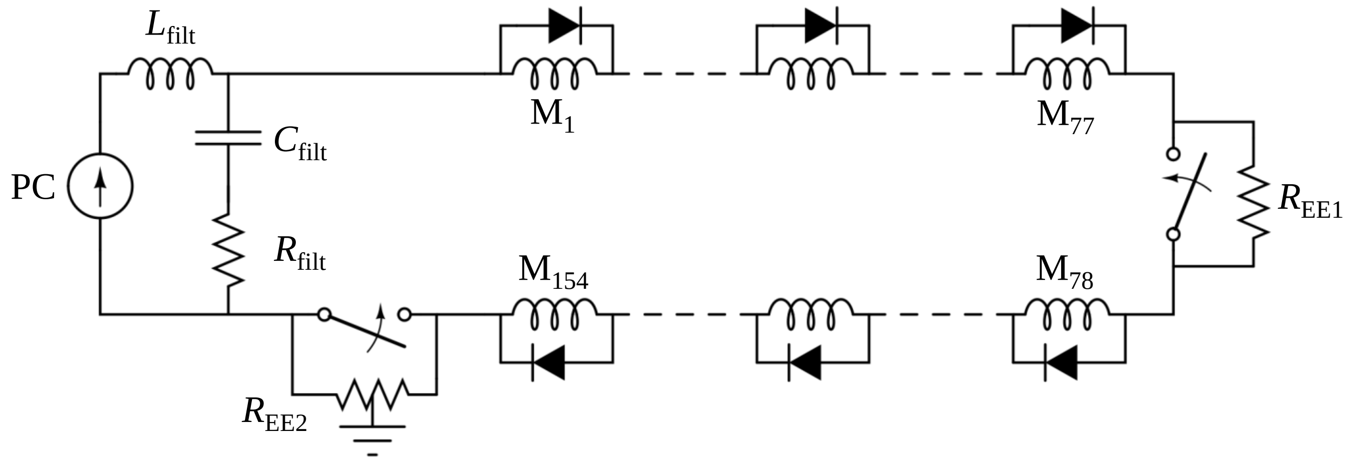
Conclusion

- The subdivision of a 4km sector in multiple circuits is required from the protection point of view
  - 5 to 6 circuits per sector are needed
  - 100 to 120 circuits, power converters, energy extractors, …, for full accelerator
- Different strategies are possible to optimize ramp-up and EE
  - Less circuits per sector (3 to 4)
  - No impact on the circuit design strategy
- CLIQ and QH protection systems have the same effect on QDS signals
  - CLIQ can be operated in a long chain of magnets
- Transient effects are significant for the FCC circuits due to high voltages
  - Further studies are needed to reduce the impact on QDS

CERN

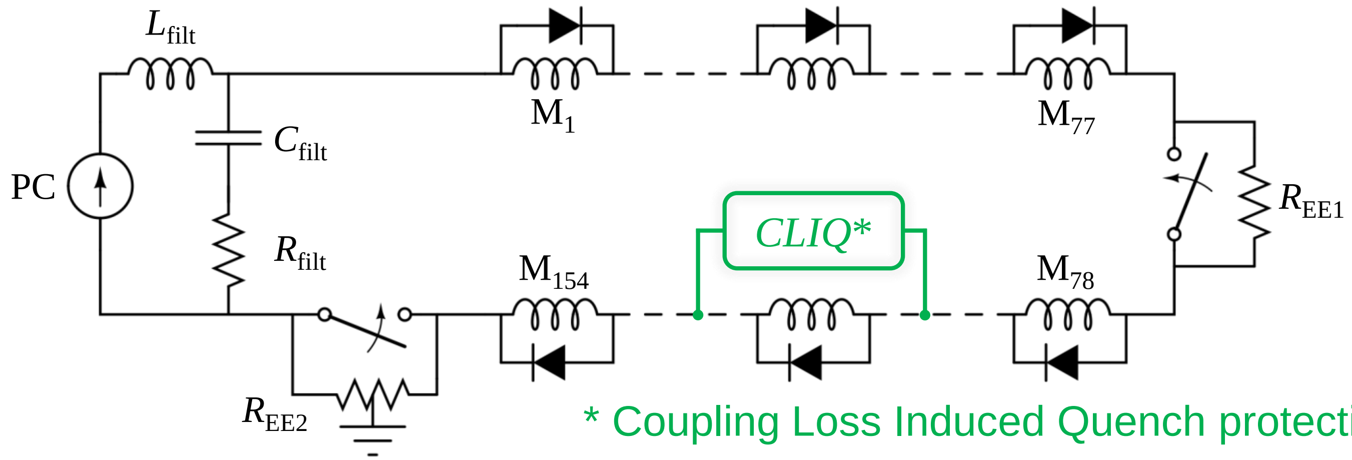
STEAM from the circuit point of view

1. Simulation conventions: SPICE solvers, netlist format, modular libraries
2. Extended modelling capabilities to fit actual needs



STEAM from the circuit point of view

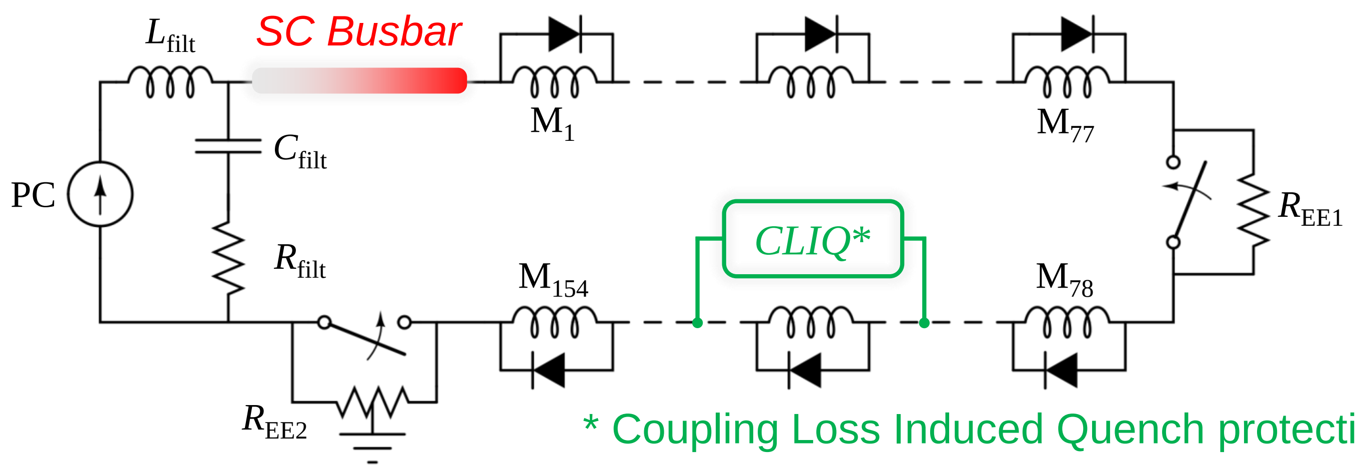
1. Simulation conventions: SPICE solvers, netlist format, modular libraries
2. Extended modelling capabilities to fit actual needs



* Coupling Loss Induced Quench protection system

STEAM from the circuit point of view

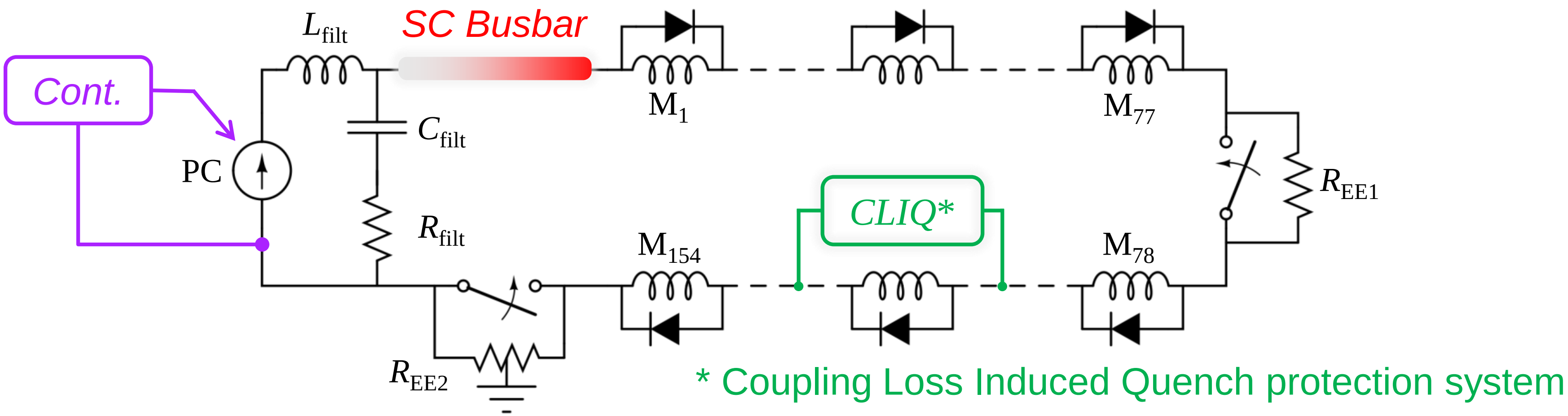
1. Simulation conventions: SPICE solvers, netlist format, modular libraries
2. Extended modelling capabilities to fit actual needs



* Coupling Loss Induced Quench protection system

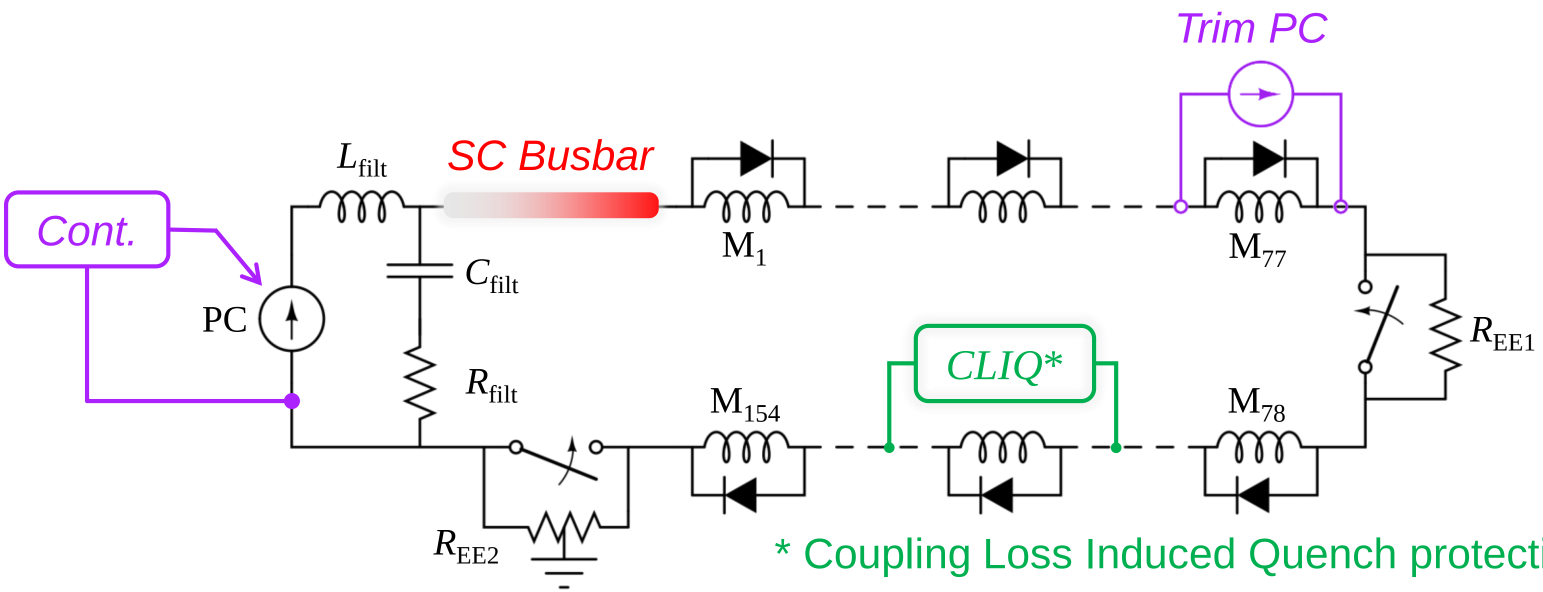
STEAM from the circuit point of view

1. Simulation conventions: SPICE solvers, netlist format, modular libraries
2. Extended modelling capabilities to fit actual needs



STEAM from the circuit point of view

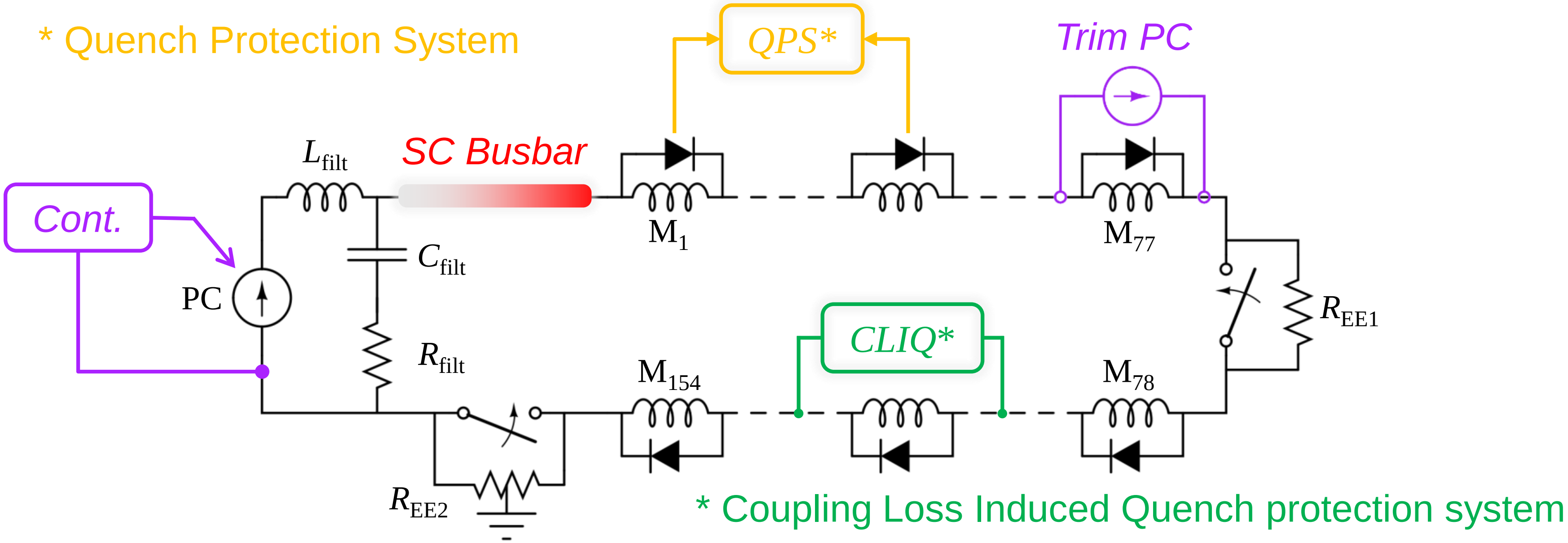
1. Simulation conventions: SPICE solvers, netlist format, modular libraries
2. Extended modelling capabilities to fit actual needs



* Coupling Loss Induced Quench protection system

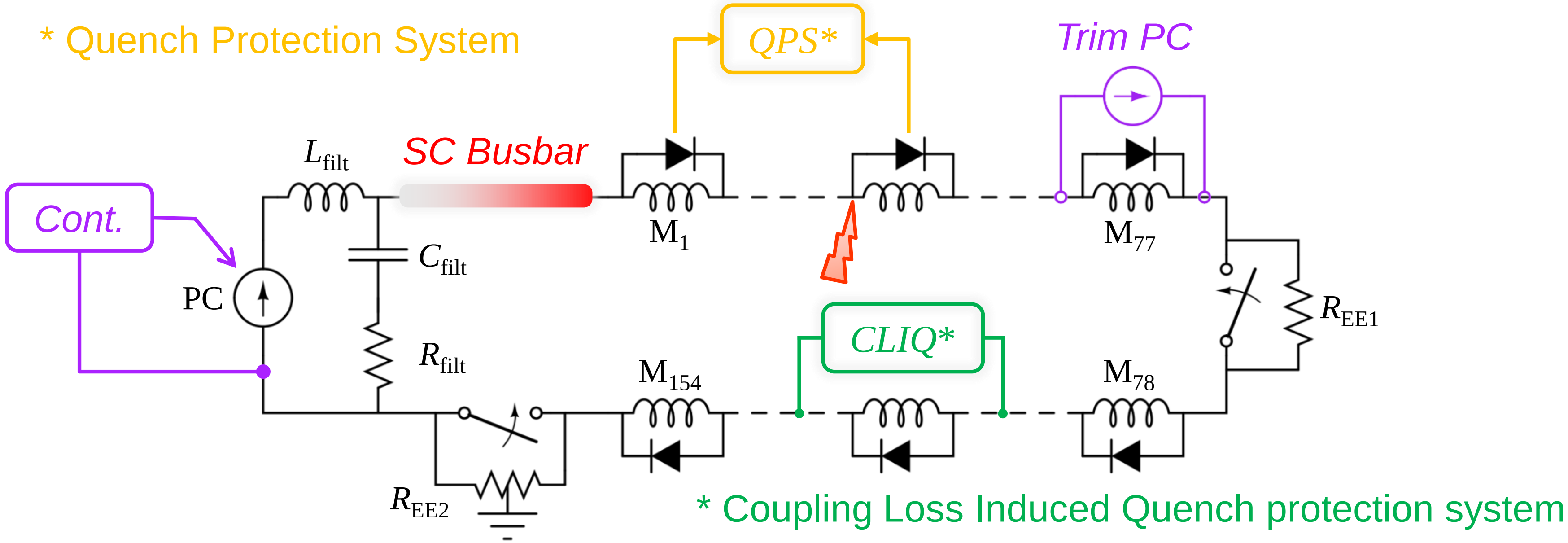
STEAM from the circuit point of view

1. Simulation conventions: SPICE solvers, netlist format, modular libraries
2. Extended modelling capabilities to fit actual needs



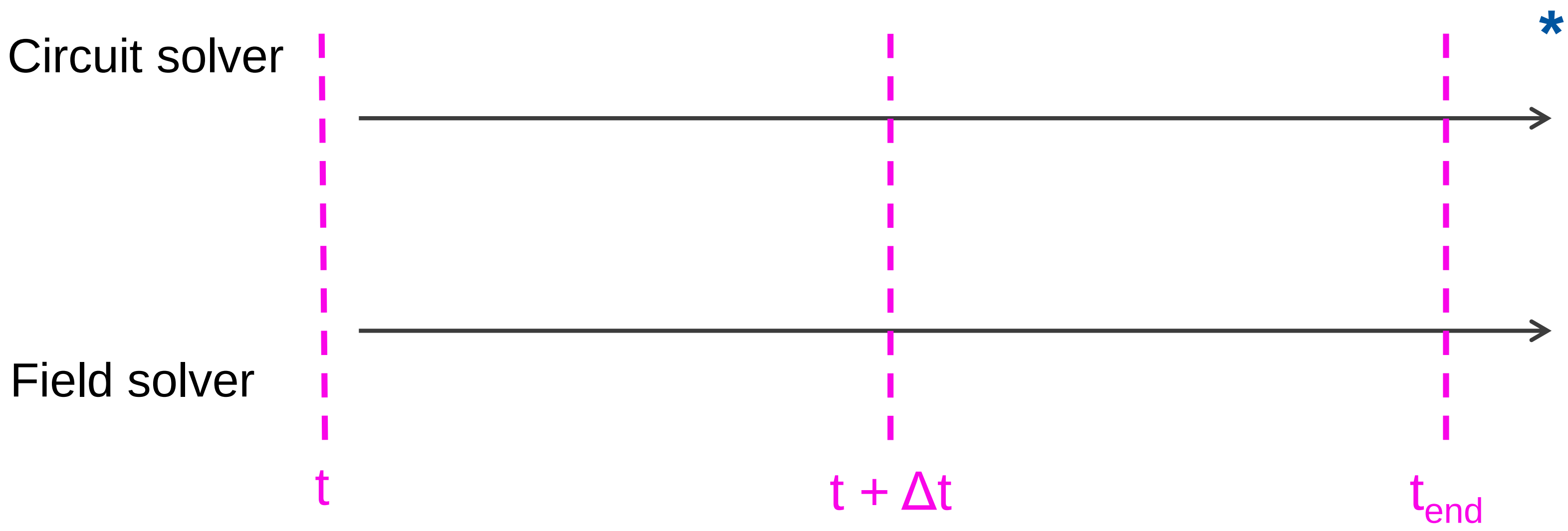
STEAM from the circuit point of view

1. Simulation conventions: SPICE solvers, netlist format, modular libraries
2. Extended modelling capabilities to fit actual needs



Field-circuit coupling

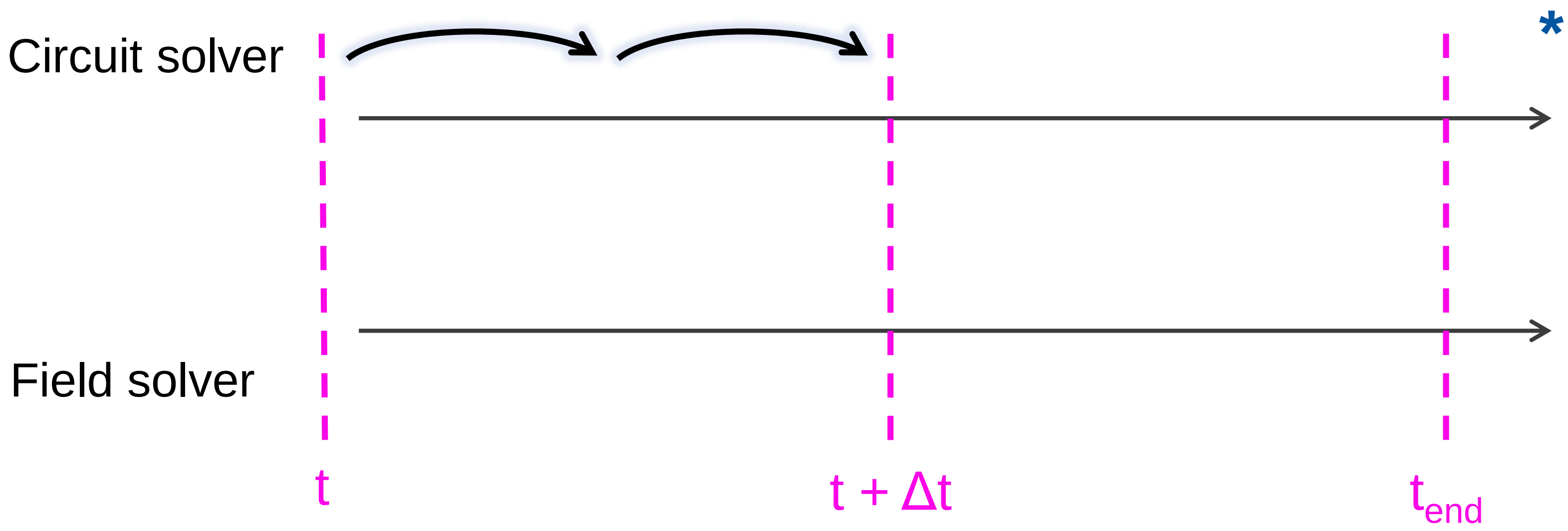
- Coupling scheme: Waveform Relaxation – Gauss-Siedel scheme



- Advantages
  - Multiple solvers with individual adaptive time stepping
  - No assumptions about current decay
  - No assumptions about field and inductance evolution
  - Convergence error under control

Field-circuit coupling

- Coupling scheme: Waveform Relaxation – Gauss-Siedel scheme

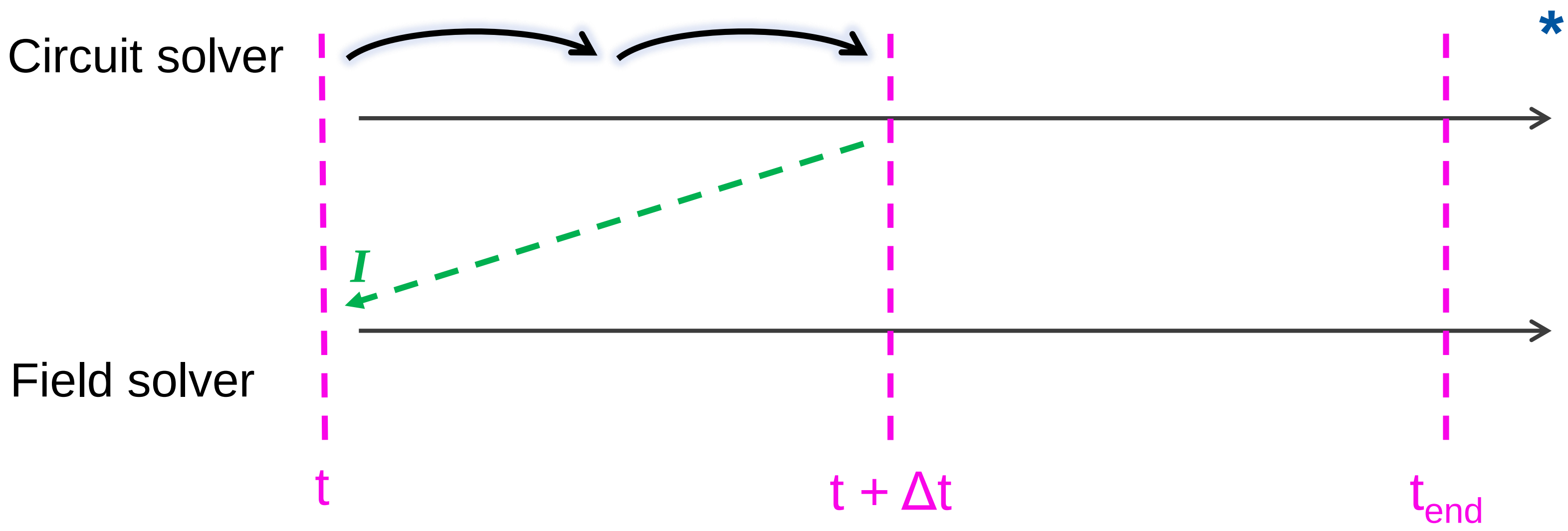


- Advantages
  - Multiple solvers with individual adaptive time stepping
  - No assumptions about current decay
  - No assumptions about field and inductance evolution
  - Convergence error under control

* Courtesy of M. Maciejewski

Field-circuit coupling

- Coupling scheme: Waveform Relaxation – Gauss-Siedel scheme

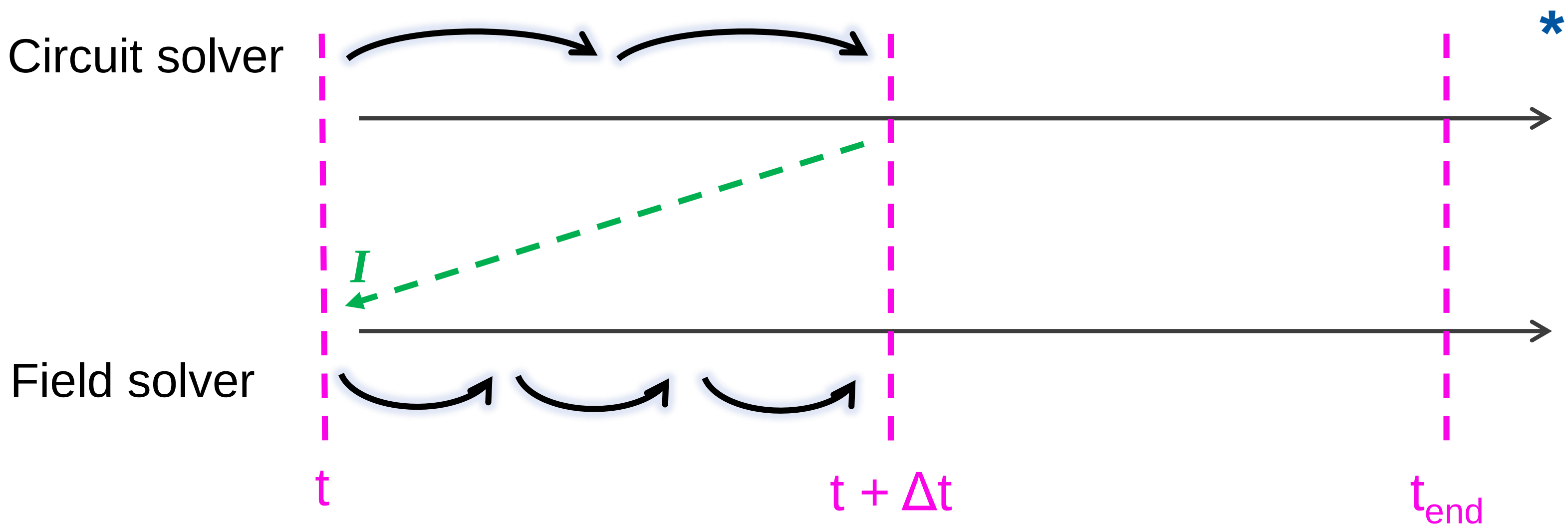


- Advantages
  - Multiple solvers with individual adaptive time stepping
  - No assumptions about current decay
  - No assumptions about field and inductance evolution
  - Convergence error under control

* Courtesy of M. Maciejewski

Field-circuit coupling

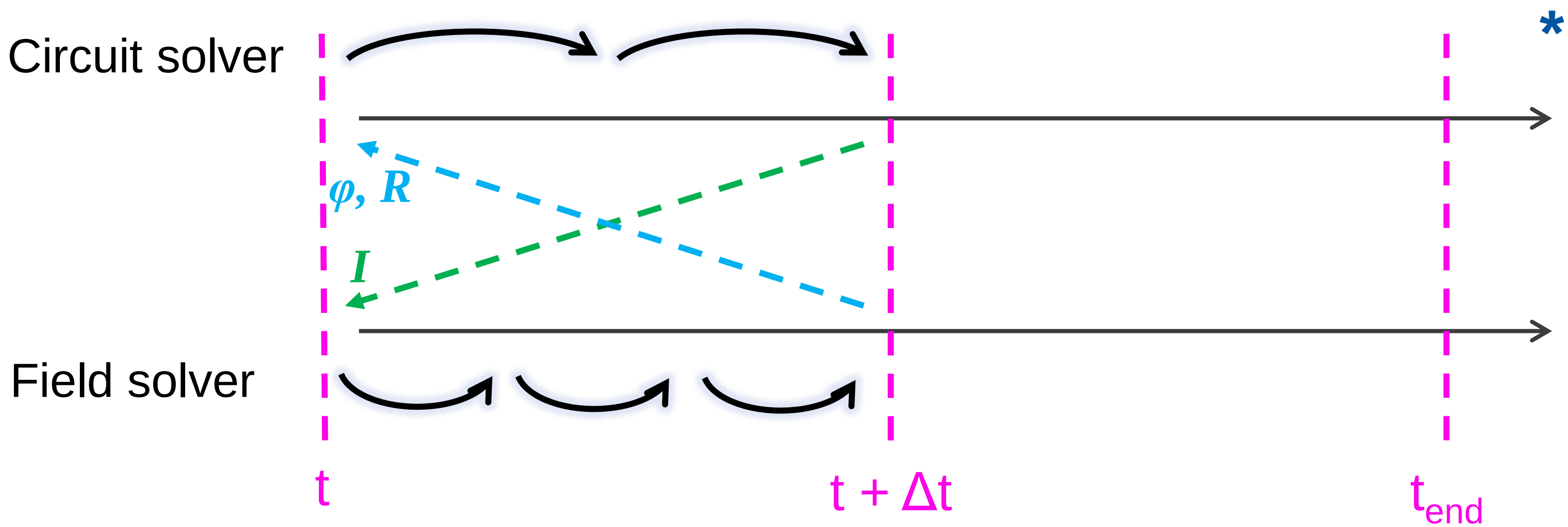
- Coupling scheme: Waveform Relaxation – Gauss-Siedel scheme



- Advantages
  - Multiple solvers with individual adaptive time stepping
  - No assumptions about current decay
  - No assumptions about field and inductance evolution
  - Convergence error under control

Field-circuit coupling

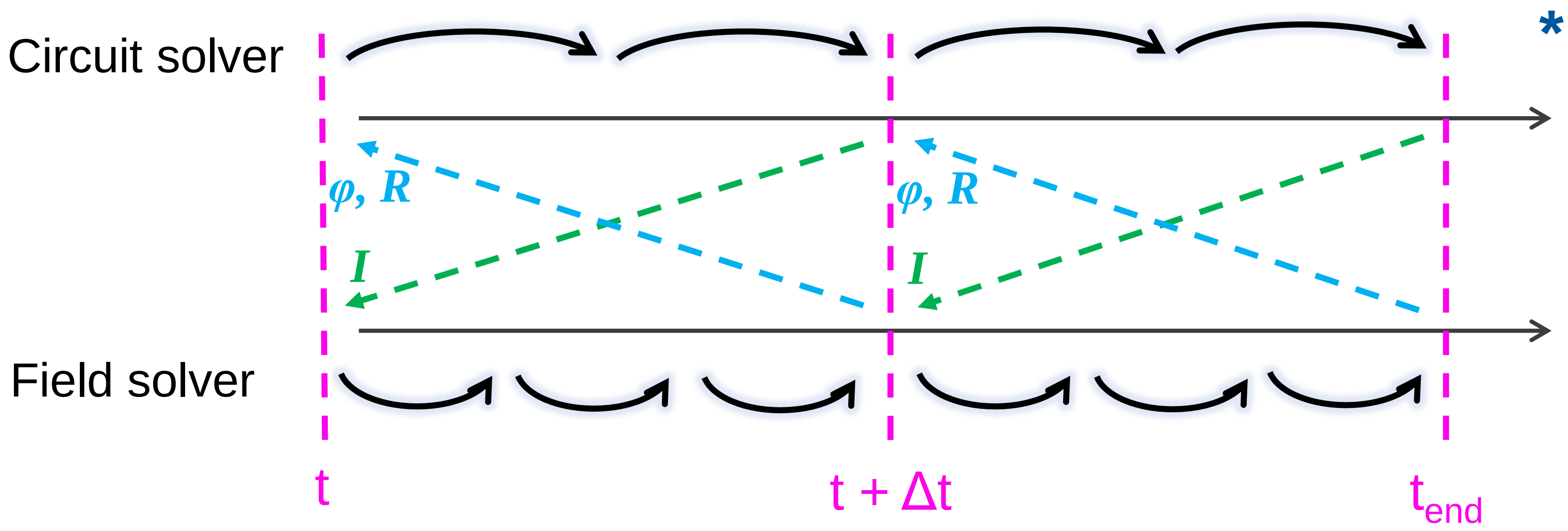
- Coupling scheme: Waveform Relaxation – Gauss-Siedel scheme



- Advantages
  - Multiple solvers with individual adaptive time stepping
  - No assumptions about current decay
  - No assumptions about field and inductance evolution
  - Convergence error under control

Field-circuit coupling

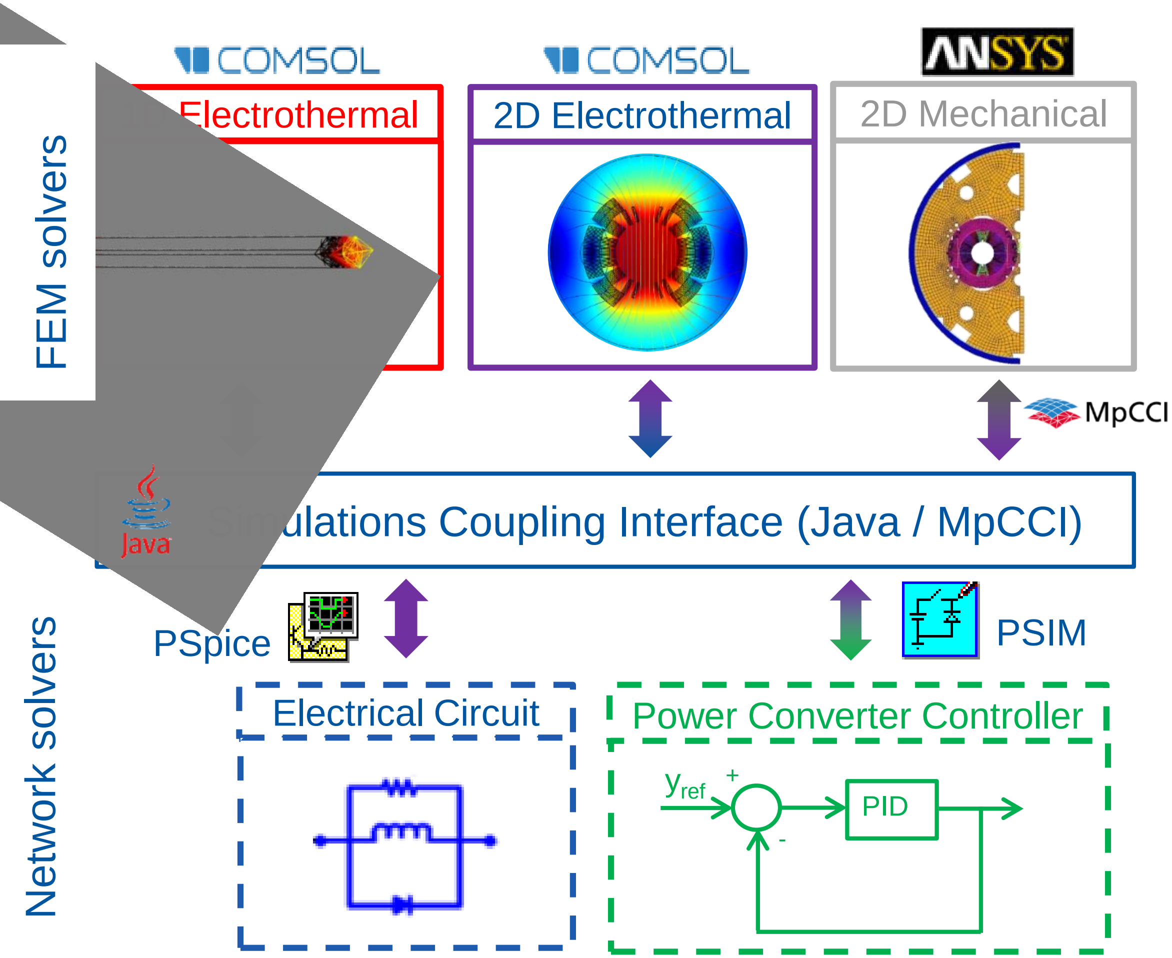
- Coupling scheme: Waveform Relaxation – Gauss-Siedel scheme



- Advantages
  - Multiple solvers with individual adaptive time stepping
  - No assumptions about current decay
  - No assumptions about field and inductance evolution
  - Convergence error under control

* Courtesy of M. Maciejewski

STEAM architecture



Motivation for simulation coupling:

Multi-physics
- Multiple coupled physical domains

Multi-rate
- Time constants ranging from μs to minutes

Multi-scale
- Geometrical dimensions differ by several orders of magnitude μm to km

Lossy inductance model