Study of Frequency Divider PLL

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Outlines:

Working principle of PLL

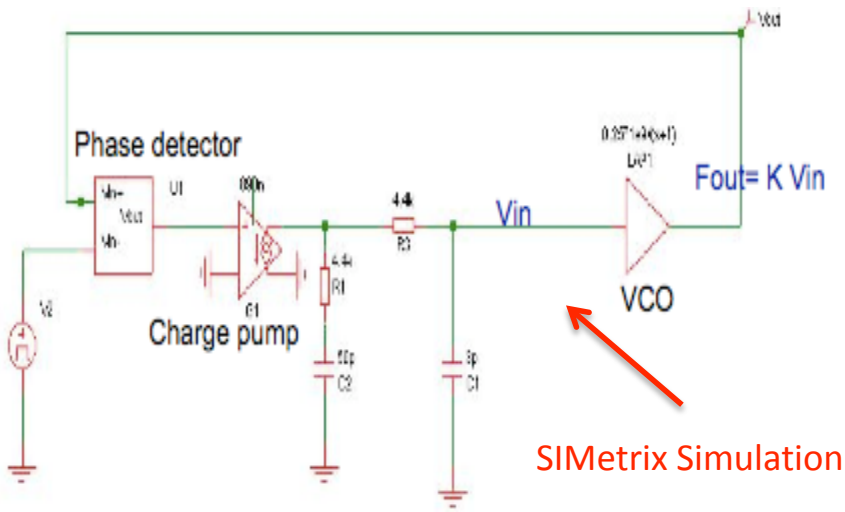
Importance of PLL in ROC

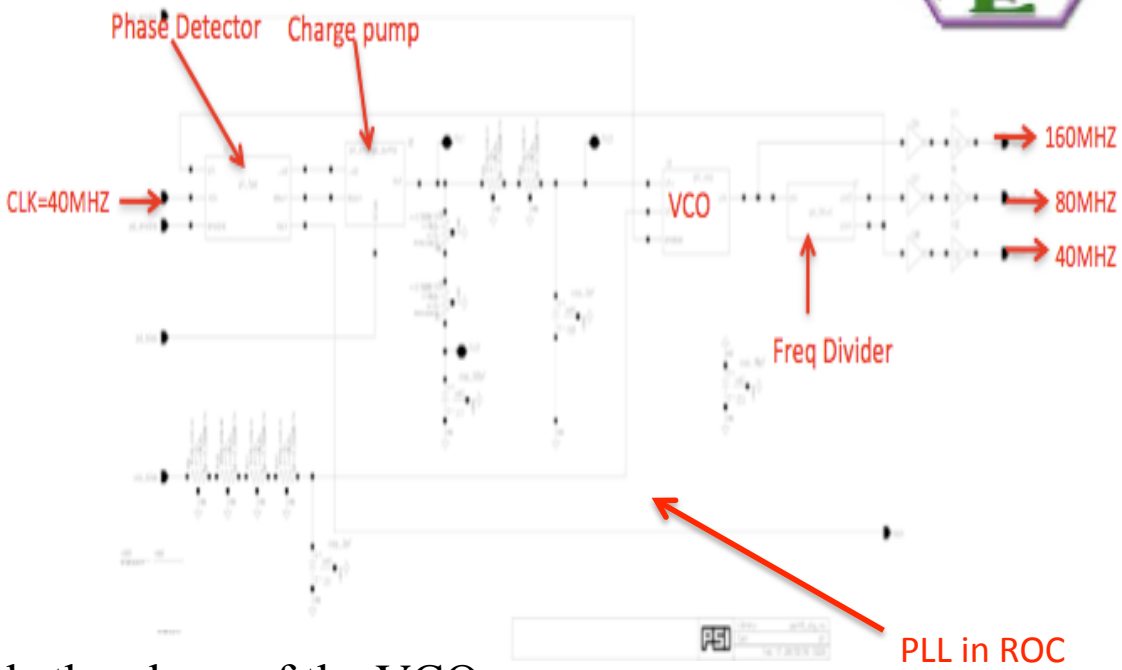
Behavior of PLL at room and low temperature

Simulation Results of ADC

Working Principle of PLL

Circuit for PLL





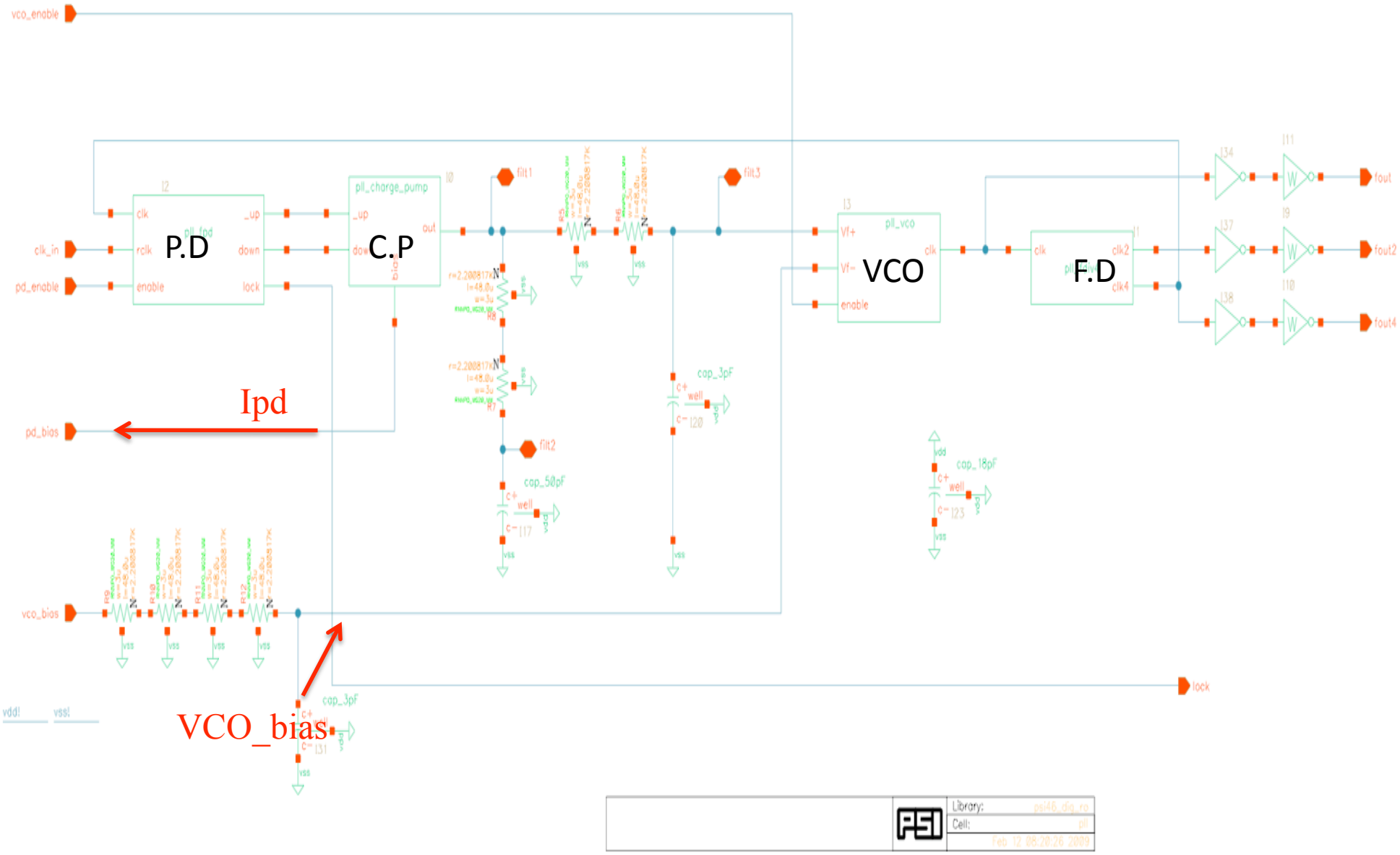
- Feed back Control system that controls the phase of the VCO.

- Input signal applied one input of P.D, the other input is connected to the output of a divide by N counter.

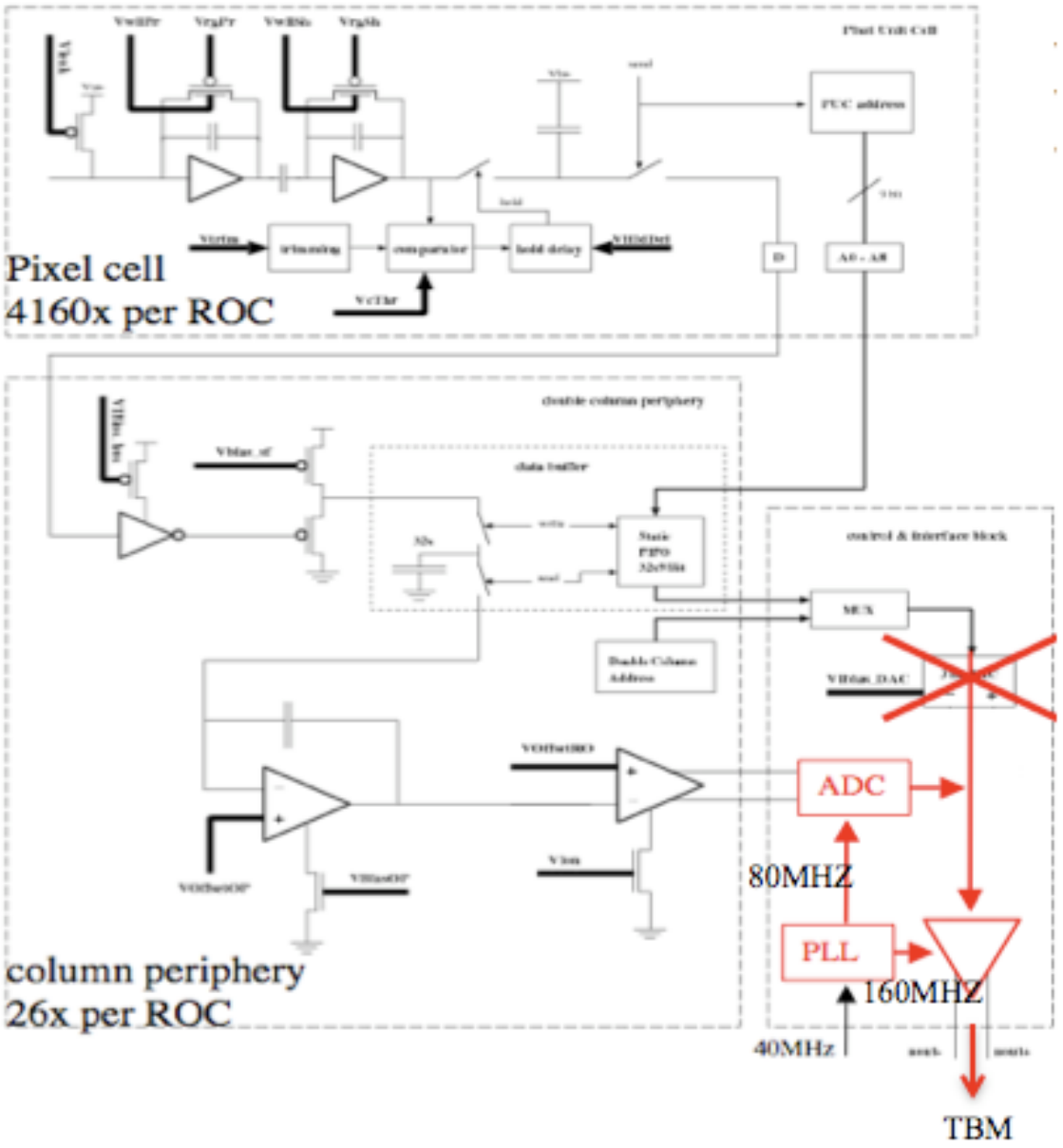
- The Output of the P.D is phase difference between the two inputs.

- This signal is applied to the loop filter with the help of charge pump. The filter signal controls the VCO . (if fvco >fclk, the capacitor to discharges to decrease input voltage to the VCO since fout=K Vin)

Components of PLL

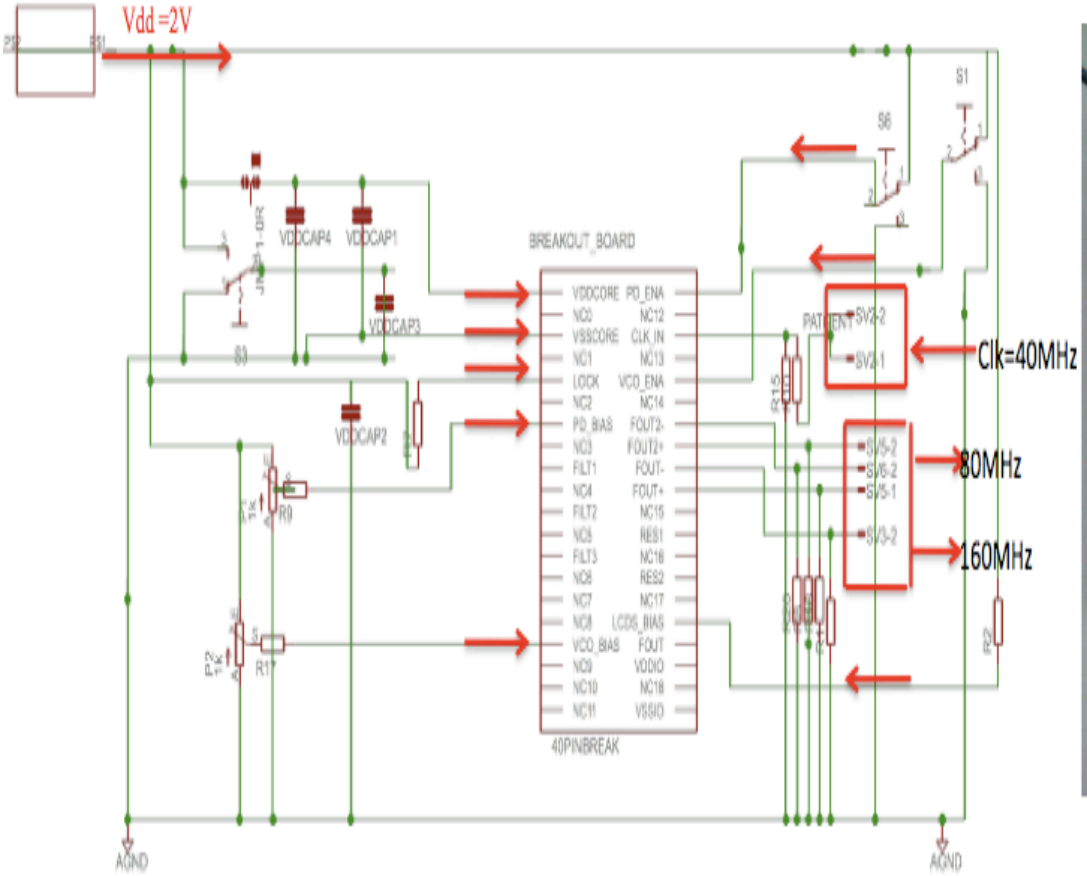


Use of PLL in ROC

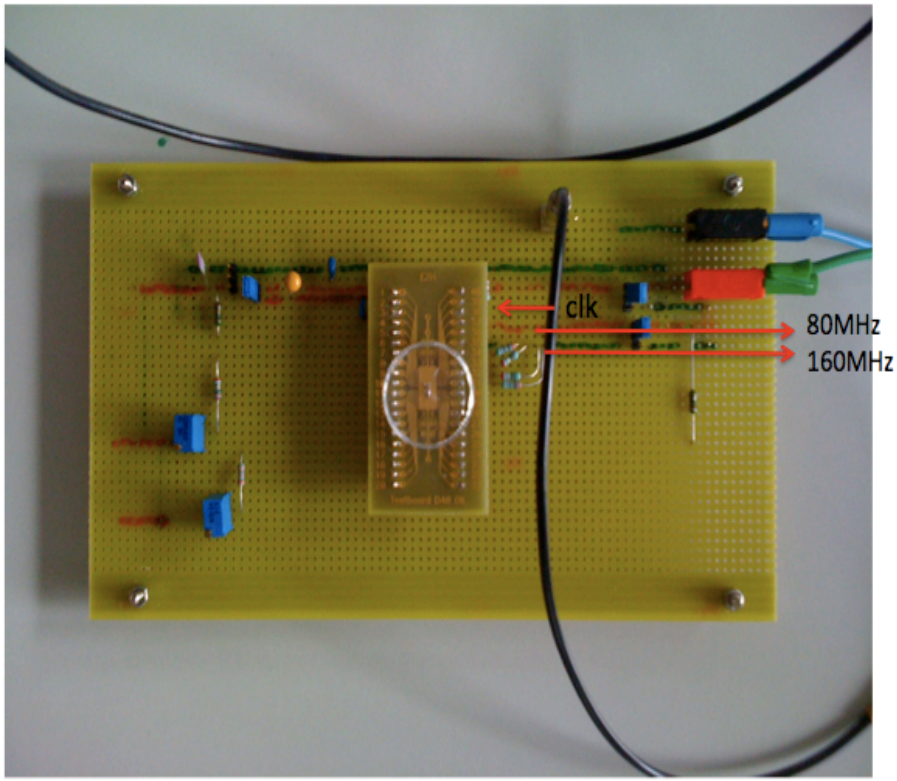


Layout of PLL

Circuit for
Input and Outputs to be taken



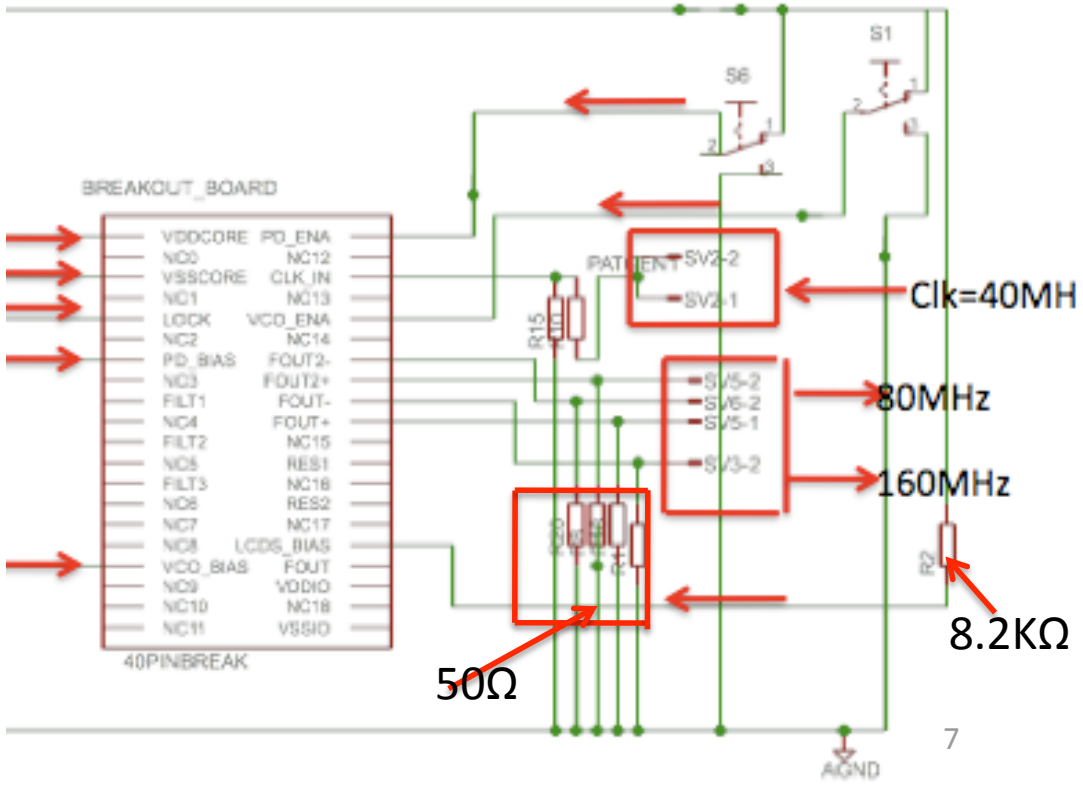
Test Setup for periphery Board



Results from PLL

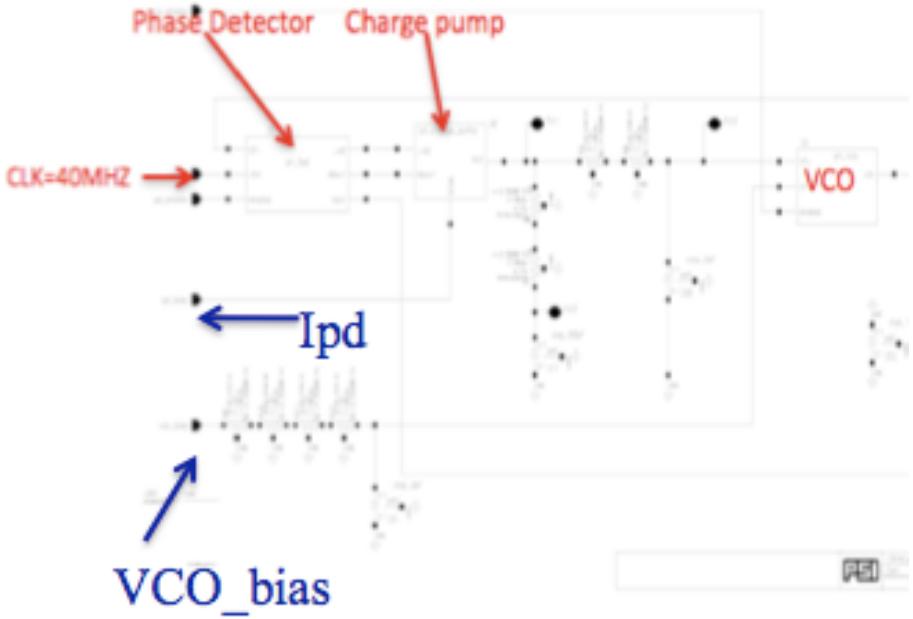
Power Consumption

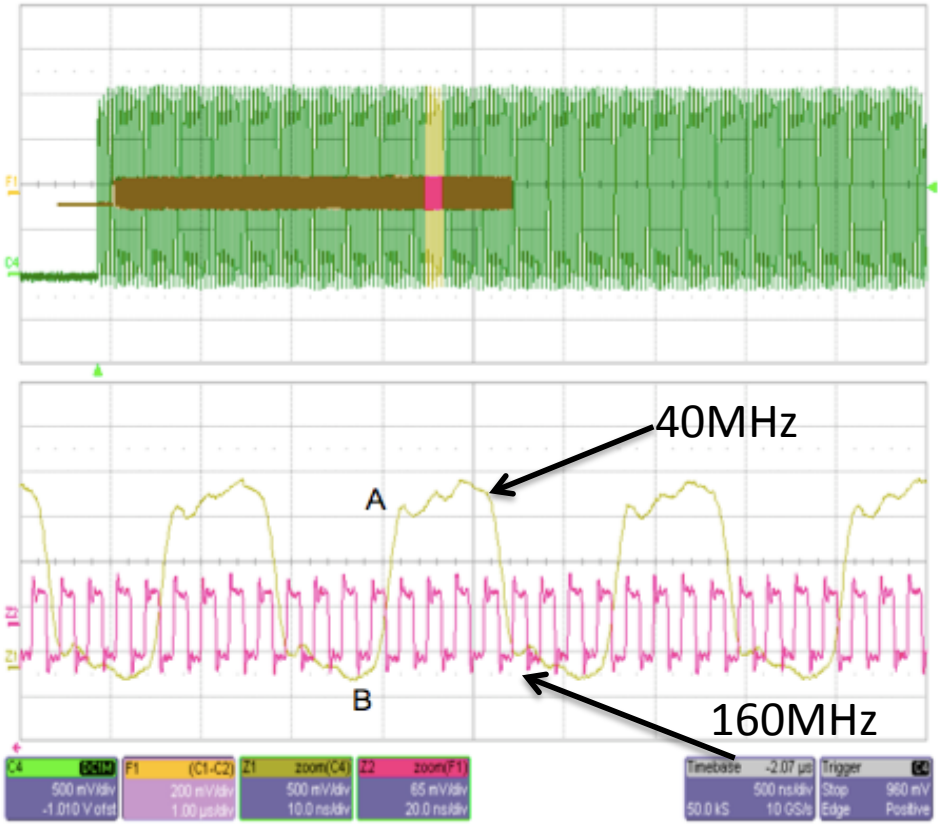
Ref Frequency(40MHZ)	I(mA)	Power Consumption (mW)
Without 50Ω resistances	0.773	1.546
Without 50Ω and 8.2KΩ	0.728	1.456
With all 50Ω and 8.2KΩ	4.783	9.566



Calculation of Locking time PLL

Locking time:



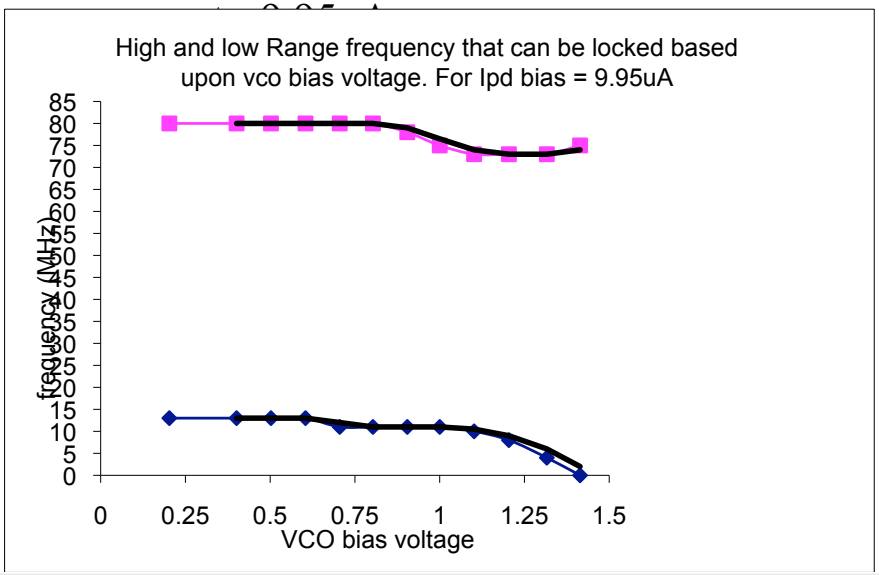


Variation parameters taken for calculating locking time are Ipd and VCO_bias

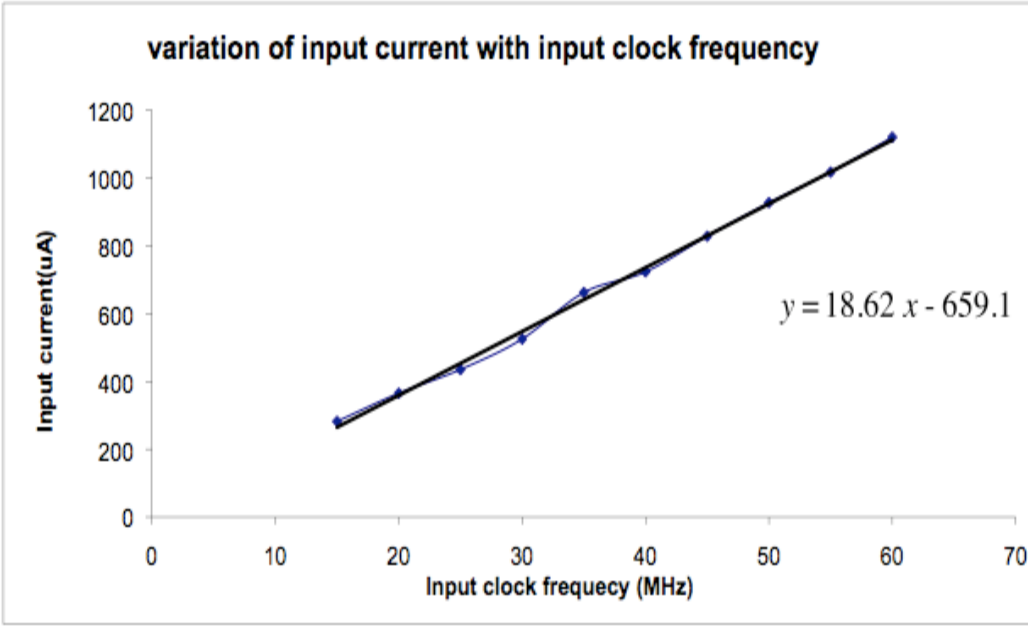
Results from PLL

Locking time

Study of Range of Frequency that can be locked based upon VCO bias voltage for Ipd bias



From 80MHz output, PLL locks from 10MHz - 75MHz Reference Input frequency.



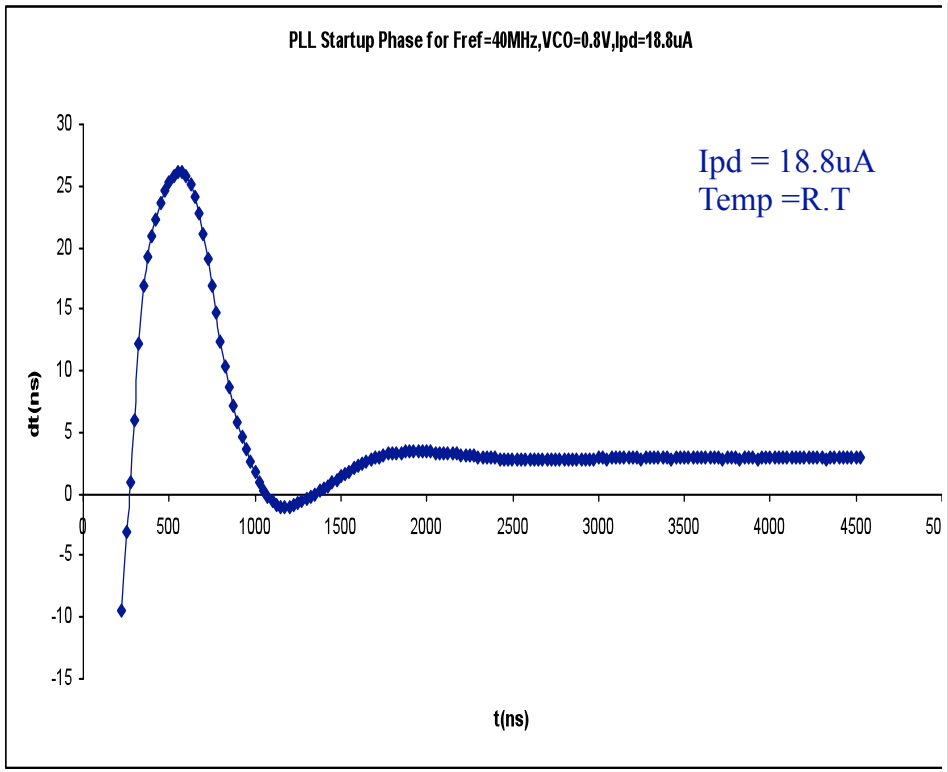
When Fref =0 , I=-659uA
Observed when Fref=0, I=134uA

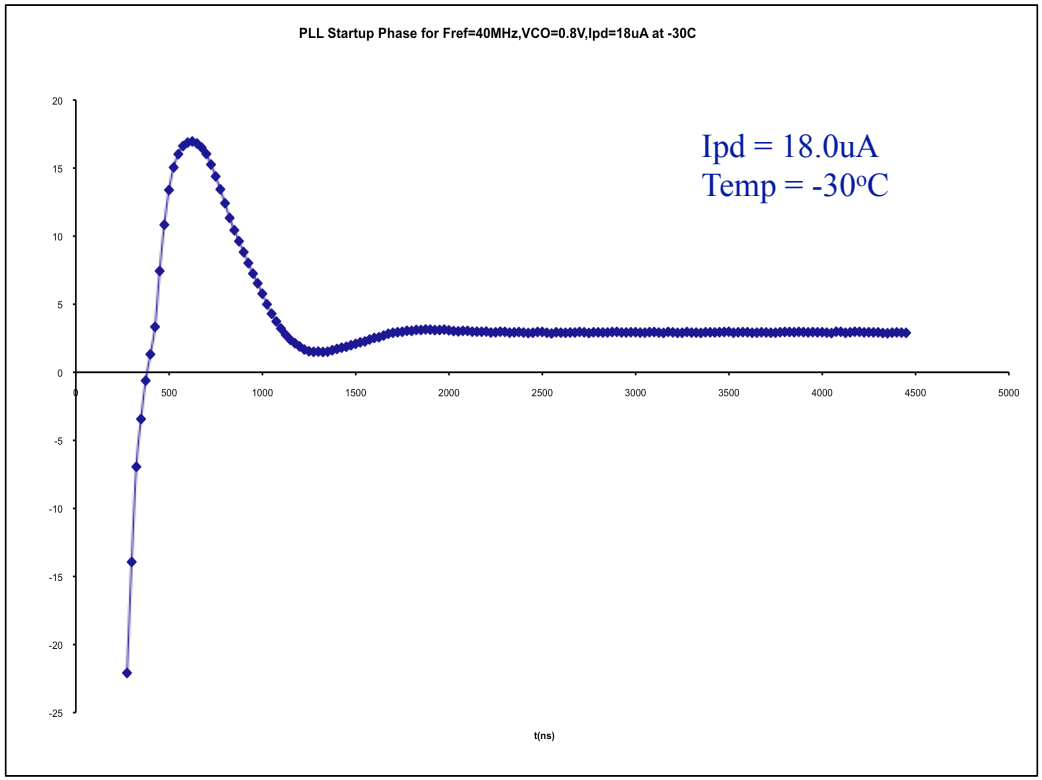
Results from PLL

Locking time:

Standard Fref =40MHz and VCO = 0.8V

Comparison Plots for temperature for different Ipd





1st overshoot 23ns at 600ns
1st undershoot -3.9ns at1100ns
2nd overshoot 0.6ns at 1900ns
Damping = 38
Locking time ~3.5us

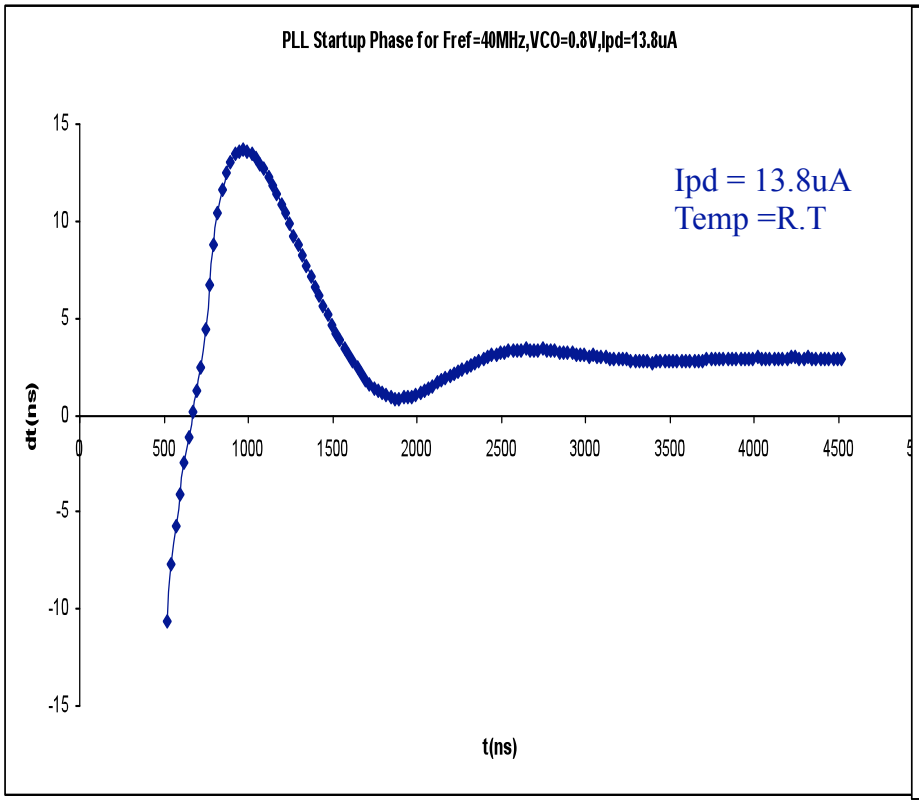
1st overshoot 14ns at 625ns
1st undershoot -1.4ns at 250ns
2nd overshoot 0.1ns at 1800ns
Damping =140
Locking time ~2.5us

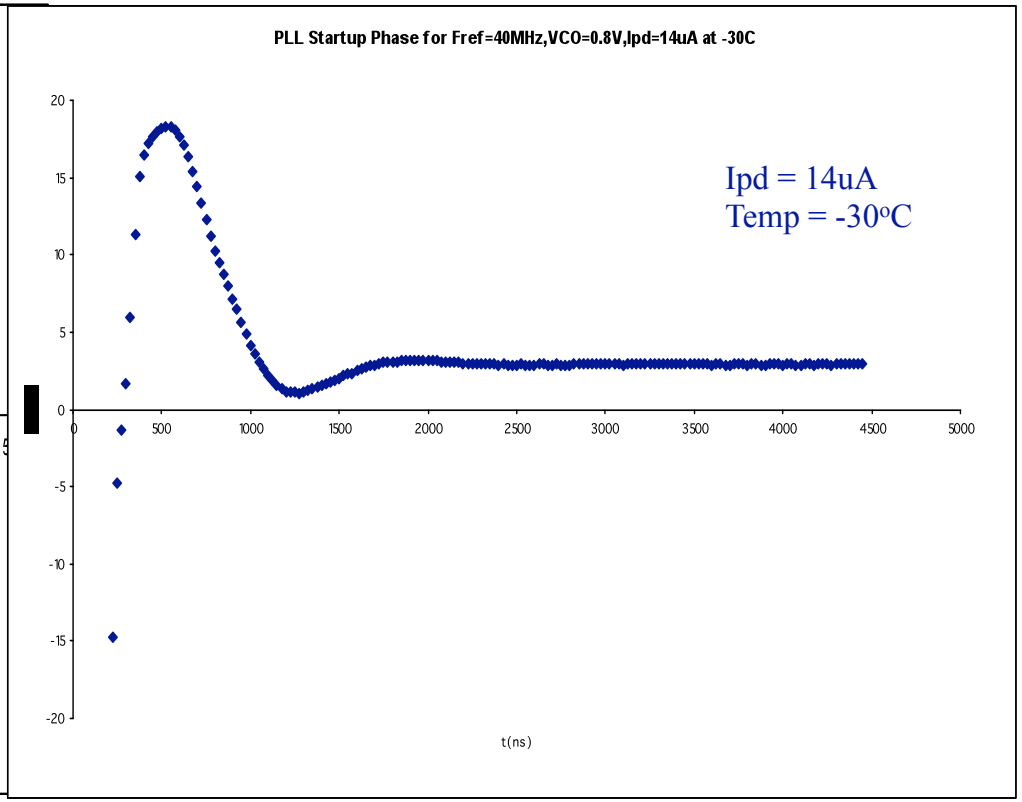
Results from PLL

Locking time:

Standard Fref =40MHz and VCO = 0.8V

Comparison Plots for temperature for different Ipd





1st overshoot 10ns at 945ns
1st undershoot -2.0ns at 1845ns
2nd overshoot 0.4ns at 2600ns
Damping = 25
Locking time ~3.7us

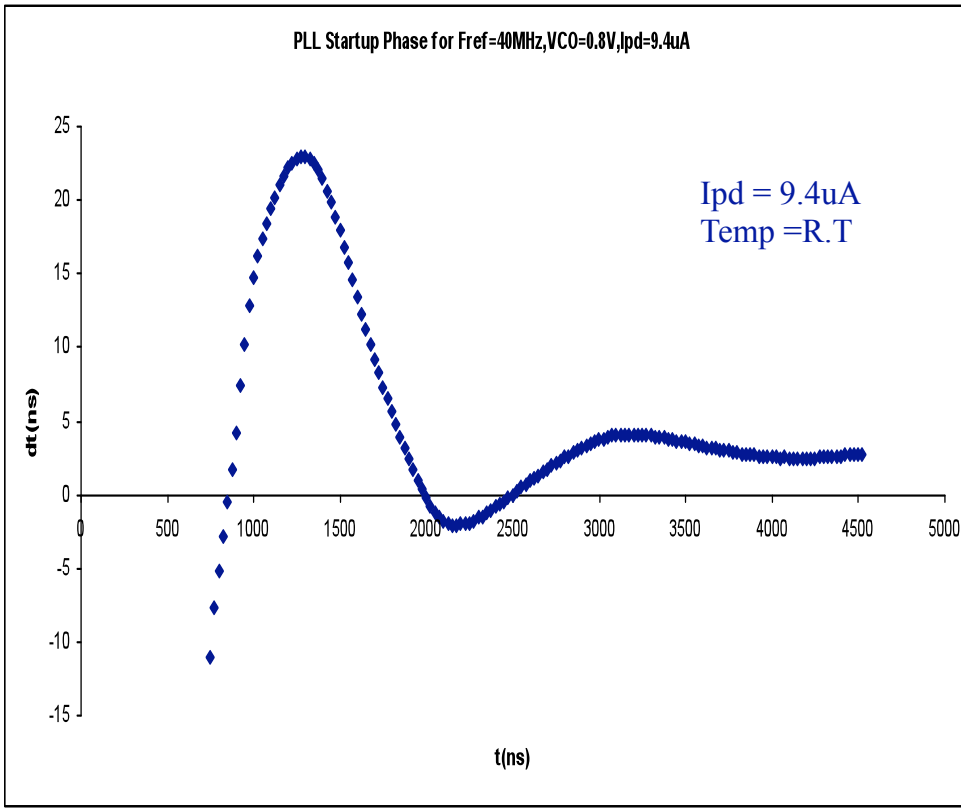
1st overshoot 15.5ns at 542ns
1st undershoot -1.8ns at1200ns
2nd overshoot 0.2ns at 1800ns
Damping = 77.5
Locking time ~ 3.0us

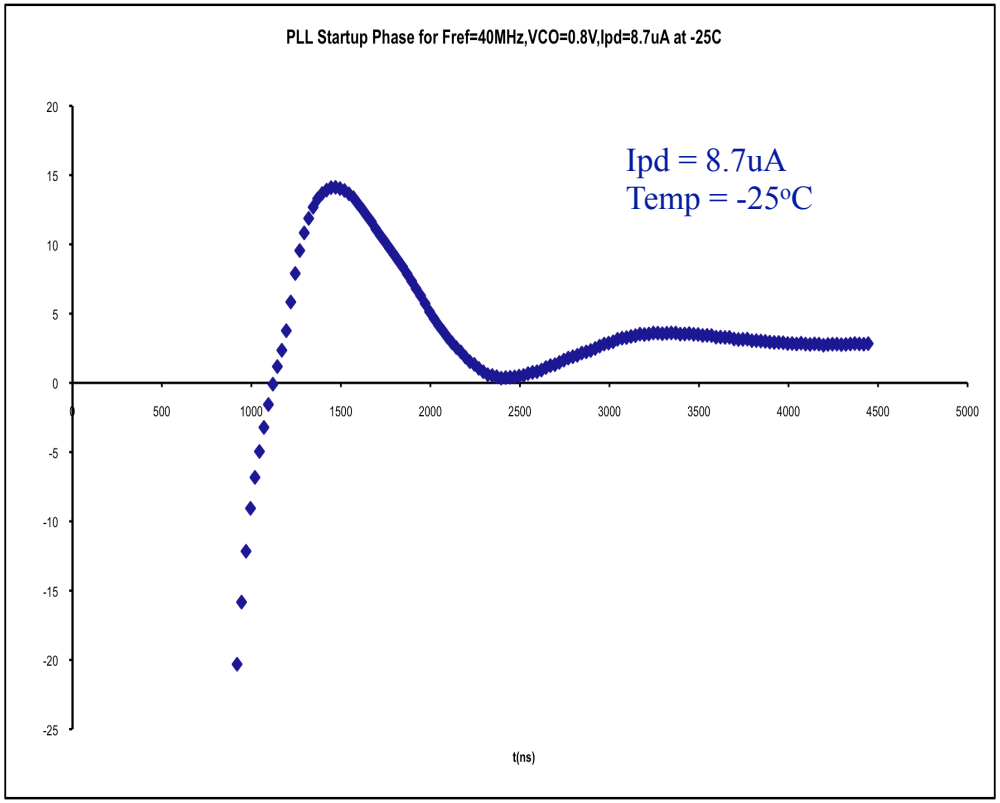
Results from PLL

Locking time:

Standard Fref =40MHz and VCO = 0.8V

Comparison Plots for temperature for different Ipd





1st overshoot 20ns at 1273ns
1st undershoot -4.4ns at 2200ns
2nd overshoot 1.6ns at 3200ns
2nd undershoot 0.1ns at 4200ns
Damping = 12.8
Locking time >4.5us

1st overshoot 11.3ns at 1445ns
1st undershoot -2.4ns at 2420ns
2nd overshoot 0.7ns at 3220ns
Damping = 16
Locking time >4.5us

Results from SIMetrix Simulation

For the study of K parameter for VCO using relation Vout = K.Vin for the test

Using the Simetrix simulation

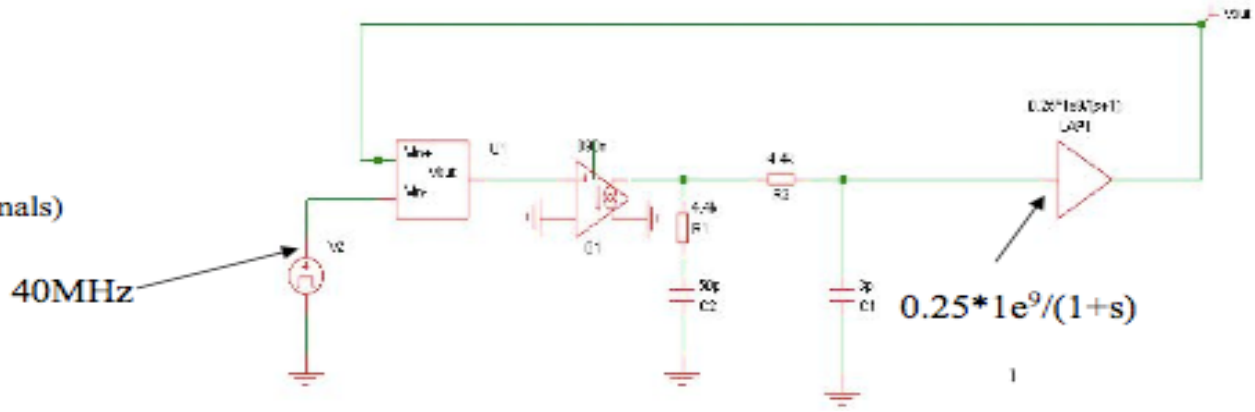
Iref =f(phase difference between two input signals)

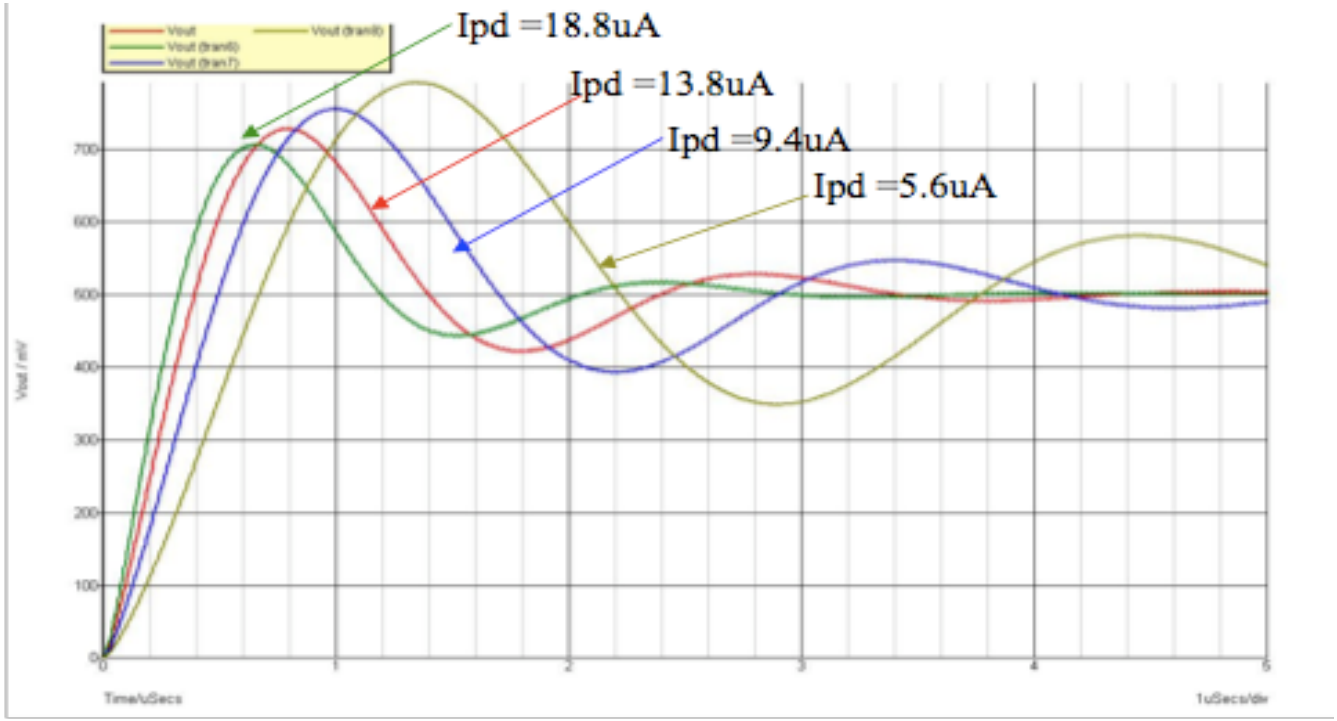
K_{pd} = 0.89 uA/rad for Ipd =5.6uA

K_{pd} = 1.5 uA/rad for Ipd =9.4uA

K_{pd} = 2.2 uA/rad for Ipd =13.8uA

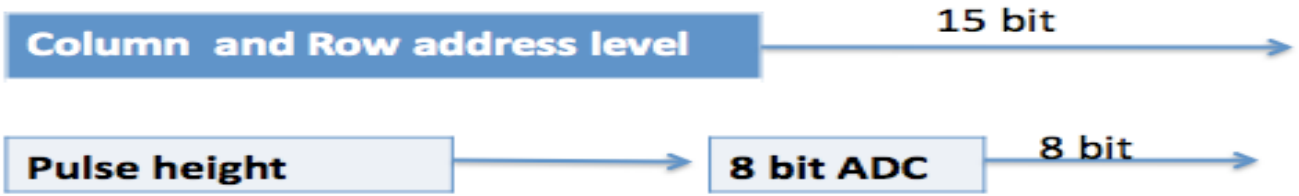
K_{pd} = 3 uA/rad for Ipd =18.8uA





Study of ADC

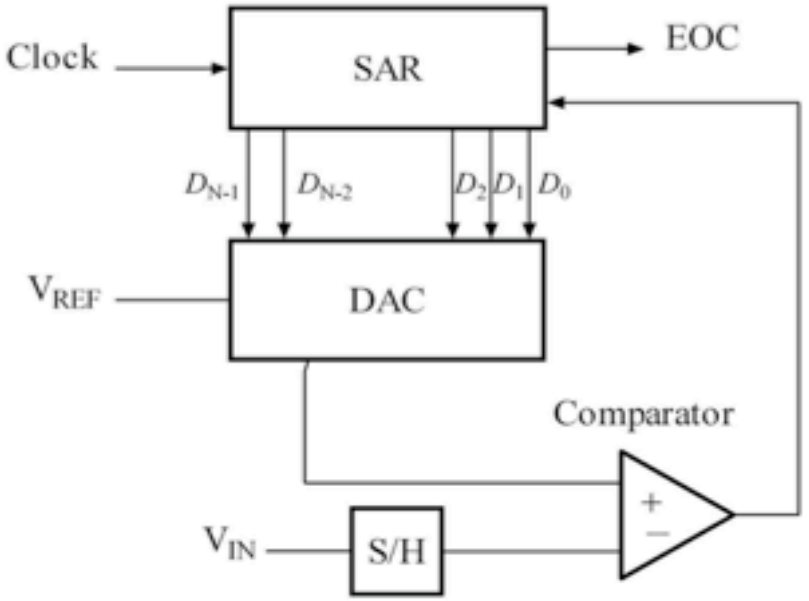
In Upgrade ROC



Working Principle : Successive approximation

SAR initialized so that MSB =1 → DAC which supplies the analog ~ of this digital code ($V_{ref}/2$).

Comparator to compare with V_{in}.

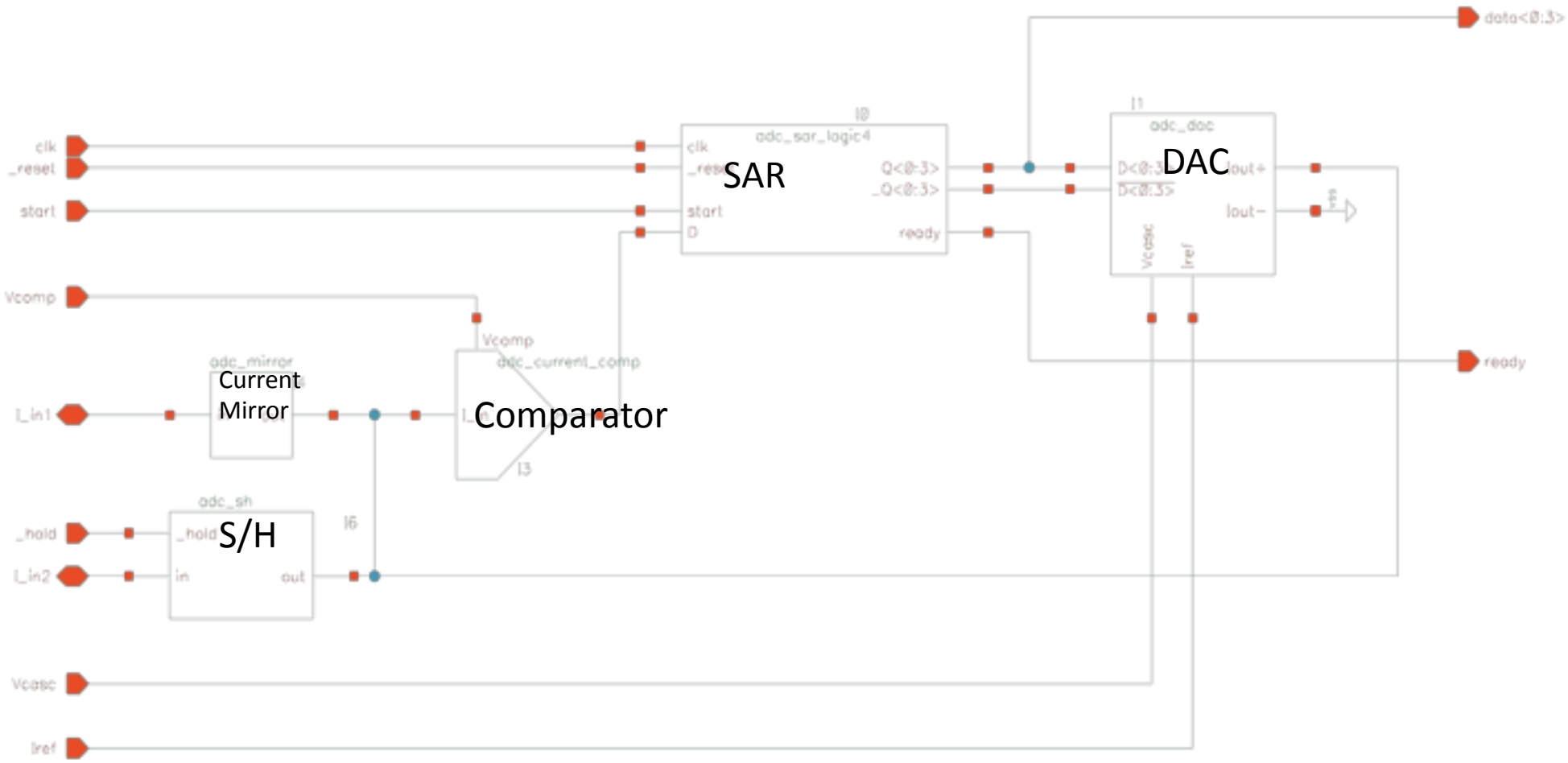


If analog voltage>V_{in} , the comparator leads SAR to reset this bit and set the next bit to a digital 1.

This binary search continues until every bit in SAR is tested. The resulting code is the digital approximation of V_{in} and is finally output by the DAC at EOC.

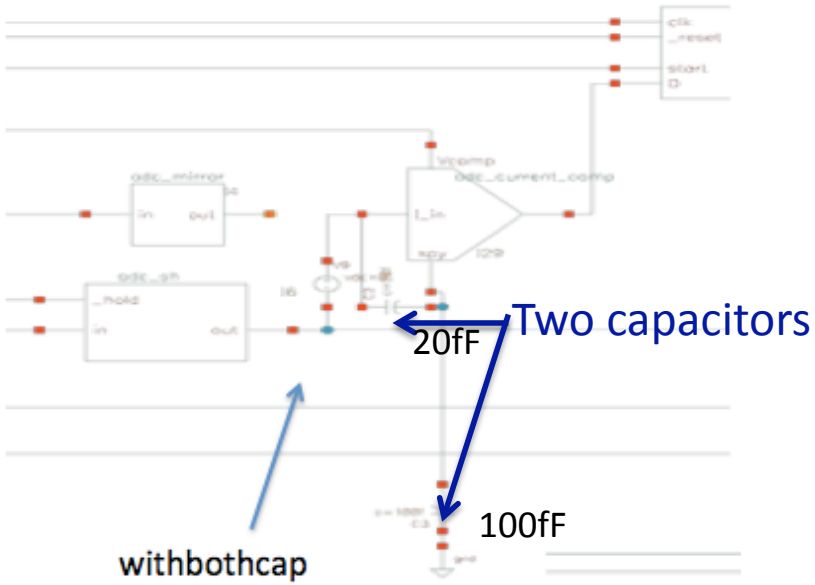
Study of ADC

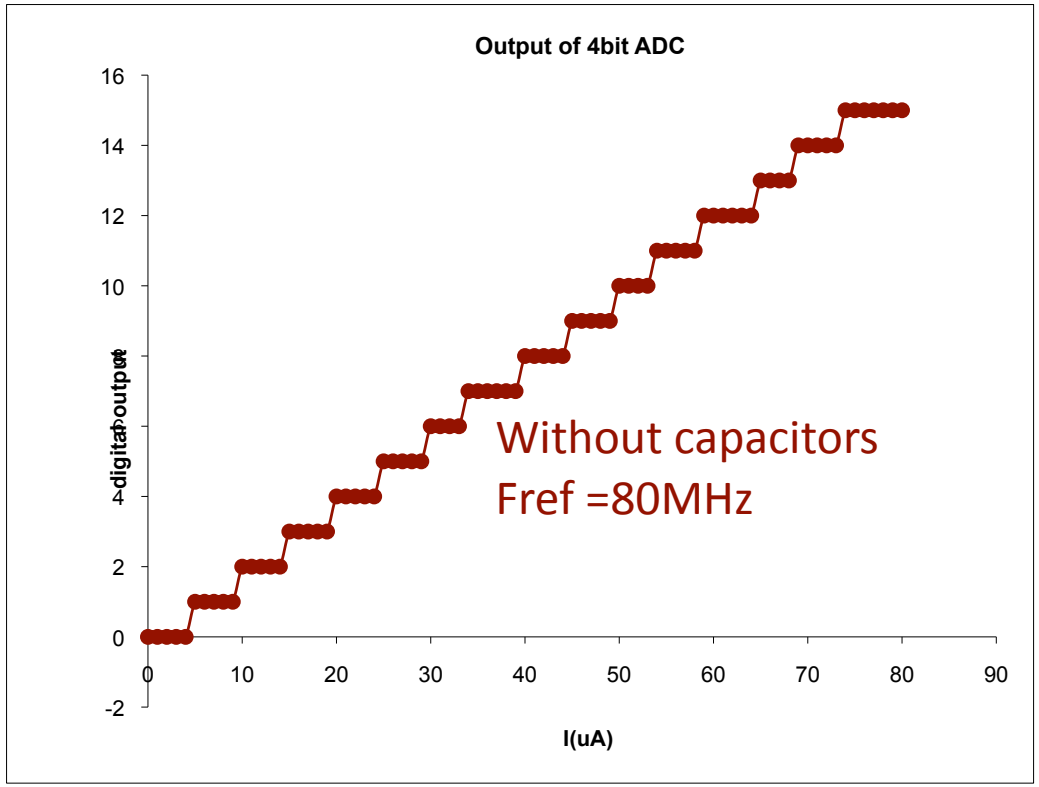
4 bit ADC



Study of ADC

Study of unequal step with testing the 4 bit ADC with the help of Simulation

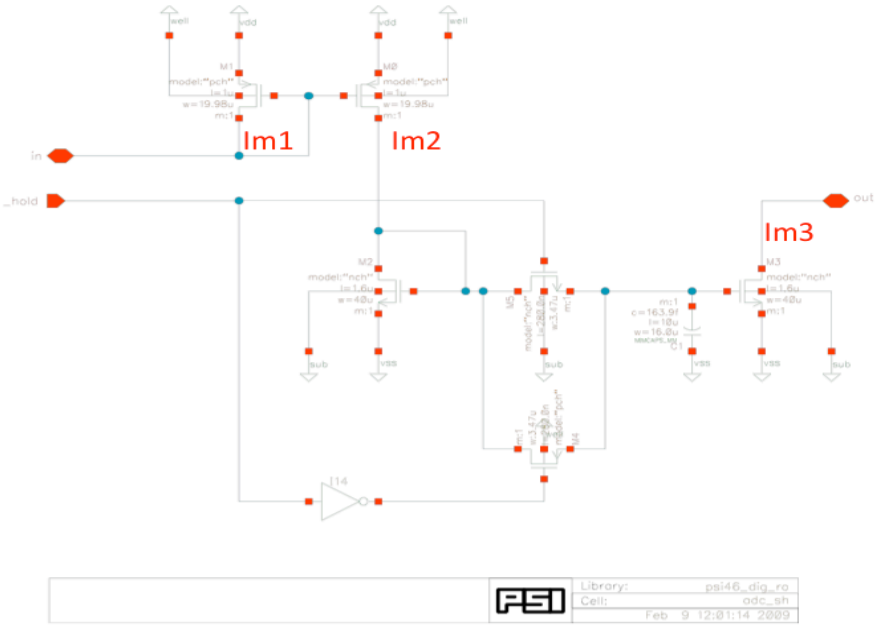


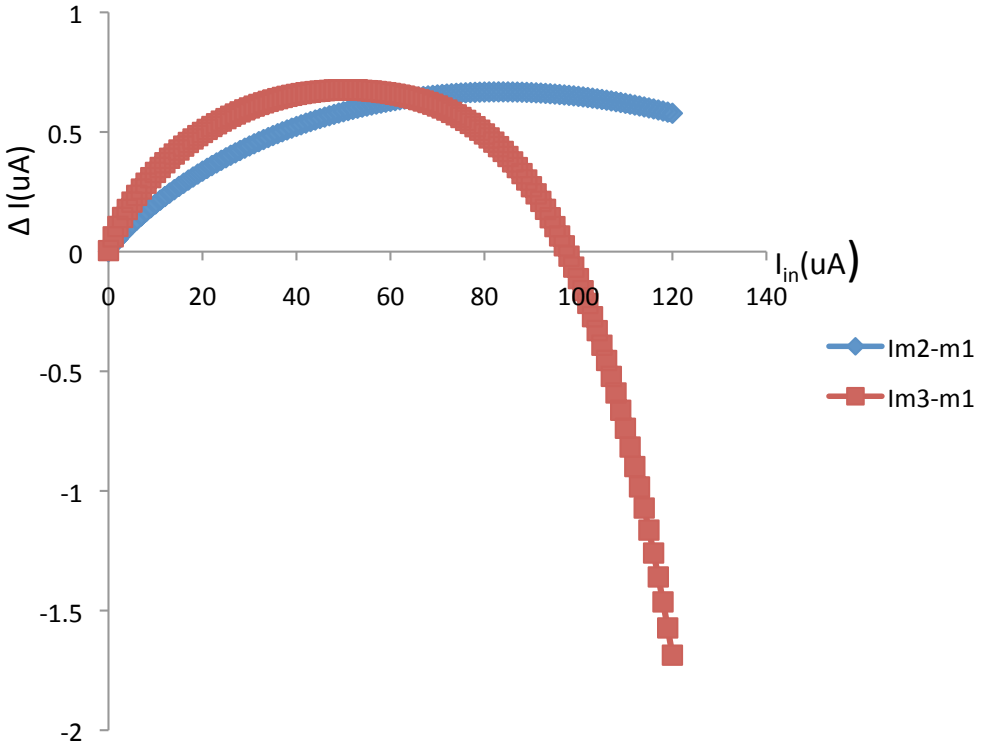


Study of Sample and Hold Circuit

Study of sample and Hold circuit

Sample and Hold circuit





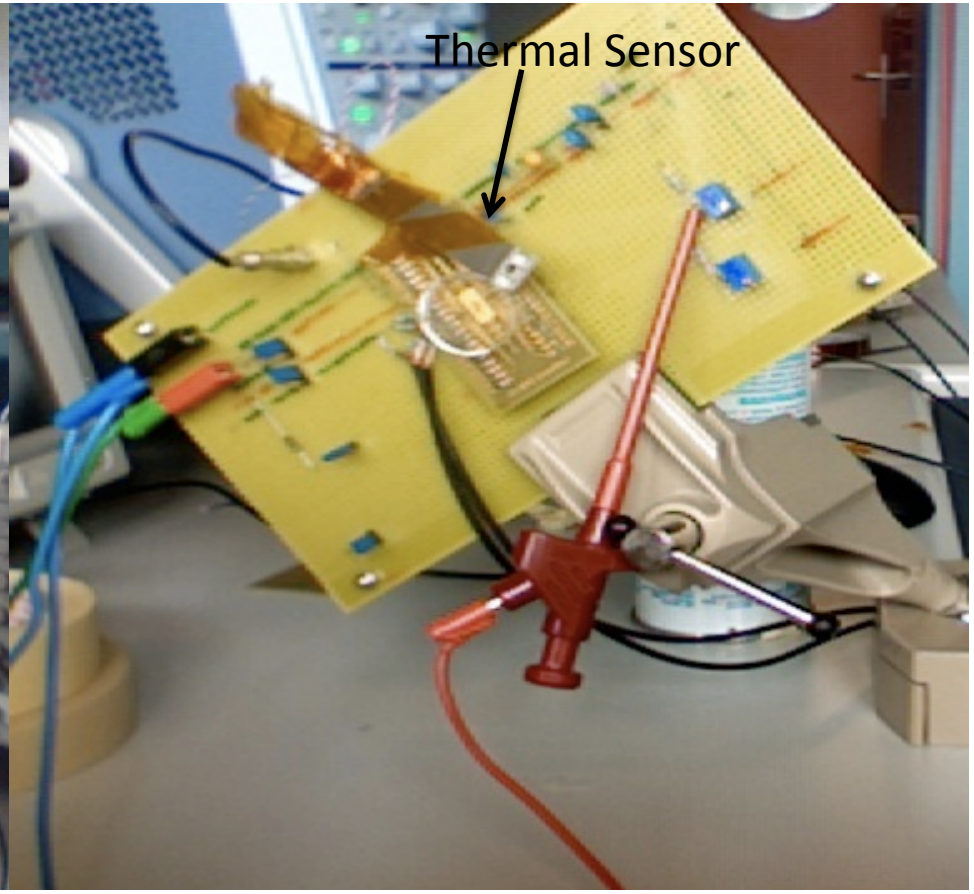
Next Step

For ADC, need to take some more measurements by connecting microprobe to the spy pad to understand the unequal step.

For PLL, calculate locking time using irradiated chip.

Back up Slide

Test Set up for calculation of Locking time at low temperature.



1,1,1,2-Tetrafluoroethane