

Charge Collection Efficiency on Irradiated Pixels

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UIC

Purpose

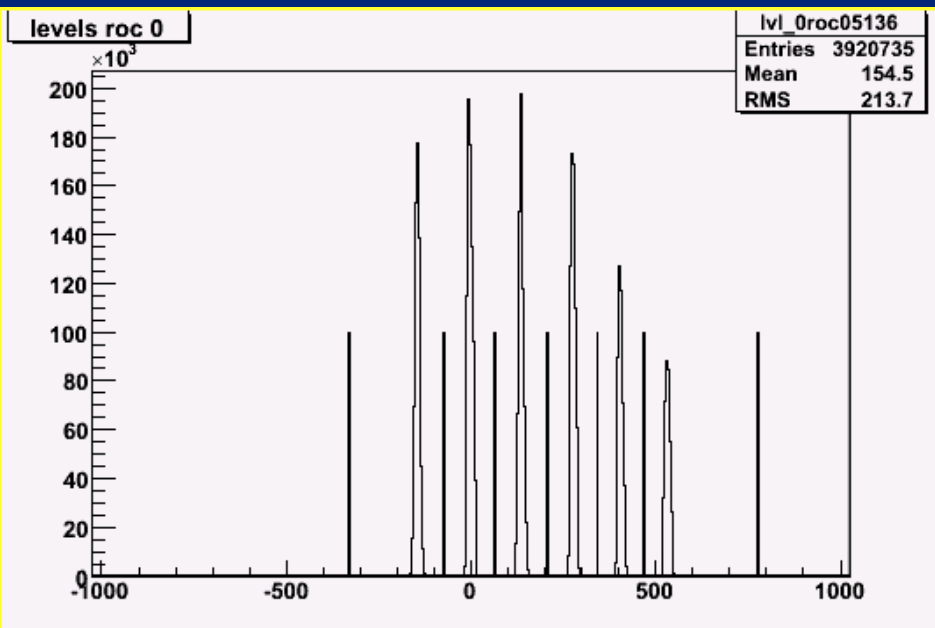
- The purpose of this study is to determine how efficiently chips can collect charge after being exposed to fluences ranging from $3.2\text{E}14$ – $5.1\text{E}15$.
- We wanted to see at what point the chips yielded inadequate results, and how long this took.
- The control was the unirradiated chip, from which charge was also collected. The source used was Sr-90.

Taking Data

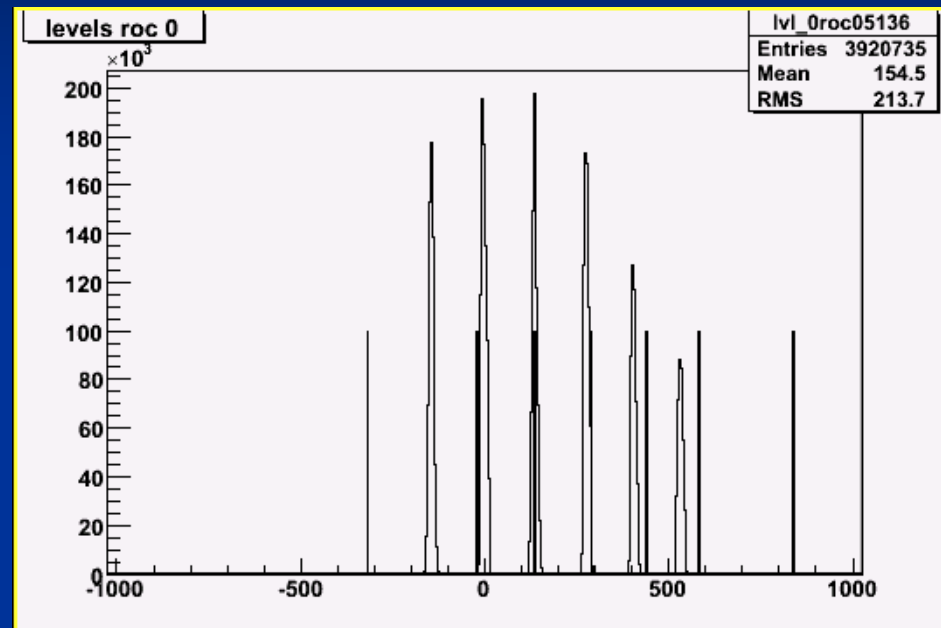
- Chips are cooled down to -25°C with better cold box (before, at -15°C)
- Each chip is calibrated with PreTest and other calibration test.
- A value of V_{cal} trim is set. Normally this is 45 V, but for higher fluences 55 V works best as shown from improved results.
- Depending on the leakage current, data and S-curves are taken for bias voltages ranging between 200-800 V.
- Data is analyzed using analysis code.

Progress

- Ran complete tests on several chips of varying fluences: mainly $5.1E15$
- Analysis consisted of determining whether fits looked like certain distributions; if not, something needed to be fixed
- We figured out how to fix bad address levels and recorded this in the Twiki



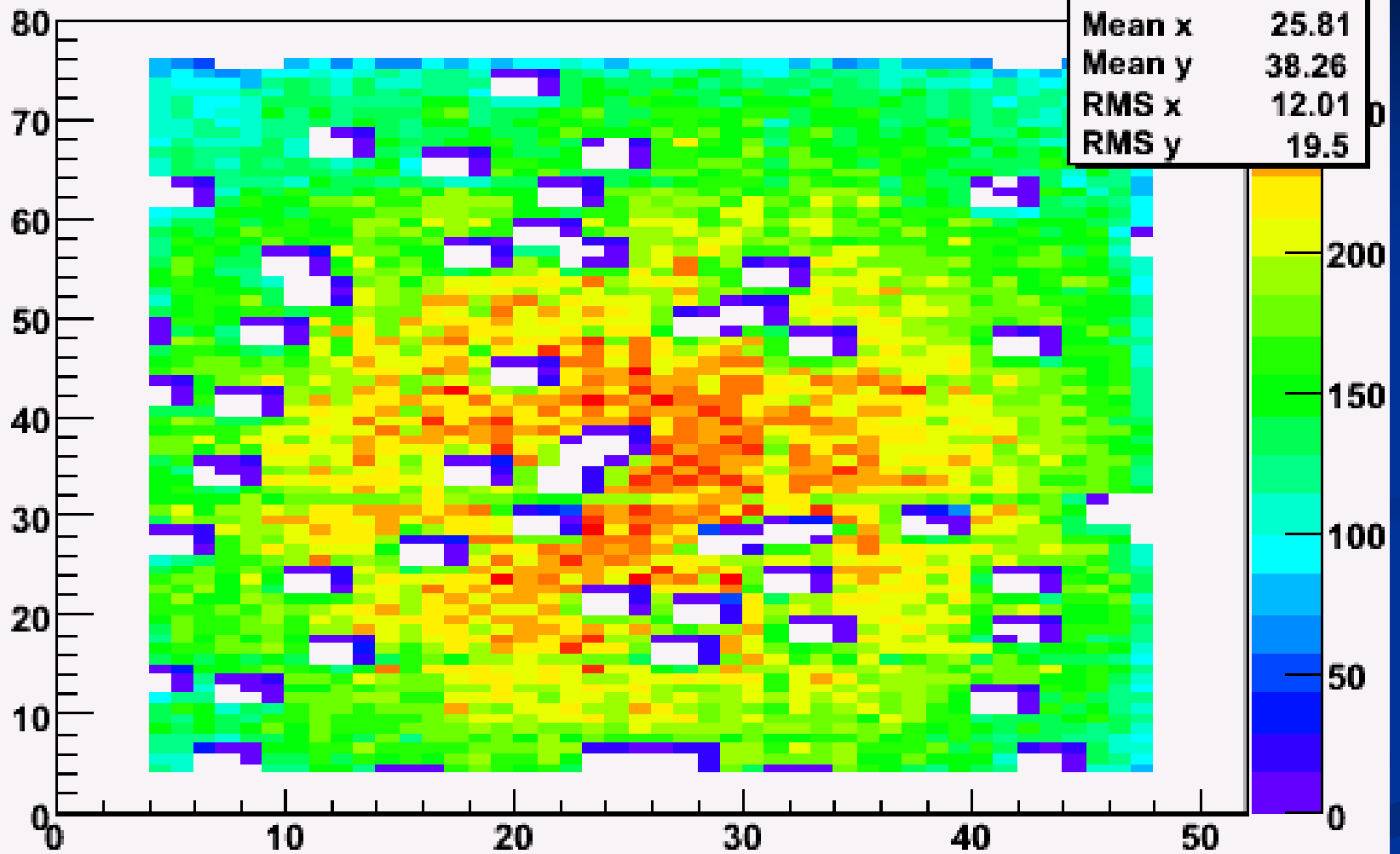
Before



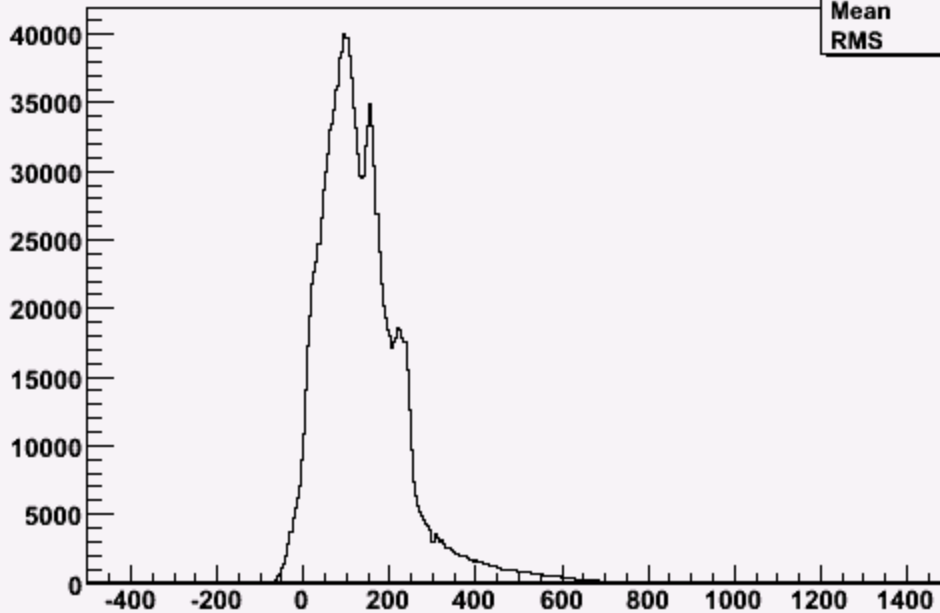
After

Position of all Clusters Run 5138

cCentre0_5138	
Entries	476942
Mean x	25.81
Mean y	38.26
RMS x	12.01
RMS y	19.5

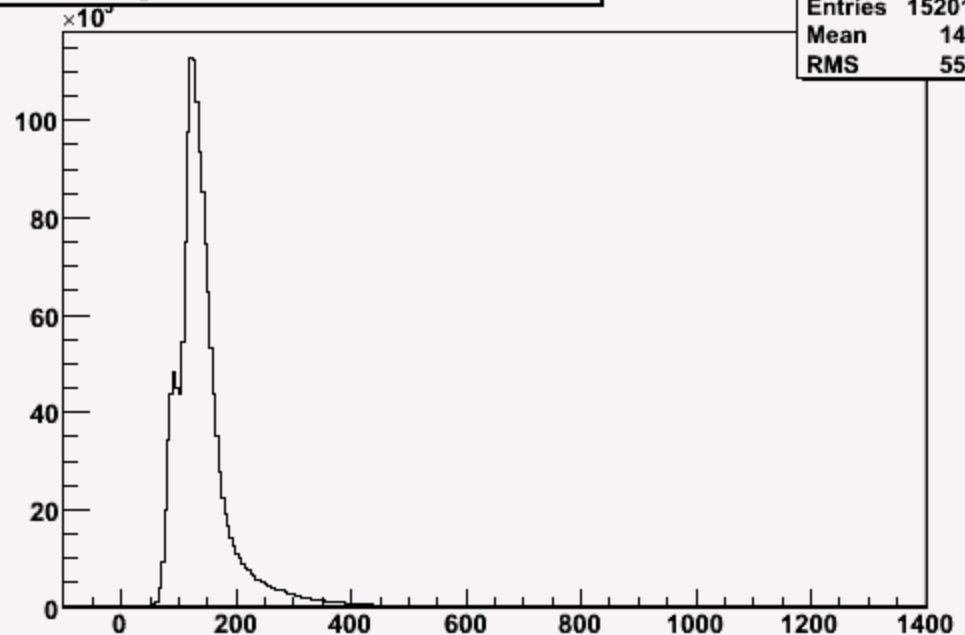


Pulse height Distribution ADC counts



- Landau Distribution for ADC graph

Pulse height Distribution in Vcal units



Hikes

