

Address Levels study using micro-twisted pair cables with different lengths

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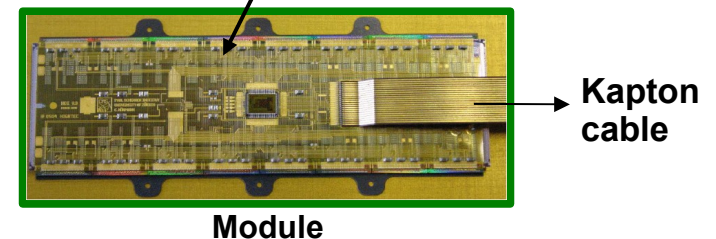
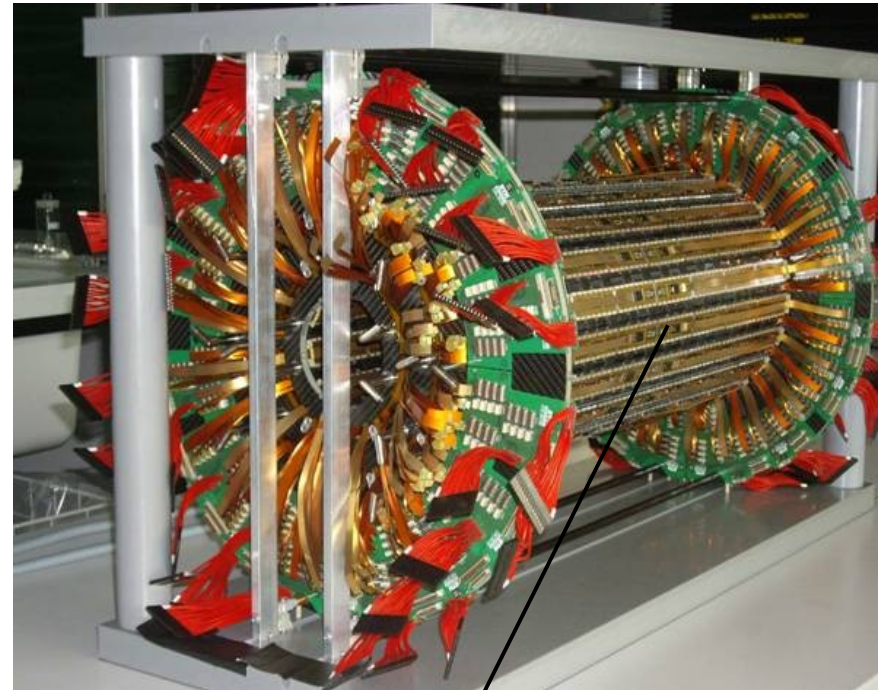
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PIRE Conference, University of Nebraska. September 2009

Motivation

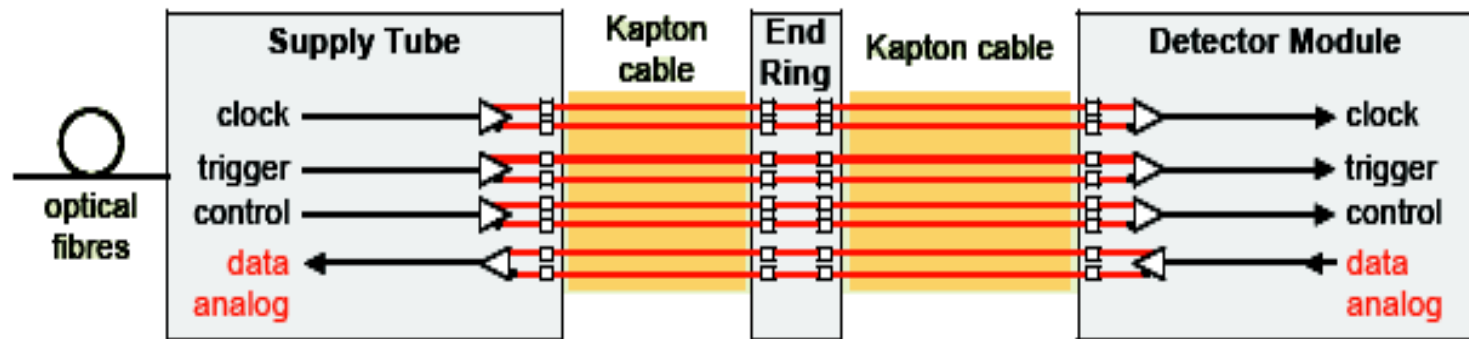
- Operate the accelerator at an order of magnitude higher luminosity of $10^{35} \text{ cm}^{-2} \cdot \text{s}^{-1}$
- Even at design luminosity the innermost layer of the barrel has to be replaced after four years.
- Goals
 - Reduction in material budget.
 - Reasonable time scale/costs.
- One possible aspect of the pixel upgrade: Kapton cables replaced with Copper Cladded Aluminum (CCA) wires. This way material within the tracker volume (BPIX) can be minimized.

CMS pixel detector barrel

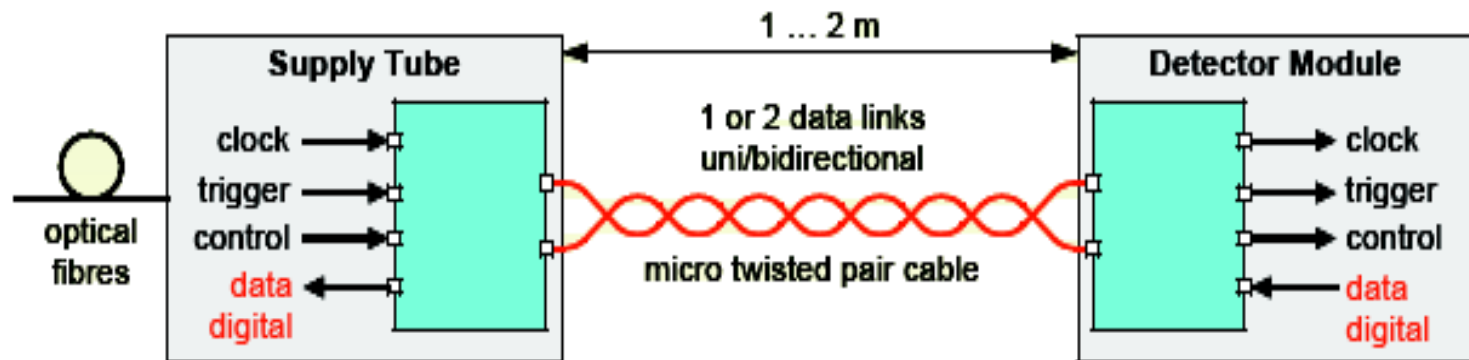


New Concept

Existing System in CMS Pixel Detector



New Concept



Replacing Kapton cables

“Justification”

- Kapton cables are expensive and limited in length (40 cm).
- Minimal material budget → micro twisted pair (unshielded).
- Minimal power consumption → low voltage swing → differential.
- Pass clock, signal, data all down one line instead of 21 or even twist 16 wires together and do a straight replacement just farther downstream.
- More freedom in bending cables in all directions.
- Can move optical links with auxiliary chips further out (~50cm) to high range and remove material budget from sensitive tracking region.
- use μ -twisted pairs 2x125 μ m of enameled Copper Cladded Aluminum (CCA) wires might provide a viable signal cable alternative for Kapton cables



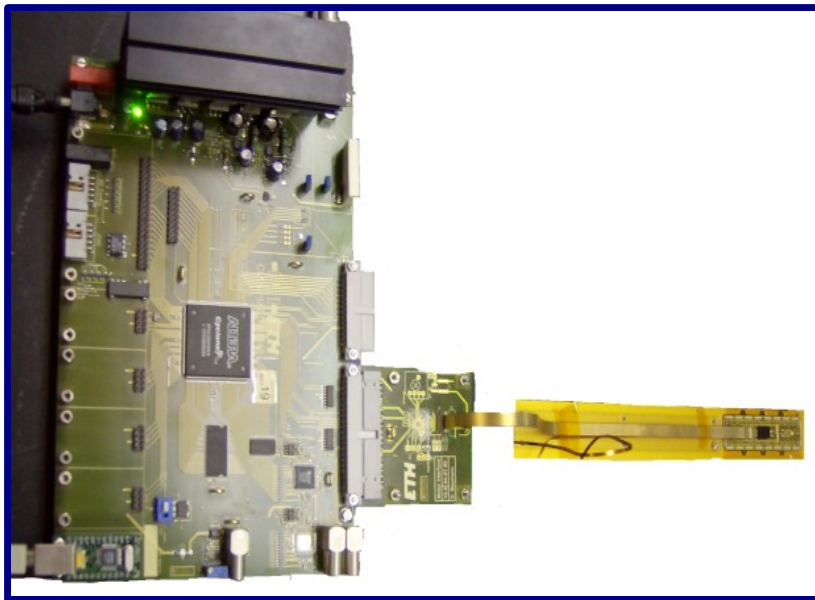
Kapton Cable



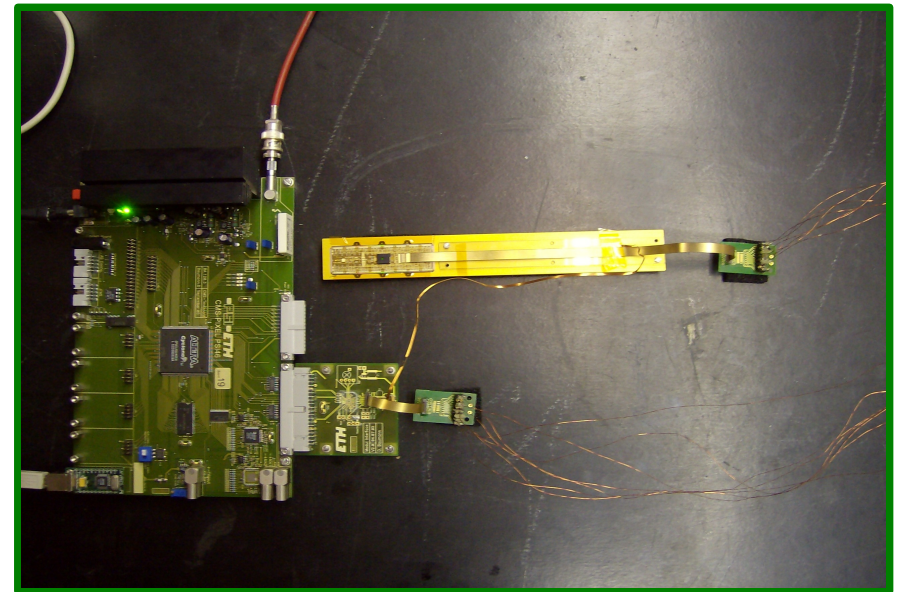
Micro-Twisted pair

Experimental Setup

Normal connection



With micro-twisted pair cable connection



Traces used to transport the control signals to the module

R_{TERM}	
Mod-side	Adapter-side
SDA_IN: 180 Ω	SDA_O: variable
CTR: 180 Ω	AOUT1: variable
CLK: 180 Ω	AOUT2: variable

Adapter-side

SDA_O: variable
AOUT1: variable
AOUT2: variable

Traces used to bring the analog information from the module

- Resistances on the module side were kept constant at 180 Ω .
- Resistances on the adapter side were set equal to each other and varied.
- Different lengths of cable were used.

History

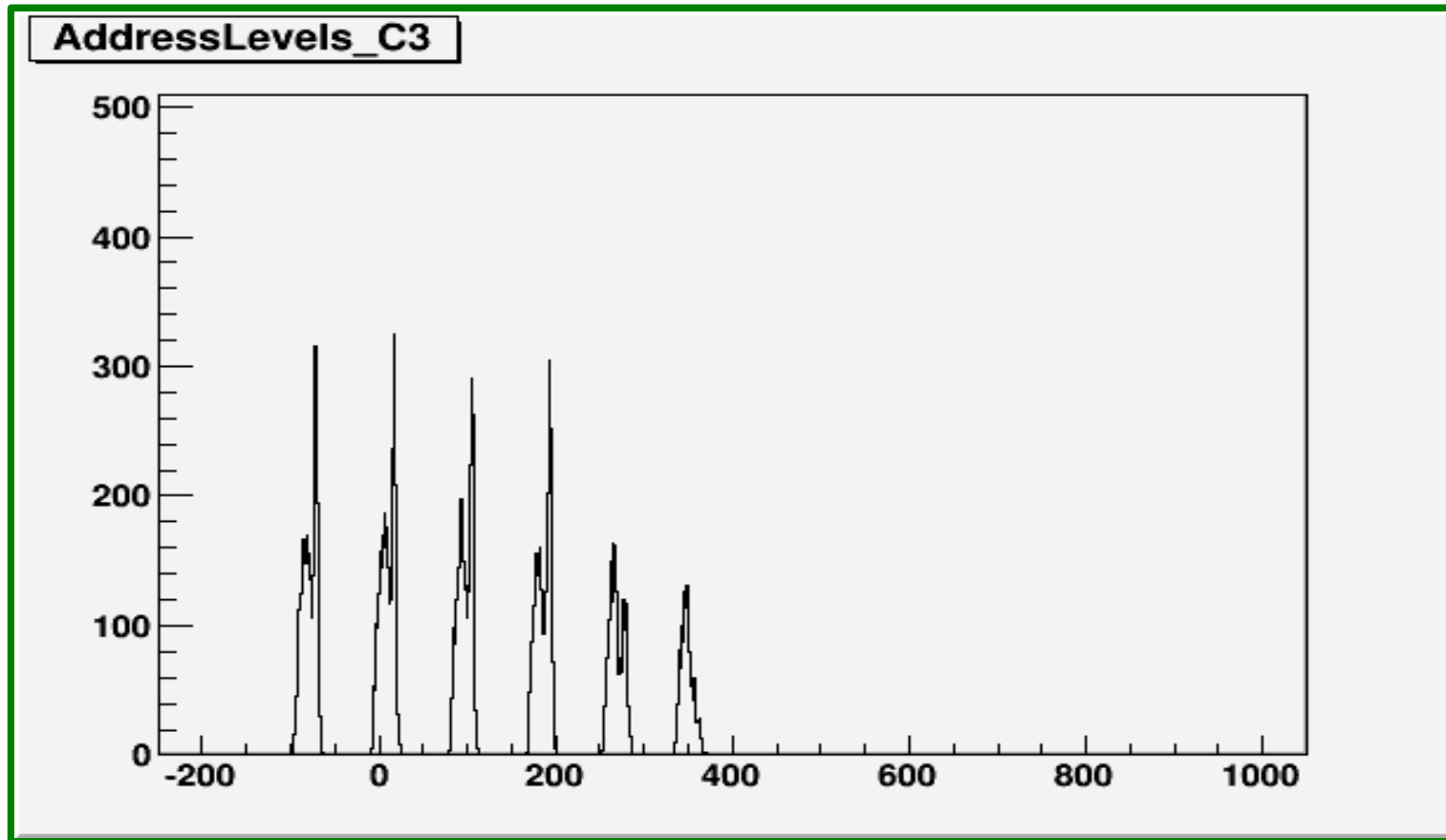
- Although we had been able to demonstrate the viability of using cables of 2.0m in length, we had encountered some problems with other lengths.
 - Pre-test failed sometimes.
 - Even when the pre-test worked, the address level distributions were too wide.

Progress

- Pre-test – Several problems were found with the algorithm that was being used for the pre-test.
 - The main one was that the pre-test failed if there was no pulse height with the initial delay value.
 - We now have a pre-test algorithm that never fails (thanks to Jhon).

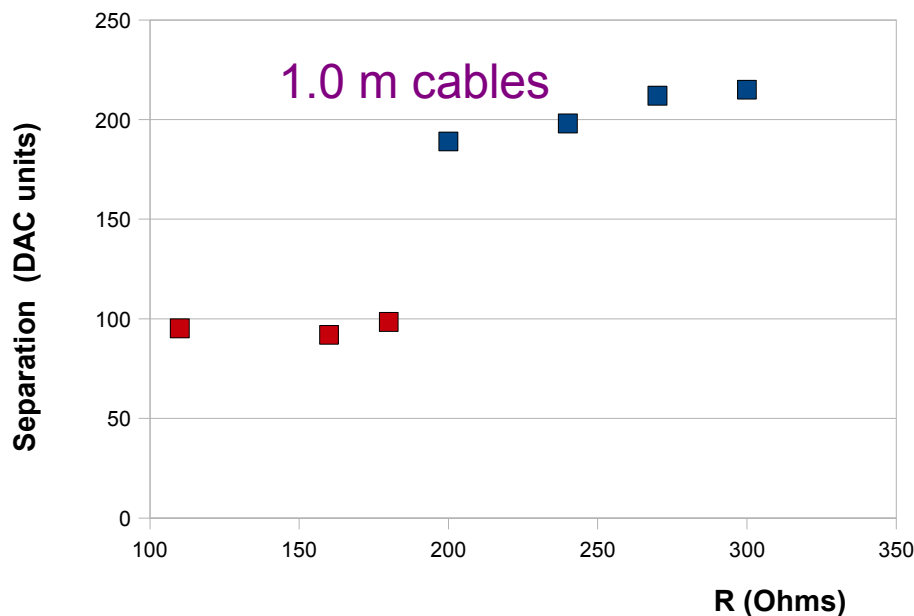
- Address Level Distributions - These improved by using other values for the resistances.
 - We have done a systematic study of performance as a function of cable length and resistance.

Quality ratio



- To define optimum performance, we defined a quality ratio, QR, as follows.
- $QR = RMS / SEPARATION$
- RMS is the rms for an address level averaged over all address levels.
- SEPARATION is the average separation between adjacent address levels.
- We want QR to be as small as possible.

Address Level Separation



★ A discontinuity is observed.

★ This is correlated with the value of the parameter DACgain which is adjusted automatically by the pre-test. For resistances below about 200 Ohms, the pretest sets DACgain to 128 (red points). Above 200 Ohms, it sets DACgain to ~200 (blue points).

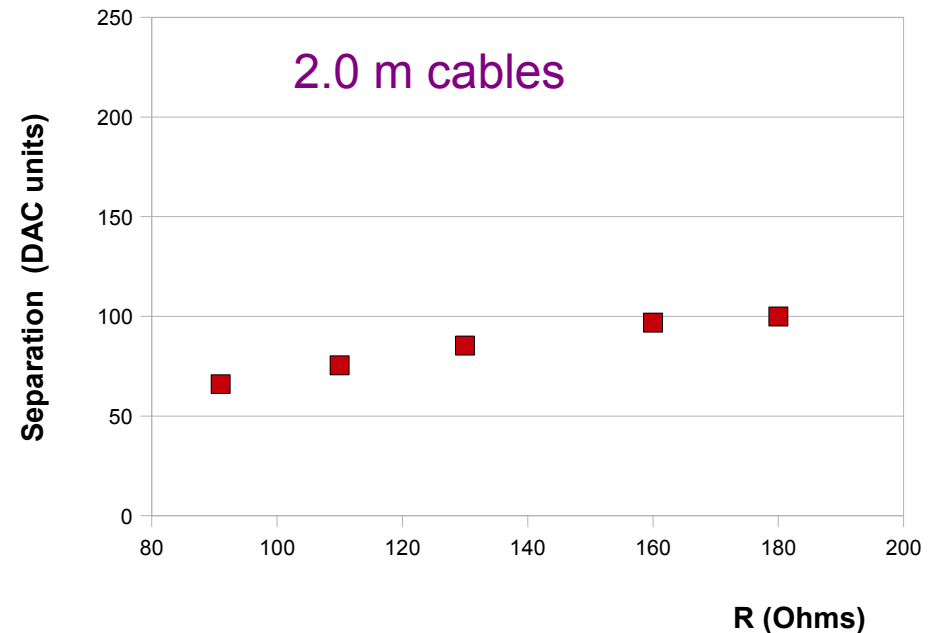
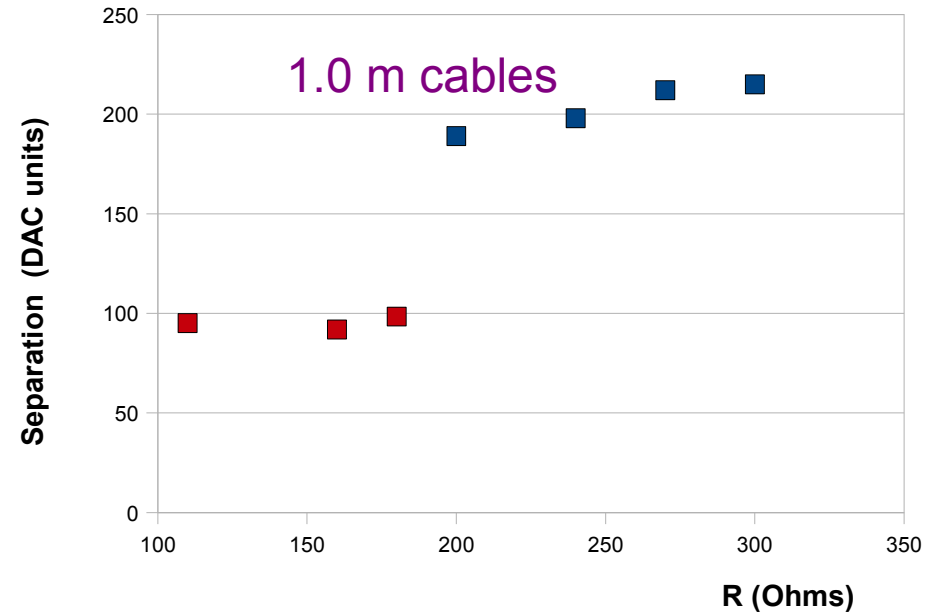
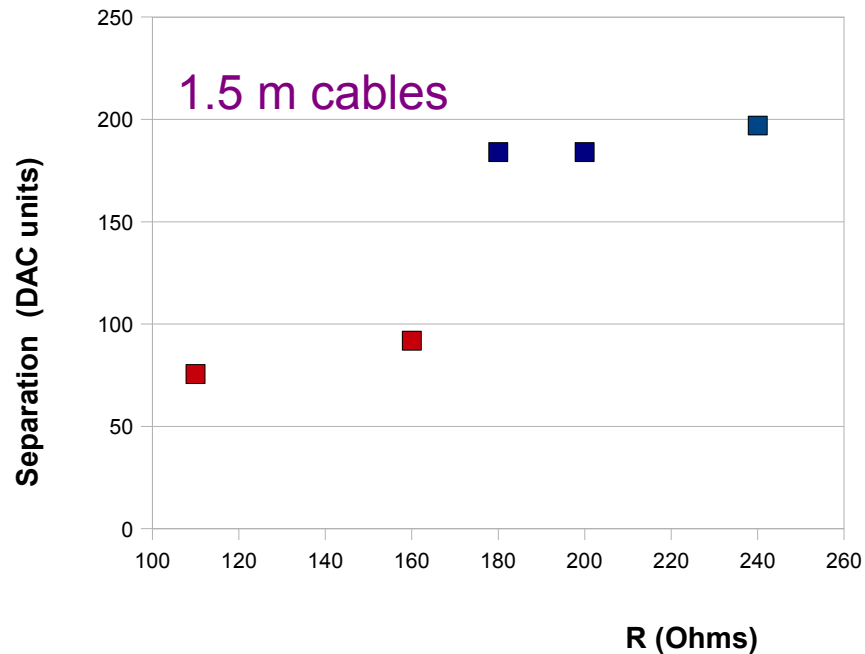
★ We do not know why DACgain is set in this way. It obviously has an effect on the absolute size of the levels and we suspect it also affects the signal pulse height but we need to find out in more detail what this parameter does.

★ Our definition of the quality ratio make our results insensitive to the absolute size of the levels.

Address Level Separation

Here are all the results.

For 2.0 m all resistances studied were below 200 Ohms.

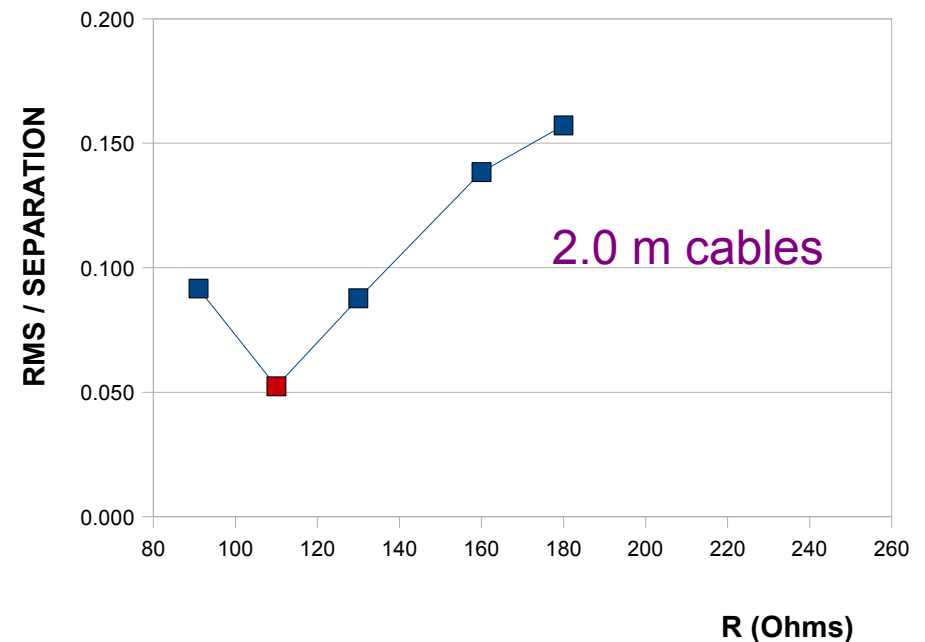
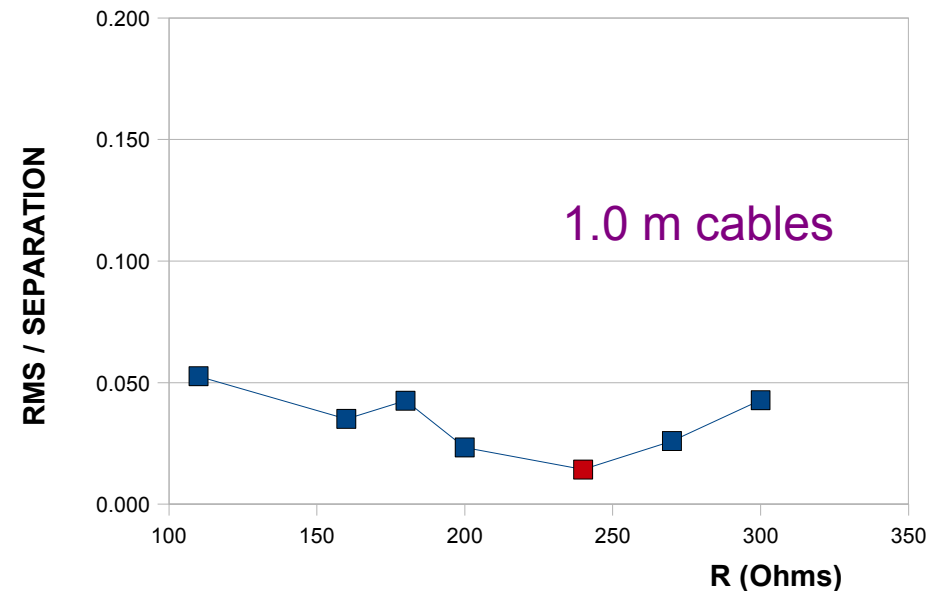
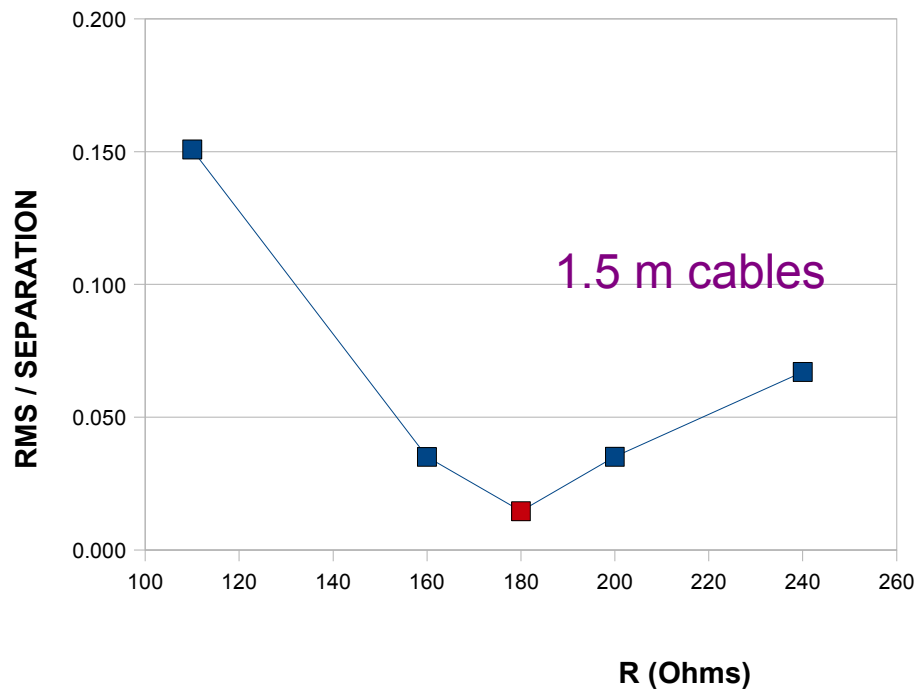


Quality Ratio vs Termination Resistance

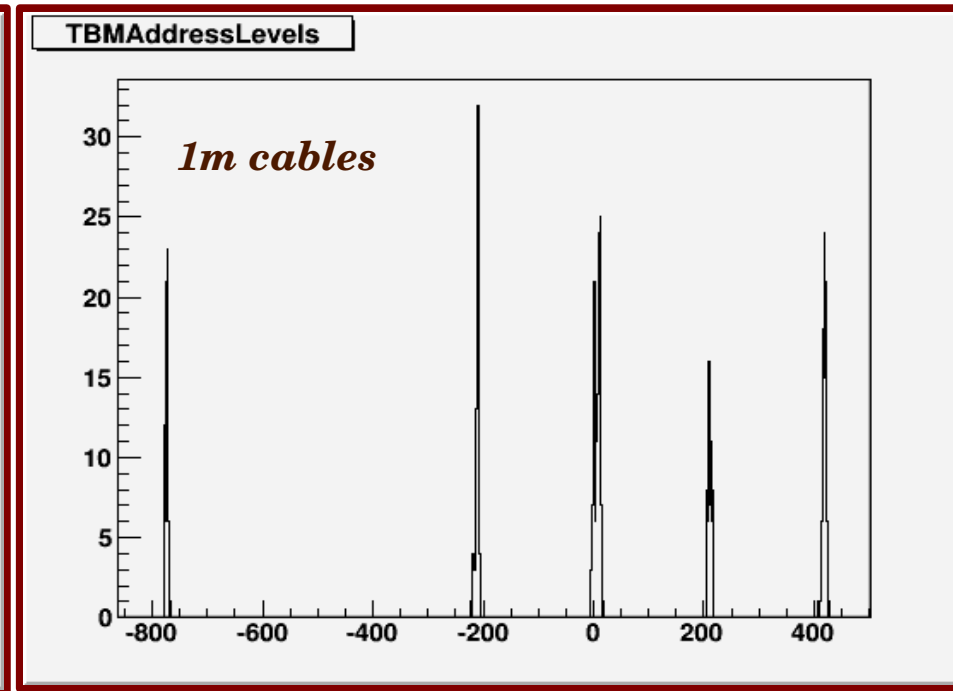
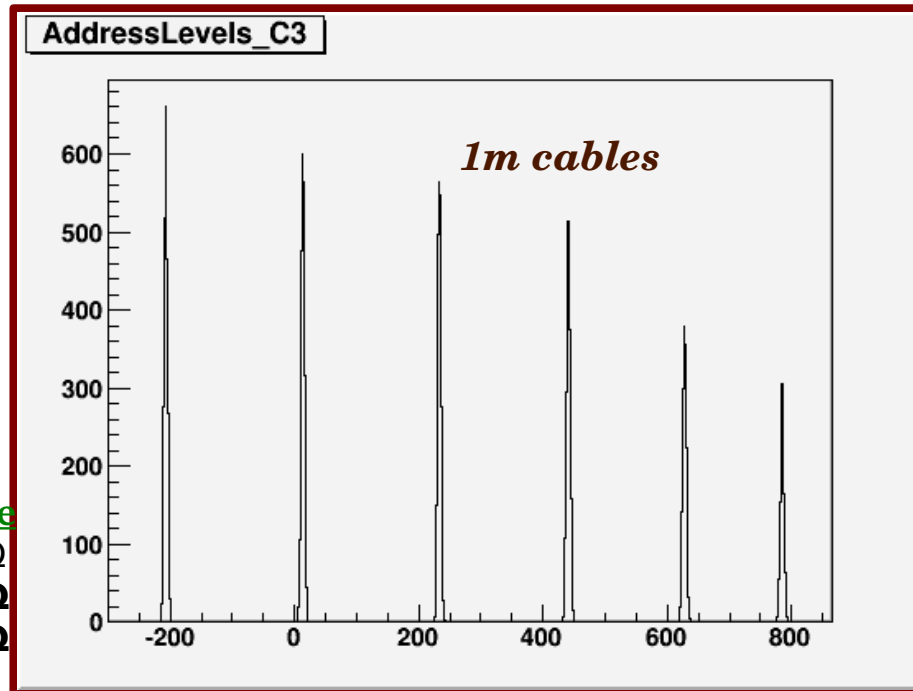
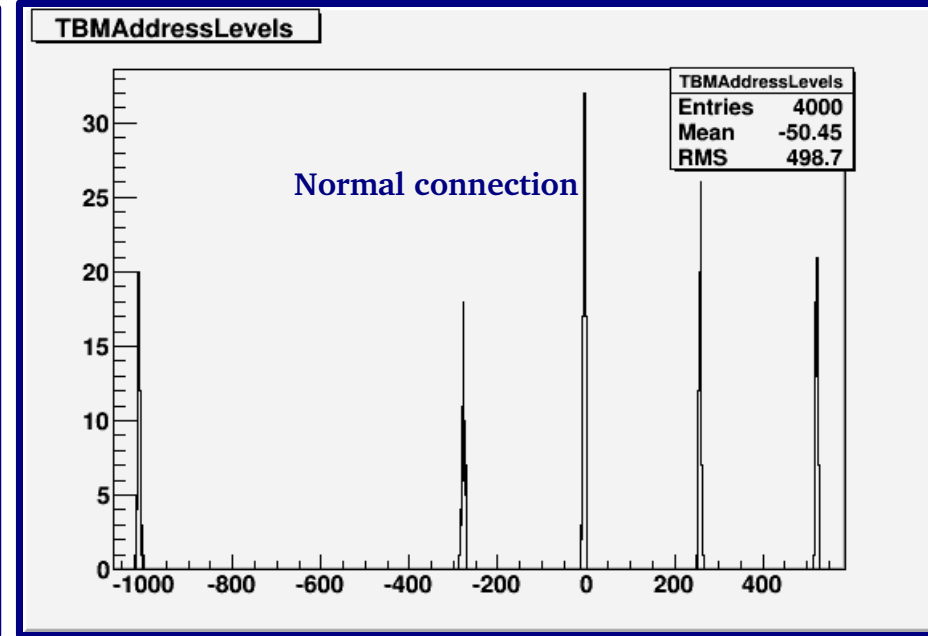
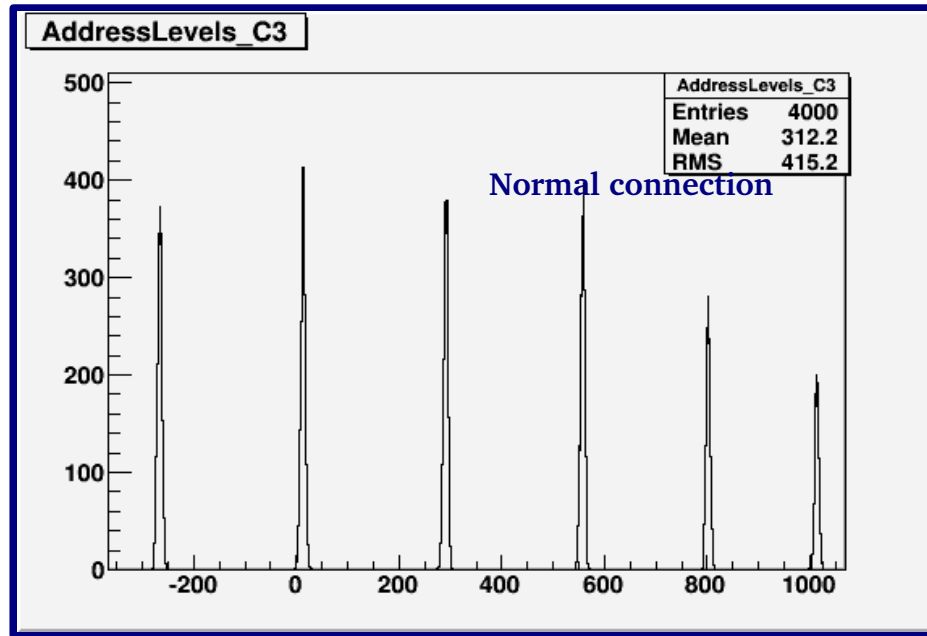
There is an optimum resistance for each length which minimizes the quality ratio.

Values of the minimum quality ratios are quite acceptable.

The “sharpness” of the minimum increases with cable length.



Optimum Address Levels (ROC 3) & TBM Levels



R_{TERM}

Mod-side

SDA_IN: 180Ω
CTR: 180Ω
CLK: 180Ω

Adapter-side

SDA_O: 240Ω
AOUT1: 240Ω
AOUT2: 240Ω

Optimum Address Levels (ROC 3) & TBM Levels

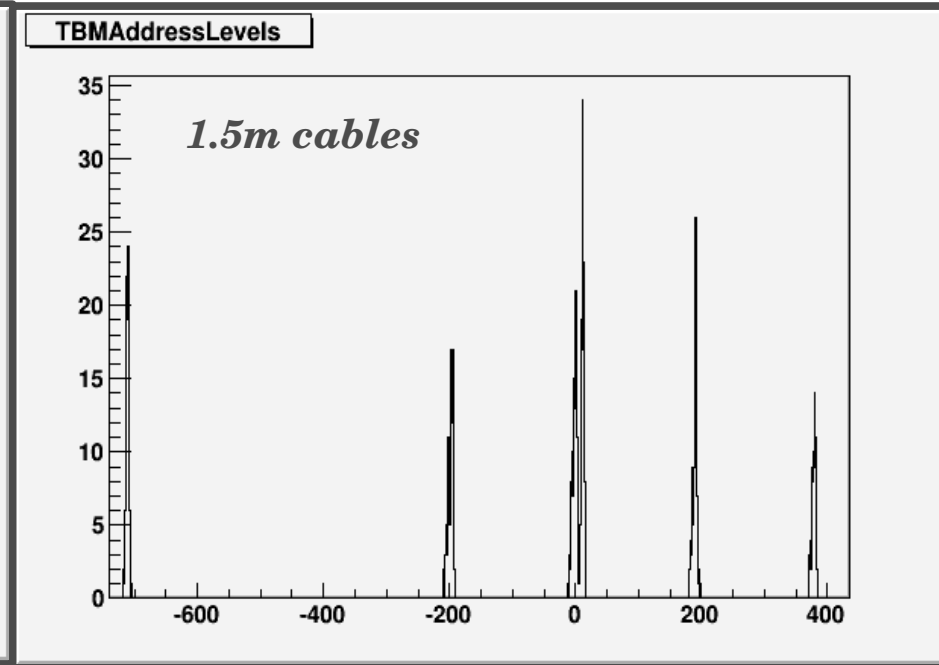
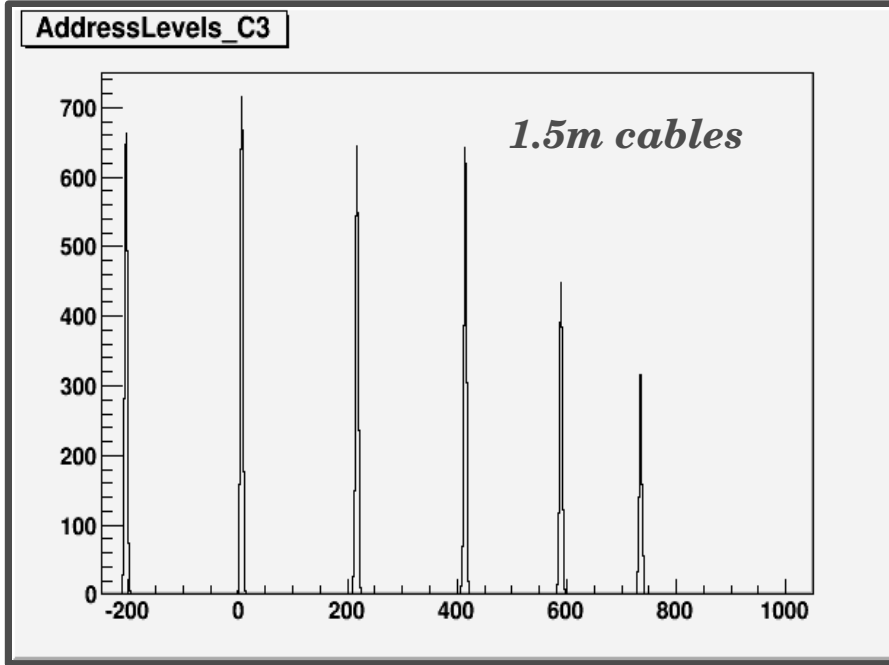
R_{TERM}

Mod-side

SDA_IN: 180Ω
CTR: 180Ω
CLK: 180Ω

Adapter-side

SDA_O: 180Ω
AOUT1: 180Ω
AOUT2: 180Ω



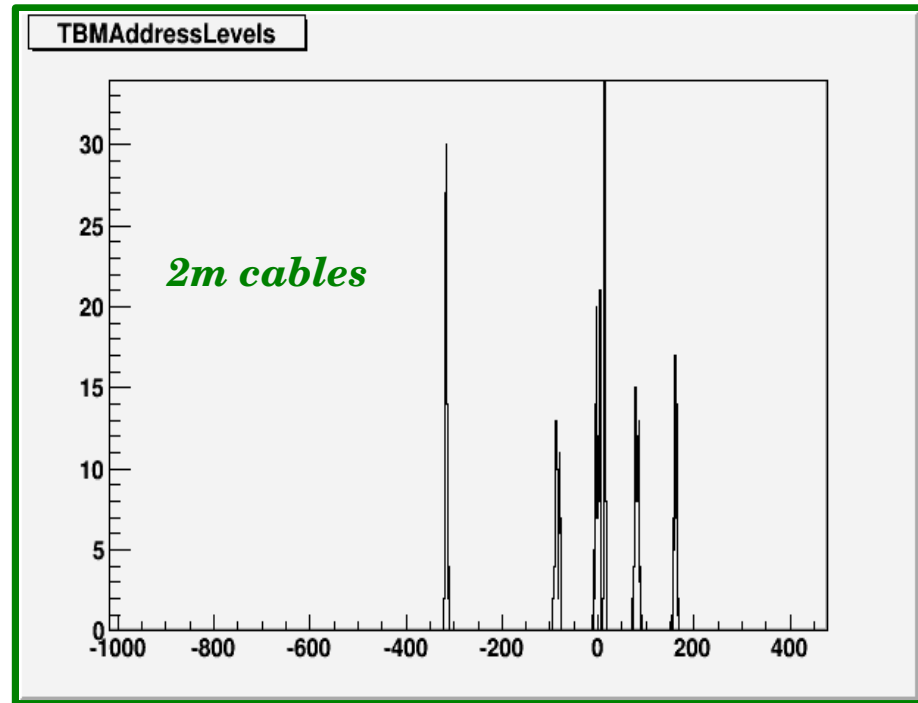
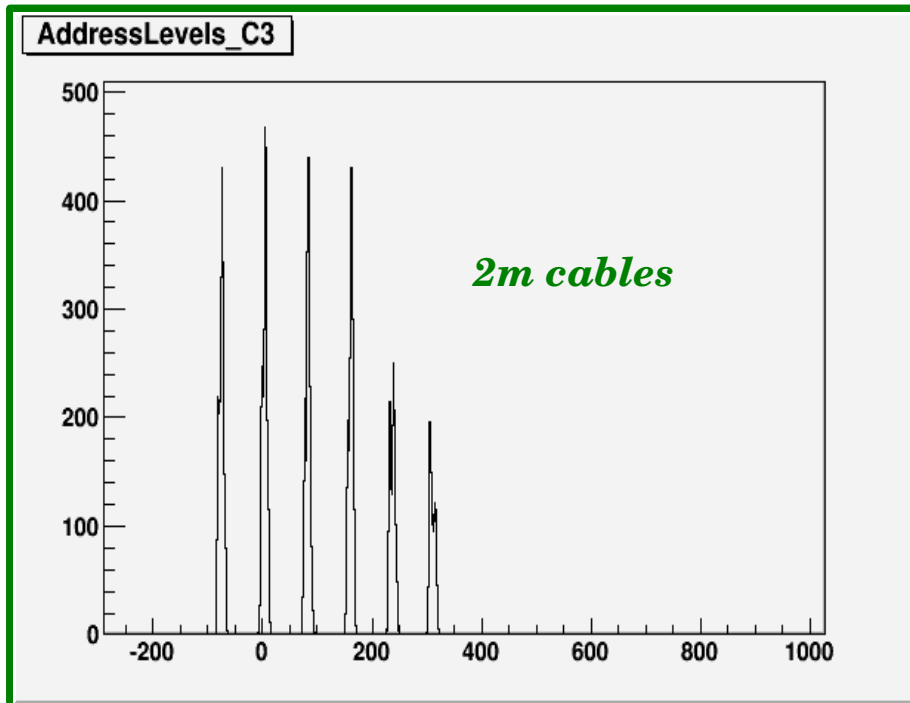
R_{TERM}

Mod-side

SDA_IN: 180Ω
CTR: 180Ω
CLK: 180Ω

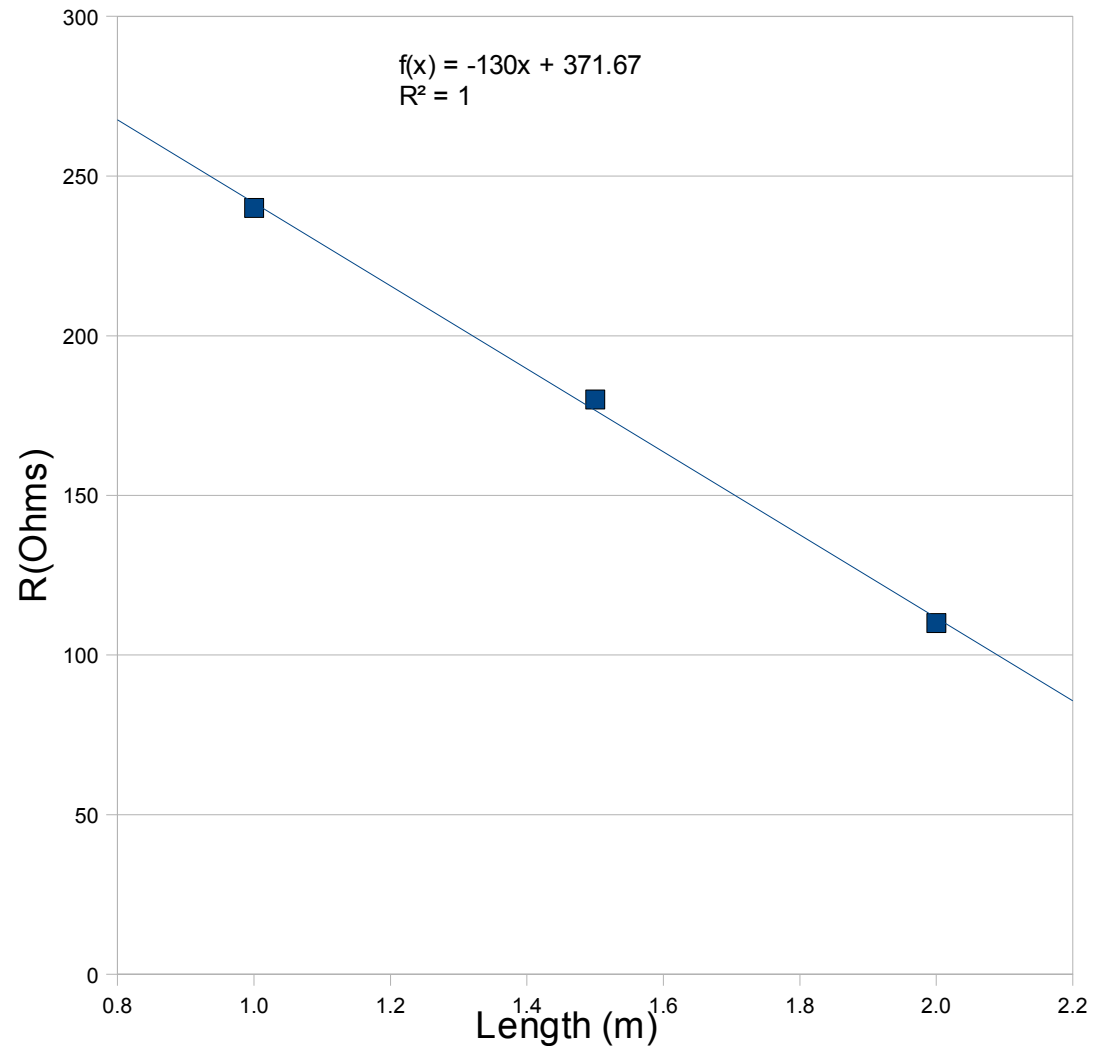
Adapter-side

SDA_O: 110Ω
AOUT1: 110Ω
AOUT2: 110Ω



$R_{optimum}$ Vs Length

There seems to be a lineal relation between optimum resistance and length but we have only measured three points.

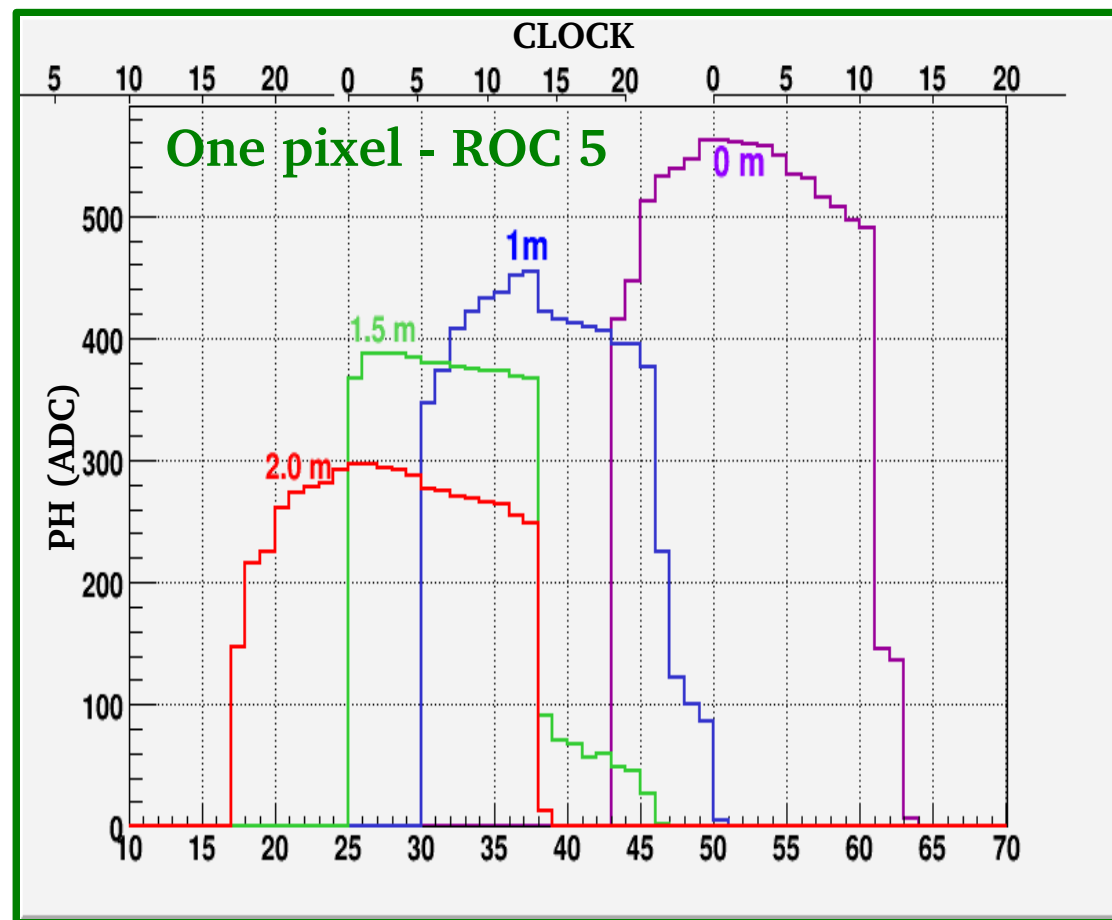


Results

Length(m)	R _{term} (Ohms)	RMS	Separation	RMS/Separation
1.0	110	5.01	95.2	0.053
1.0	160	3.22	91.9	0.035
1.0	180	4.19	98.4	0.043
1.0	200	4.41	189.0	0.023
1.0	240	2.82	198.0	0.014
1.0	270	5.50	212.0	0.026
1.0	300	9.20	215.0	0.043
1.5	110	11.40	75.6	0.151
1.5	160	3.22	91.9	0.035
1.5	180	2.69	184.0	0.015
1.5	200	6.46	184.0	0.035
1.5	240	13.20	197.0	0.067
2.0	91	6.05	66.0	0.092
2.0	110	3.95	75.4	0.052
2.0	130	7.49	85.4	0.088
2.0	160	13.40	96.8	0.138
2.0	180	15.70	99.9	0.157

CLOCK study

- In Jhon's new version of the pretest, a scan of the CLOCK delay (in 1 ns steps) is done in order to determine and set an optimum value.
- This parameter controls the sampling time interval of the ADC on the test board.
-
- Smaller values of the CLOCK parameter correspond to later sampling times.
- The CLOCK value is set as to give maximum pulse height.
-
- The results are consistent with the fact that the signal takes time to travel down the cable.
-
- The PH vs delay distributions are different for different cable lengths.

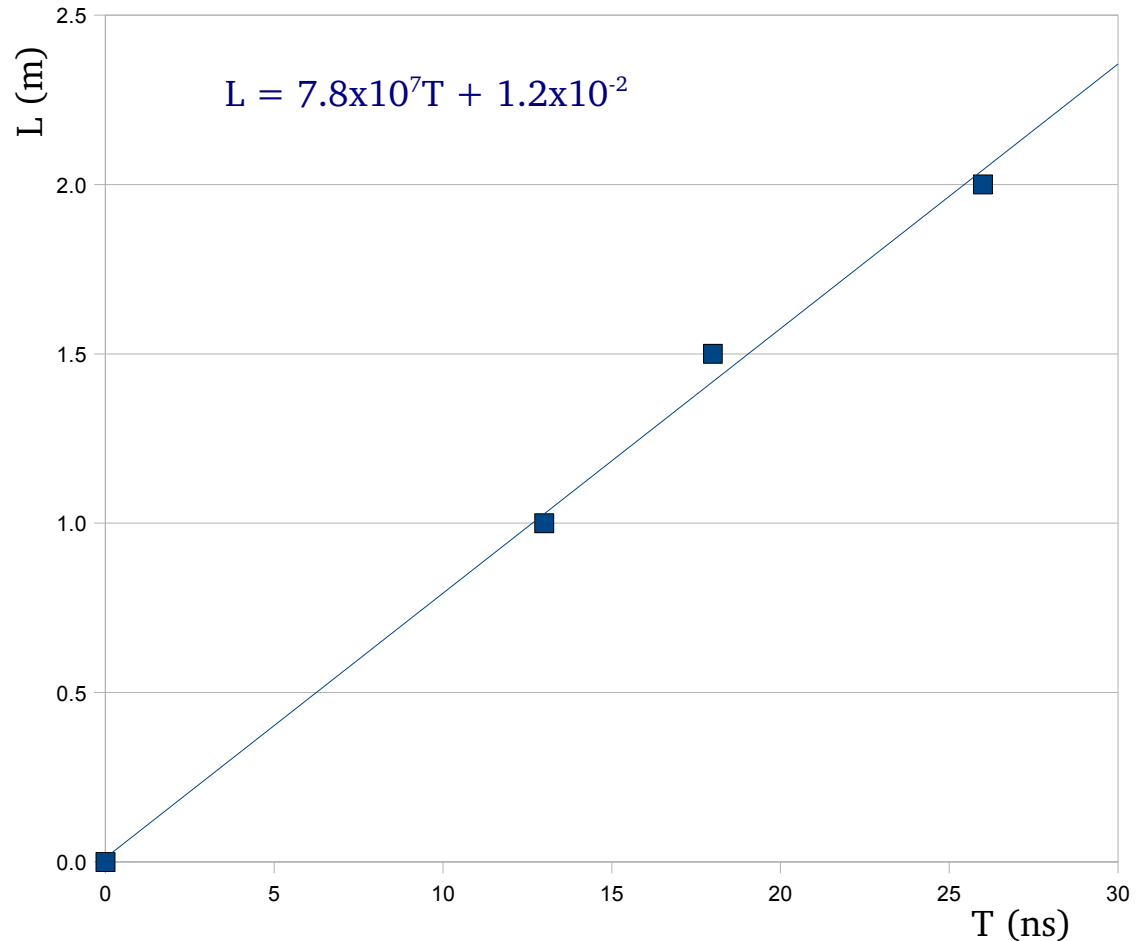


Measurement of the pulse height of a random pixel as a function of delay.

Length Vs Timing

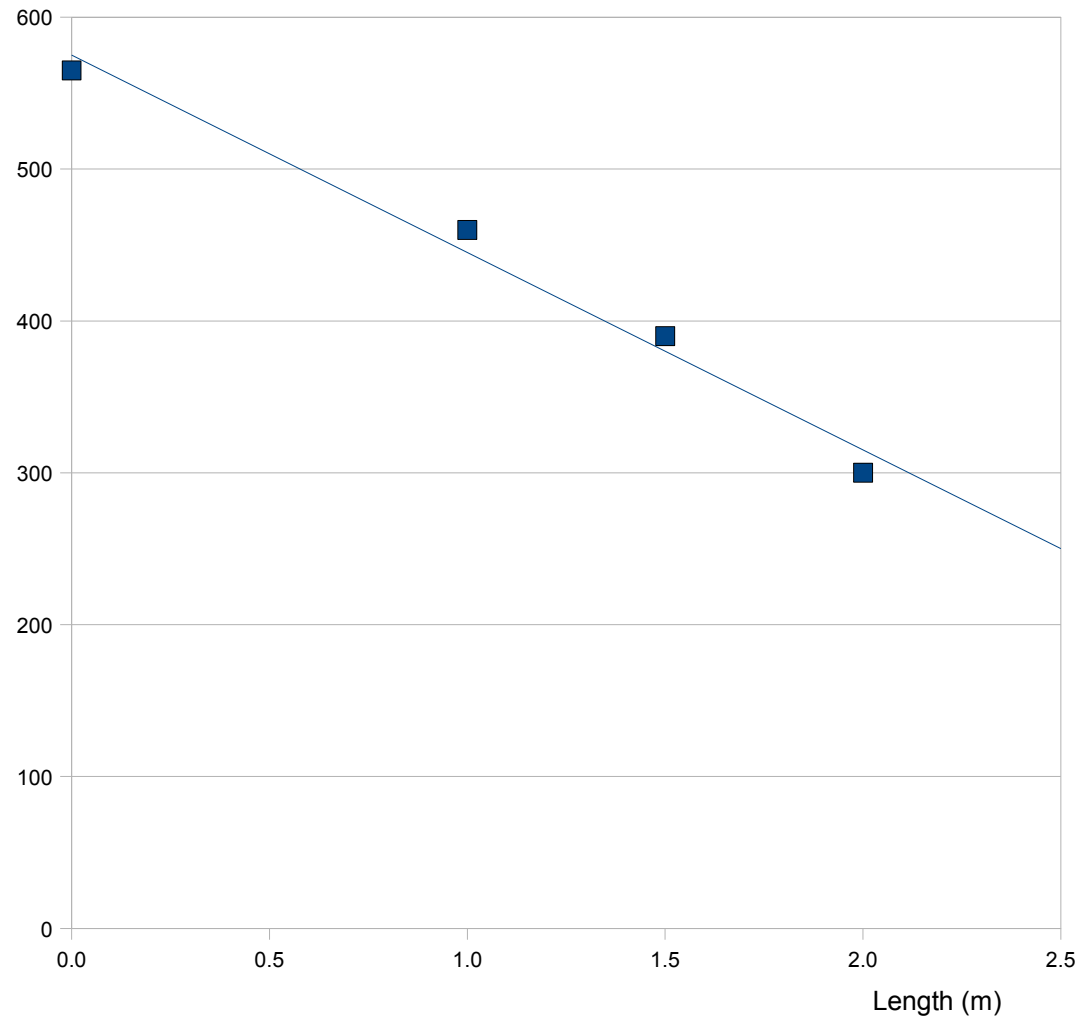
In order to measure a propagation velocity, we define the time for each length using the leading edge of the distributions.

We get a velocity of $0.26c$.



Max PH value Vs Length

Attenuation of the signal height is observed and it seems to be lineal.



Conclusions

- We can obtain satisfactory performance for all lengths of micro-twisted pair cables. This was obtained changing the pre-test algorithm and changing the AOUT1 and AOUT2 resistance values in the test adapter side.
- More detailed studies are in progress specifically a study of simulation on SIMatrix with transmission lines to try understand the results with different resistance values and lengths.

Backup Slides

1.0 m cables

R_{TERM}

Mod-side

SDA_IN: 180 Ω

CTR: 180 Ω

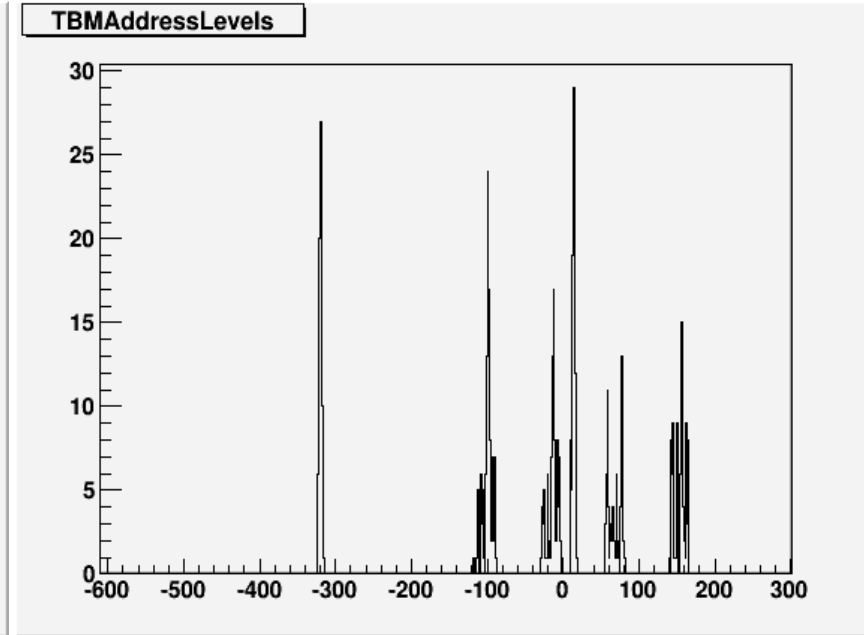
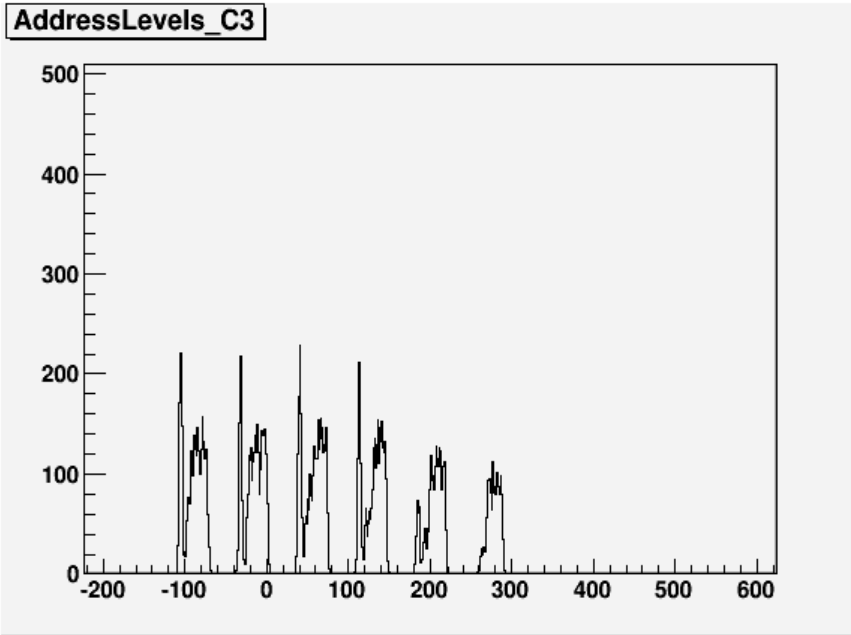
CLK: 180 Ω

Adapter-side

SDA_O: 110 Ω

AOUT1: 110 Ω

AOUT2 : 110 Ω



R_{TERM}

Mod-side

SDA_IN: 180 Ω

CTR: 180 Ω

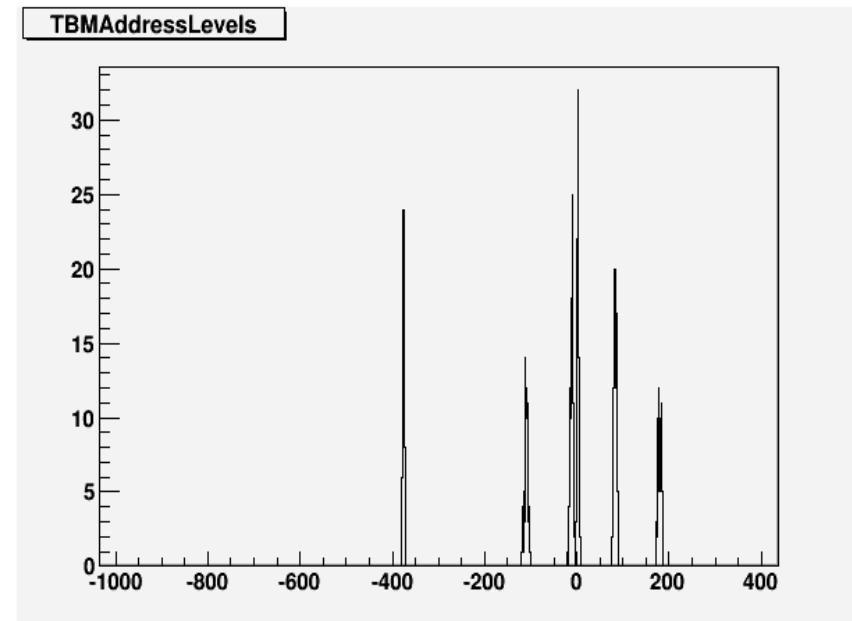
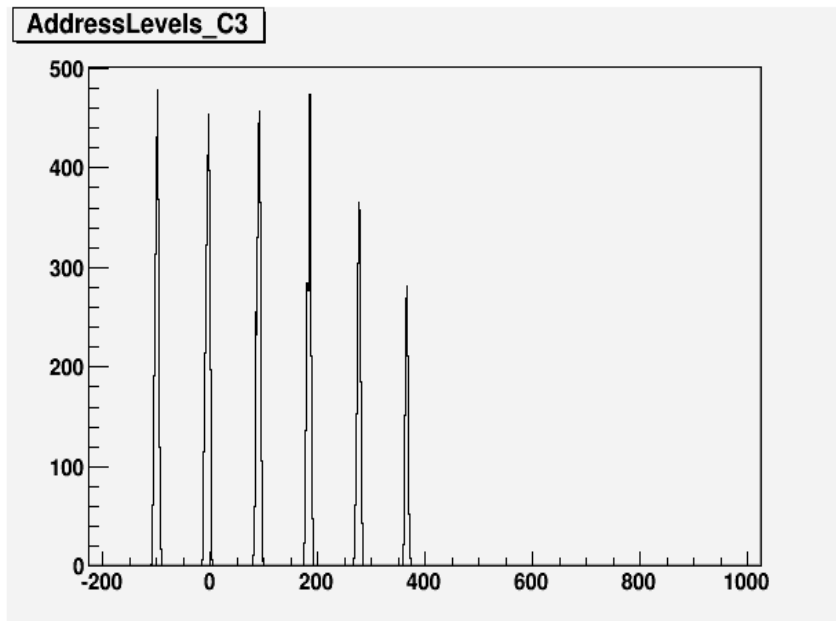
CLK: 180 Ω

Adapter-side

SDA_O: 160 Ω

AOUT1: 160 Ω

AOUT2 : 160 Ω



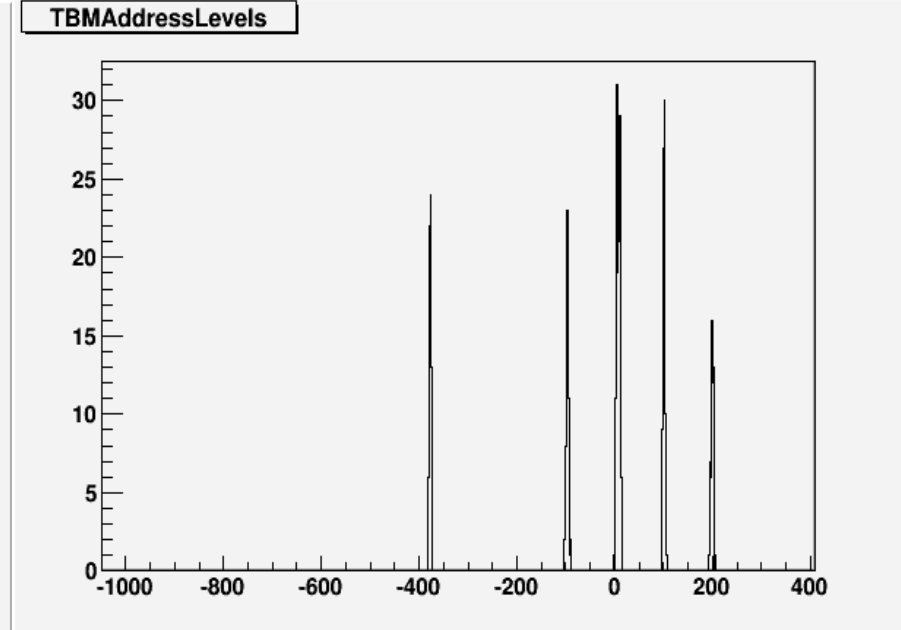
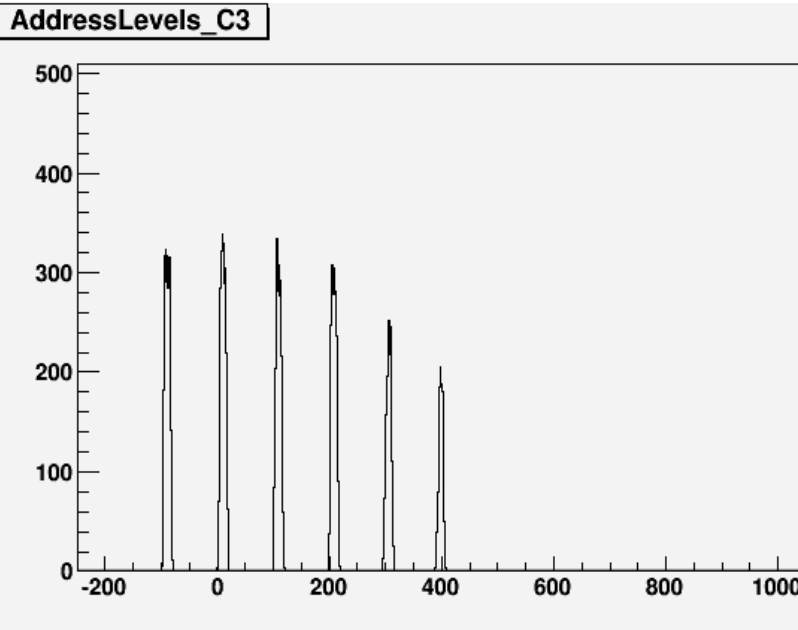
1.0 m cables

Mod-side

SDA_IN: 180 Ω
CTR: 180 Ω
CLK: 180 Ω

Adapter-side

SDA_O: 180 Ω
AOUT1: 180 Ω
AOUT2 : 180 Ω



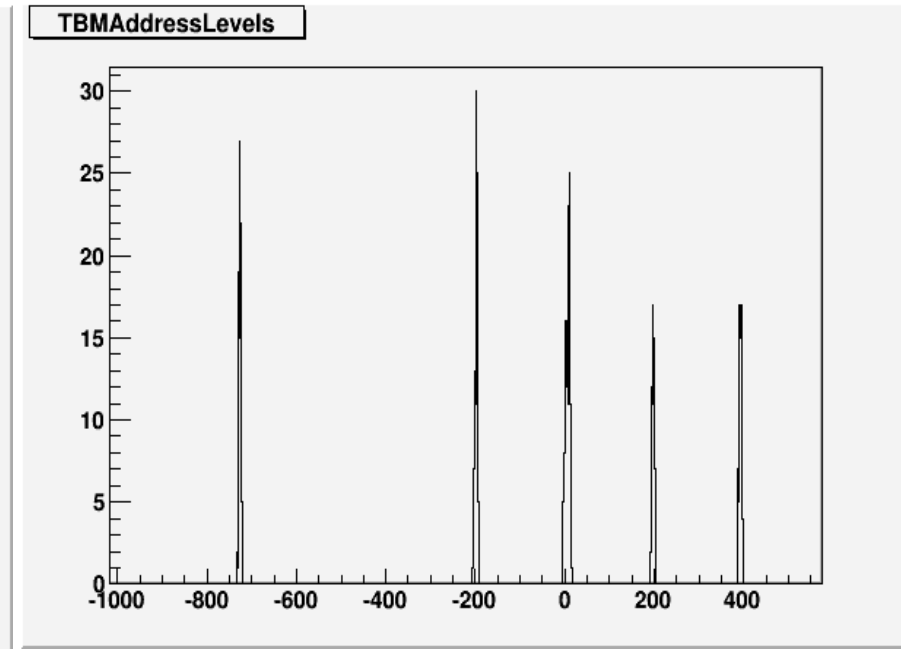
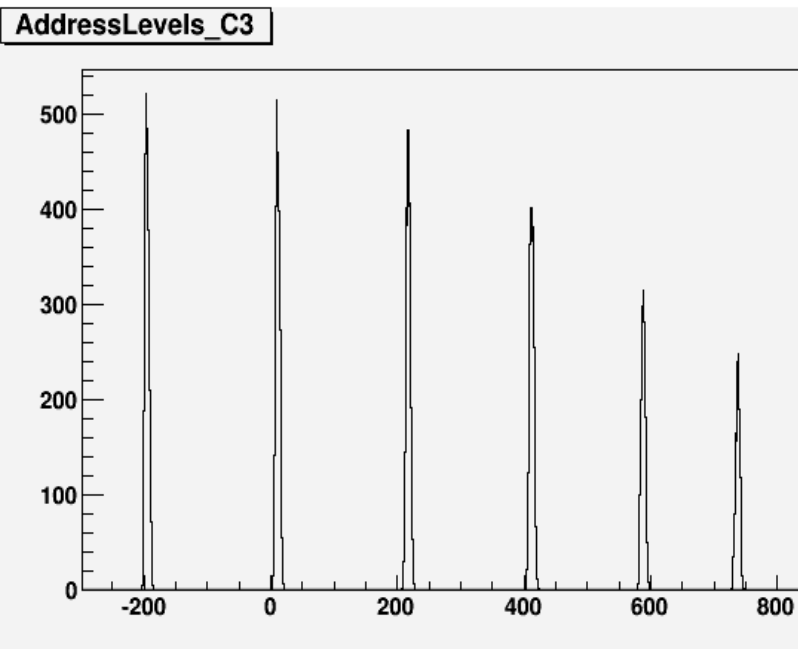
R_{TERM}

Mod-side

SDA_IN: 180 Ω
CTR: 180 Ω
CLK: 180 Ω

Adapter-side

SDA_O: 200 Ω
AOUT1: 200 Ω
AOUT2 : 200 Ω



1.0 m cables

R_{TERM}

Mod-side

SDA_IN: 180Ω

CTR: 180Ω

CLK: 180Ω

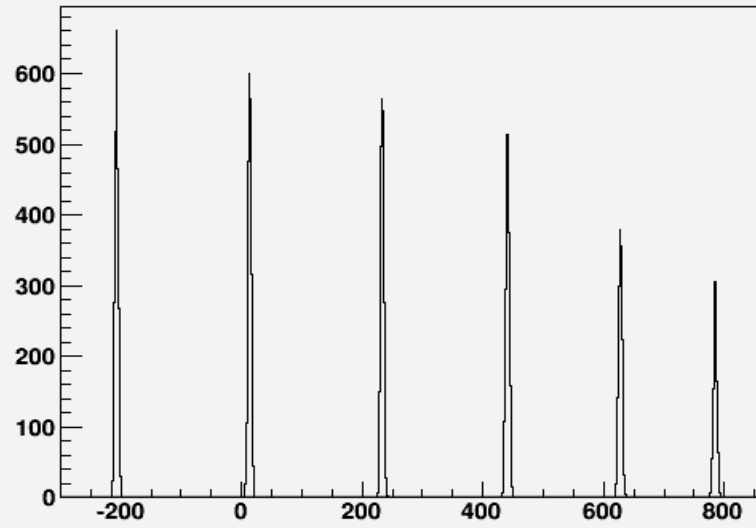
Adapter-side

SDA_O: 240Ω

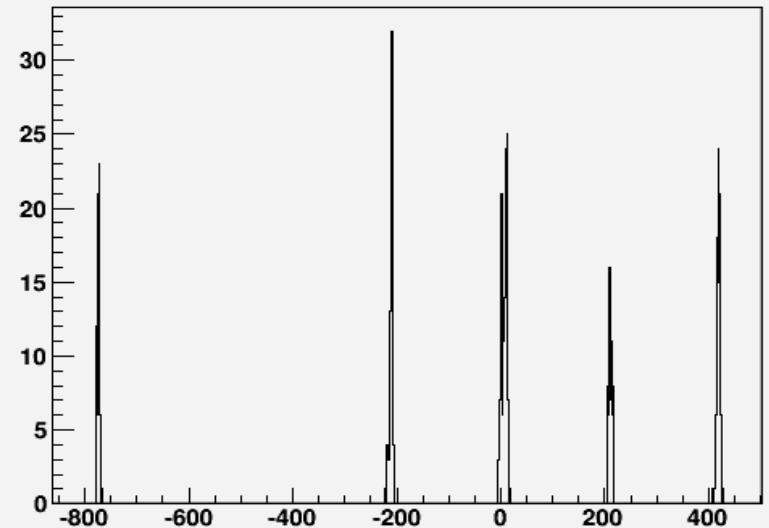
AOUT1: 240Ω

AOUT2 : 240Ω

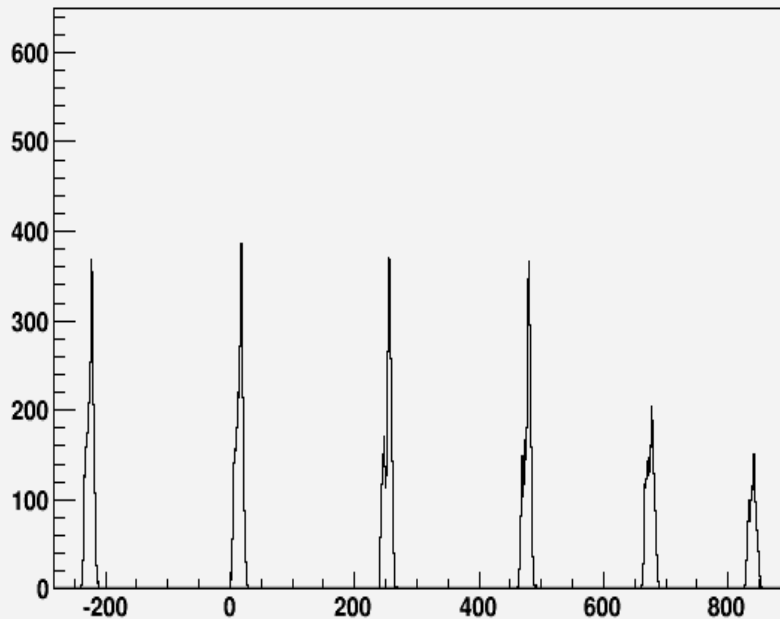
AddressLevels_C3



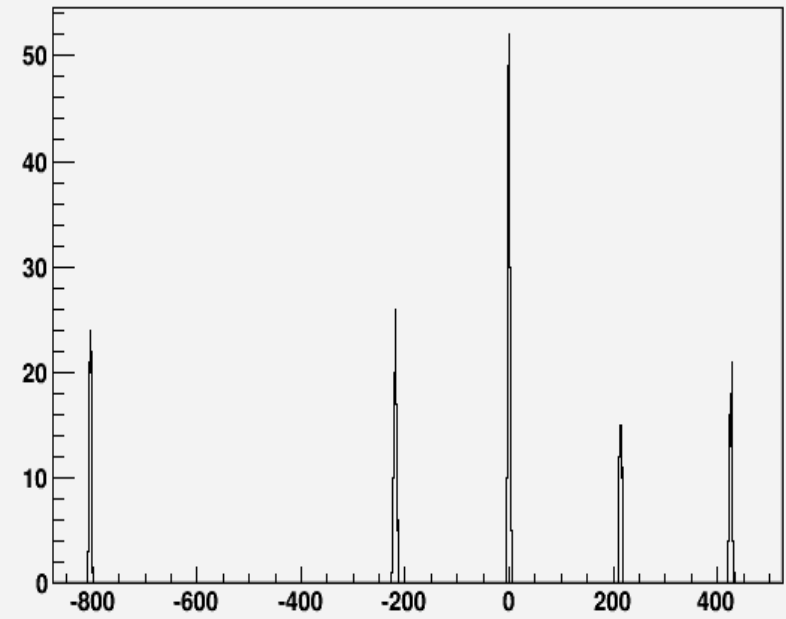
TBMAddressLevels



AddressLevels_C3



TBMAddressLevels



R_{TERM}

Mod-side

SDA_IN: 180Ω

CTR: 180Ω

CLK: 180Ω

Adapter-side

SDA_O: 270Ω

AOUT1: 270Ω

AOUT2 : 270Ω

1.0 m cables

R_{TERM}

Mod-side

SDA_IN: 180Ω

CTR: 180Ω

CLK: 180Ω

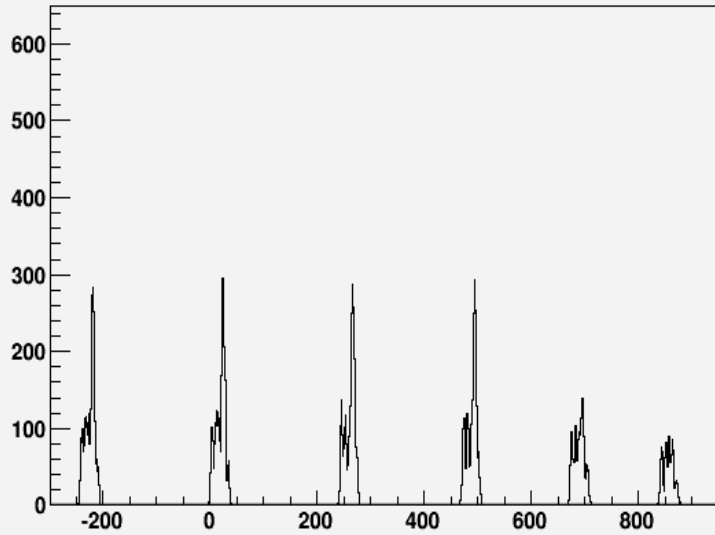
Adapter-side

SDA_O: 300Ω

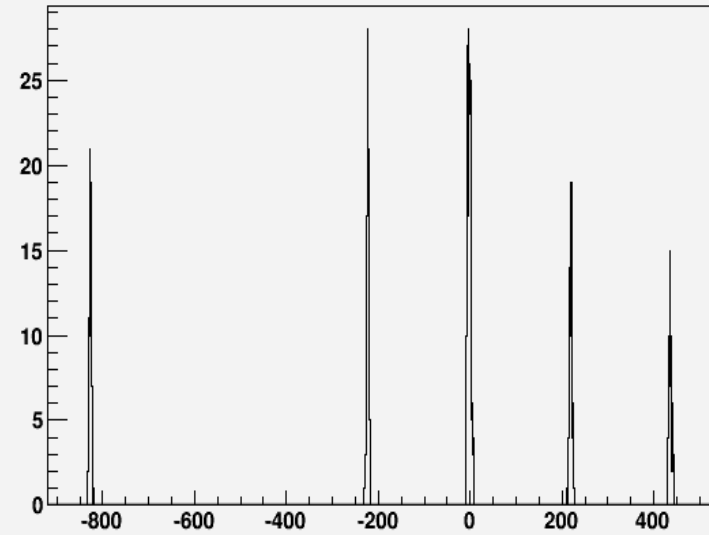
AOUT1: 300Ω

AOUT2 : 300Ω

AddressLevels_C3



TBMAddressLevels



1.5 m cables

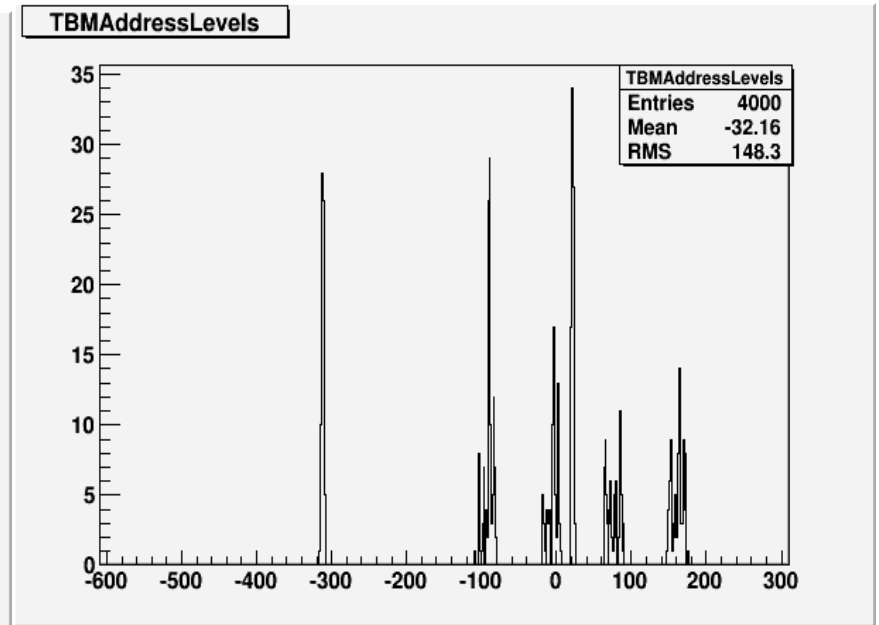
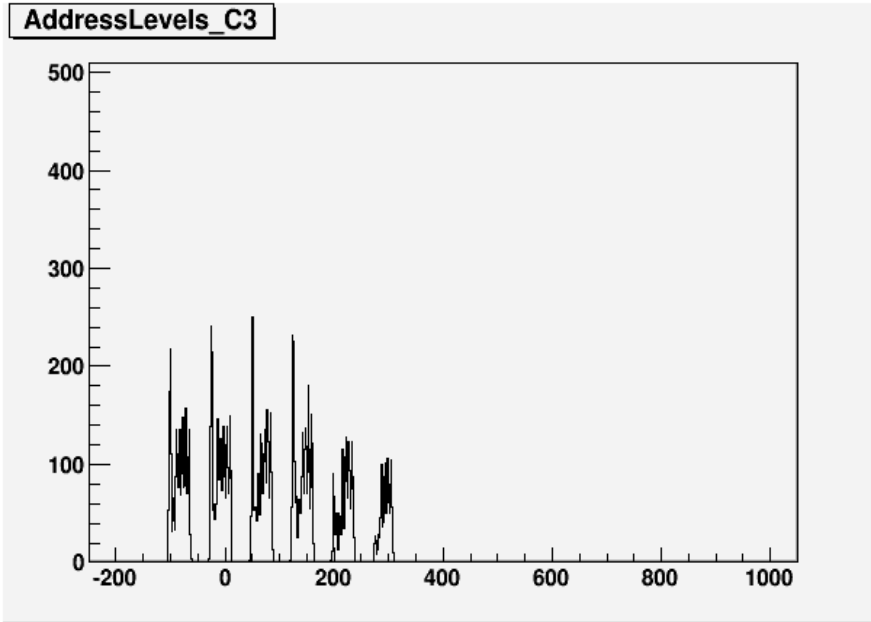
R_{TERM}

Mod-side

SDA_IN: 180 Ω
CTR: 180 Ω
CLK: 180 Ω

Adapter-side

SDA_O: 110 Ω
AOUT1: 110 Ω
AOUT2 : 110 Ω



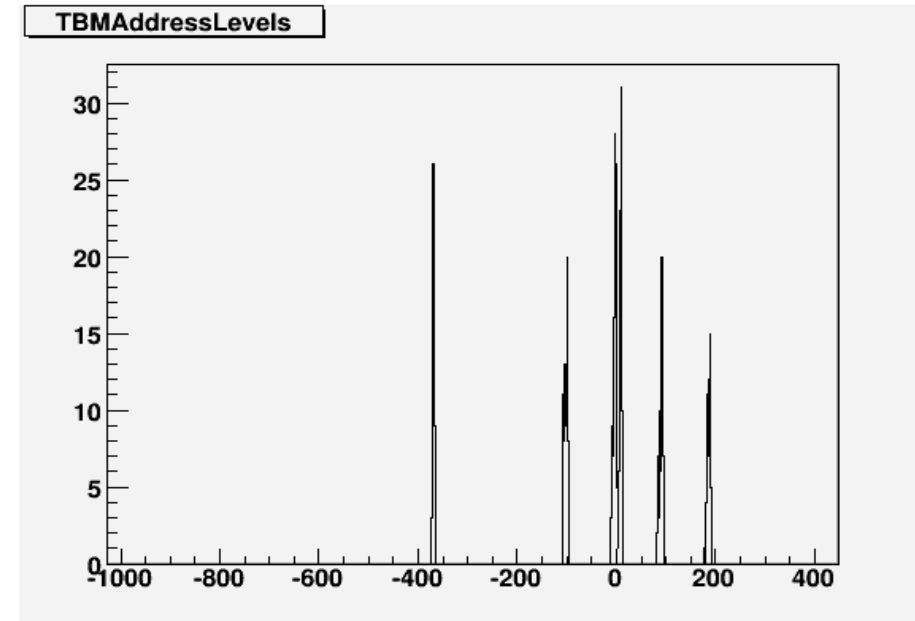
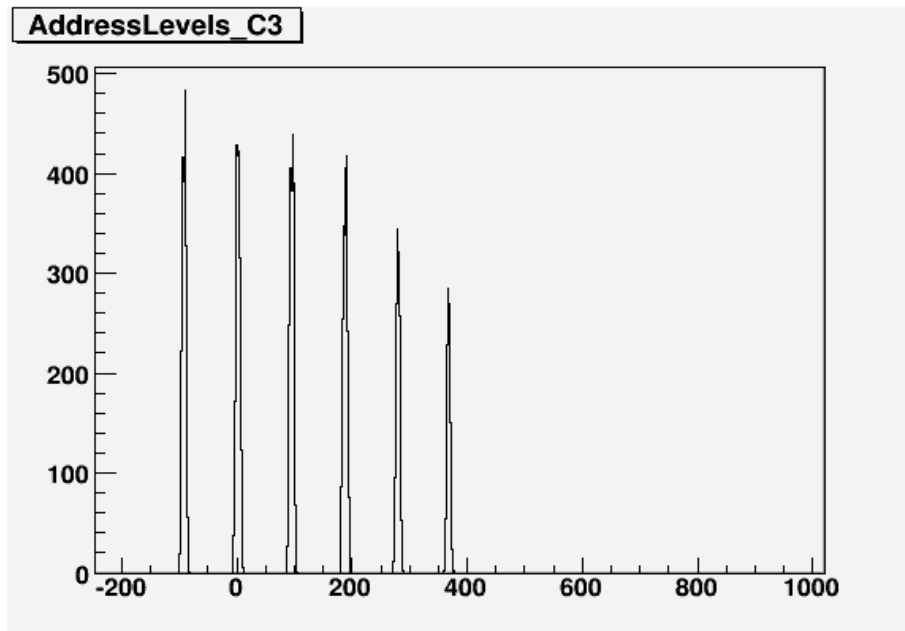
R_{TERM}

Mod-side

SDA_IN: 180 Ω
CTR: 180 Ω
CLK: 180 Ω

Adapter-side

SDA_O: 160 Ω
AOUT1: 160 Ω
AOUT2 : 160 Ω



1.5 m cables

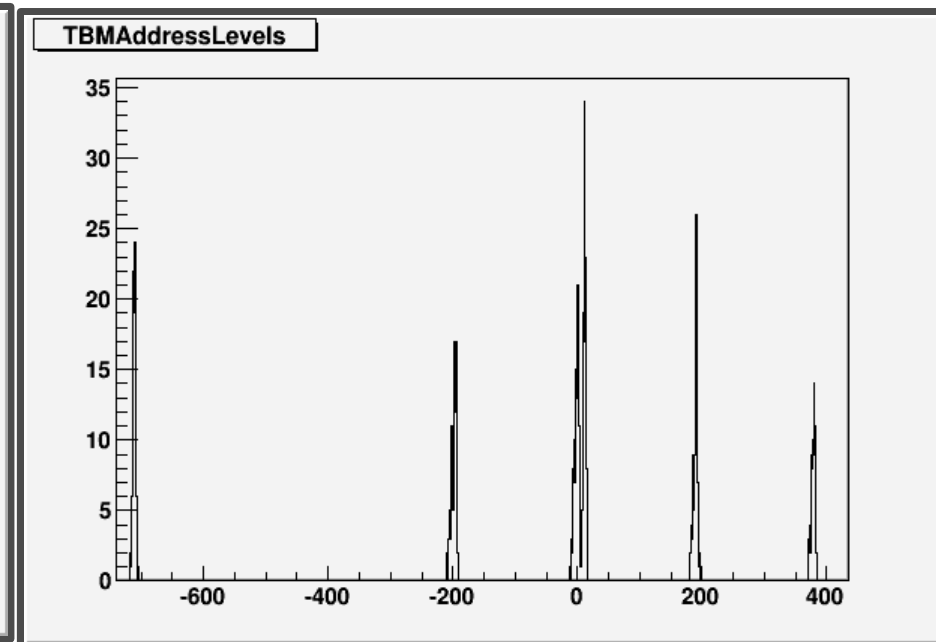
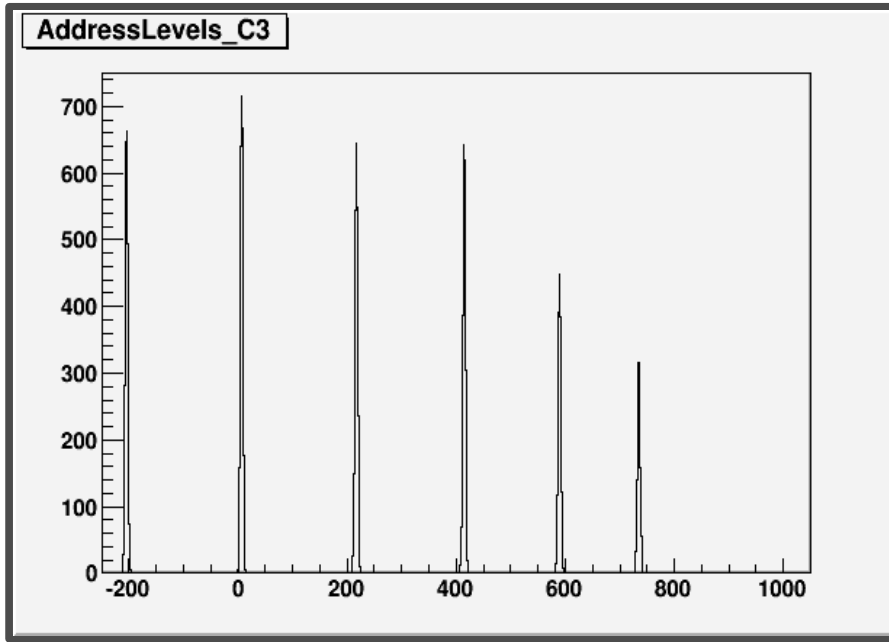
R_{TERM}

Mod-side

SDA_IN: 180 Ω
CTR: 180 Ω
CLK: 180 Ω

Adapter-side

SDA_O: 180 Ω
AOUT1: 180 Ω
AOUT2 : 180 Ω



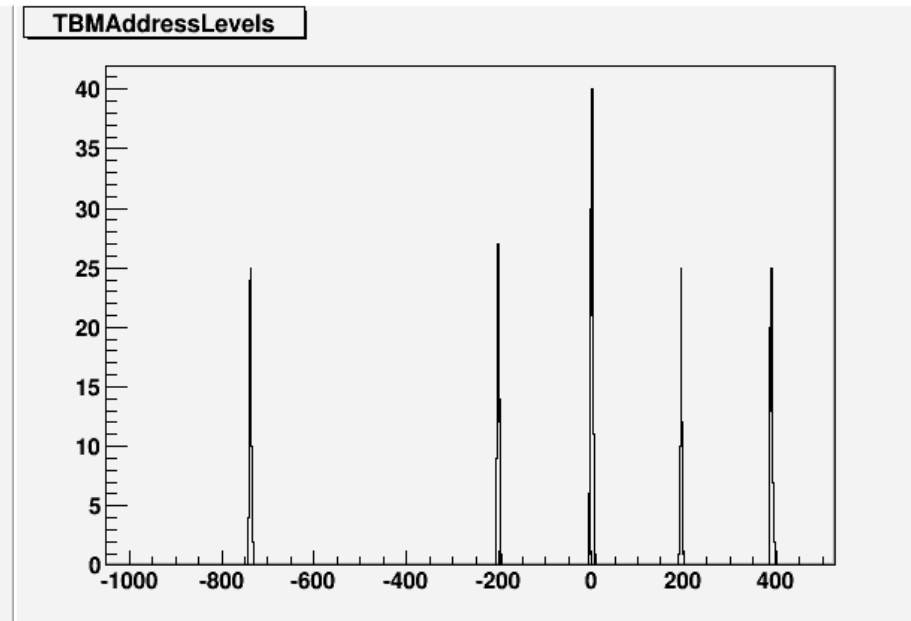
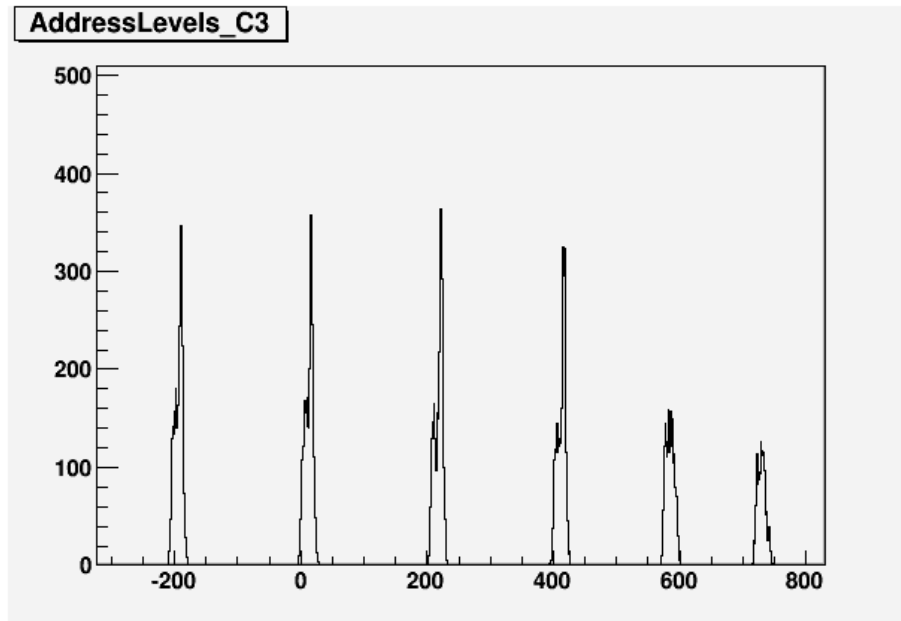
R_{TERM}

Mod-side

SDA_IN: 180 Ω
CTR: 180 Ω
CLK: 180 Ω

Adapter-side

SDA_O: 200 Ω
AOUT1: 200 Ω
AOUT2 : 200 Ω



1.5 m cables

R_{TERM}

Mod-side

SDA_IN: 180Ω

CTR: 180Ω

CLK: 180Ω

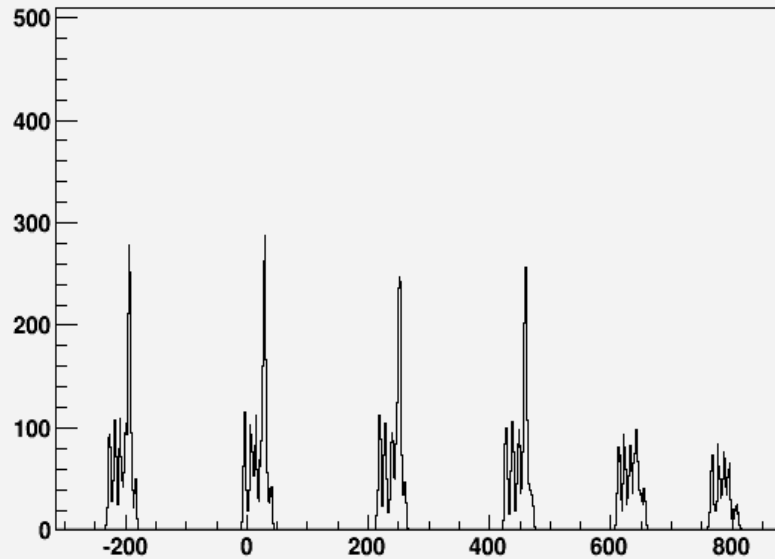
Adapter-side

SDA_O: 240Ω

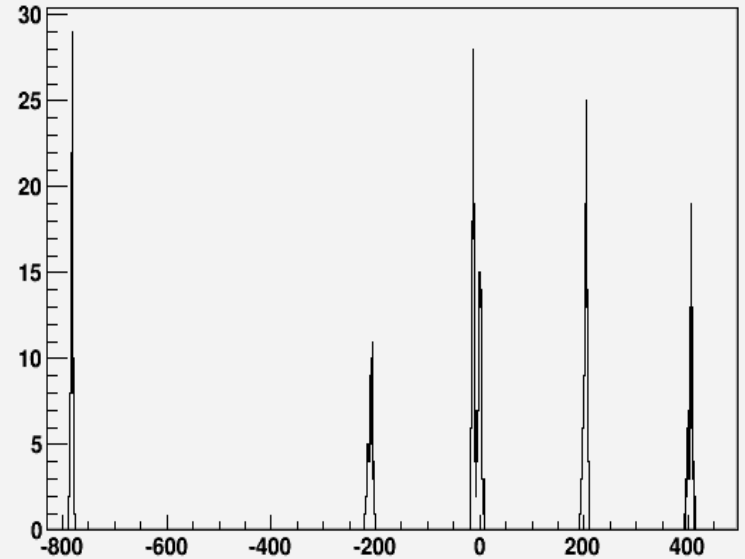
AOUT1: 240Ω

AOUT2 : 240Ω

AddressLevels_C3



TBMAddressLevels



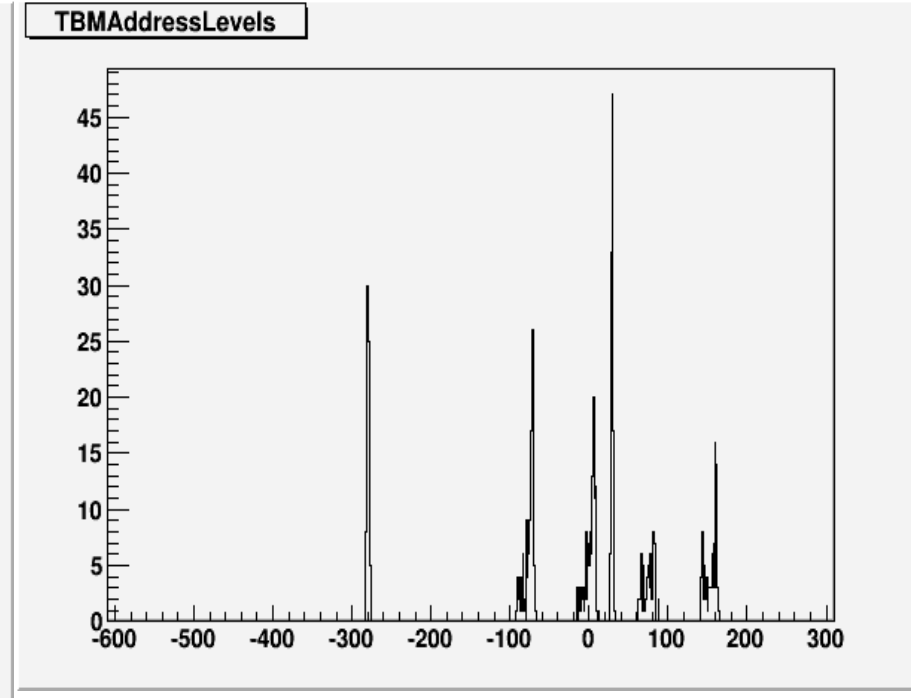
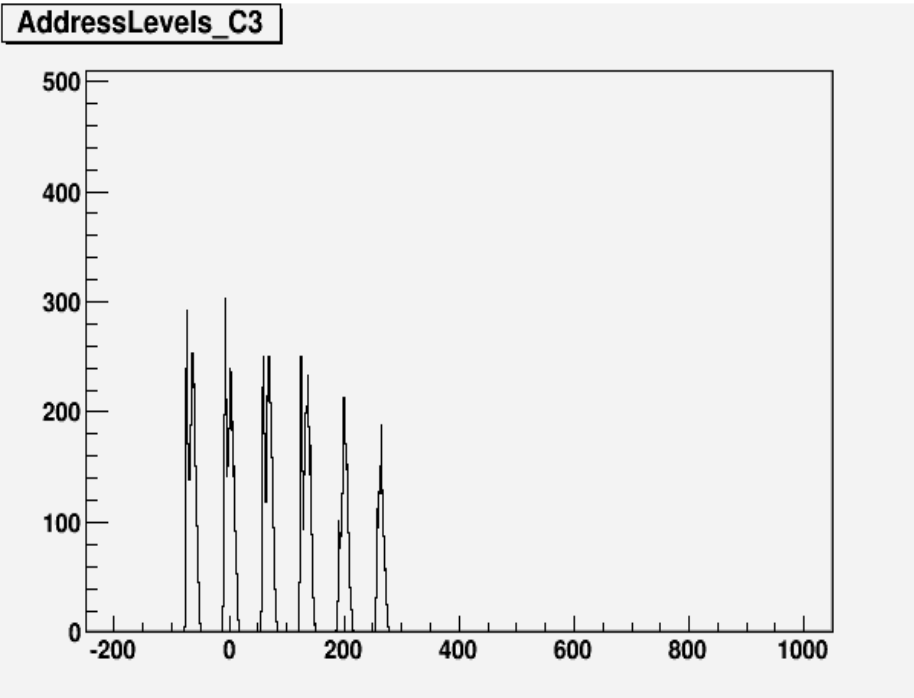
2m cables

Mod-side

SDA_IN: 180Ω
CTR: 180Ω
CLK: 180Ω

Adapter-side

SDA_O: 91Ω
AOUT1: 91Ω
AOUT2: 91Ω

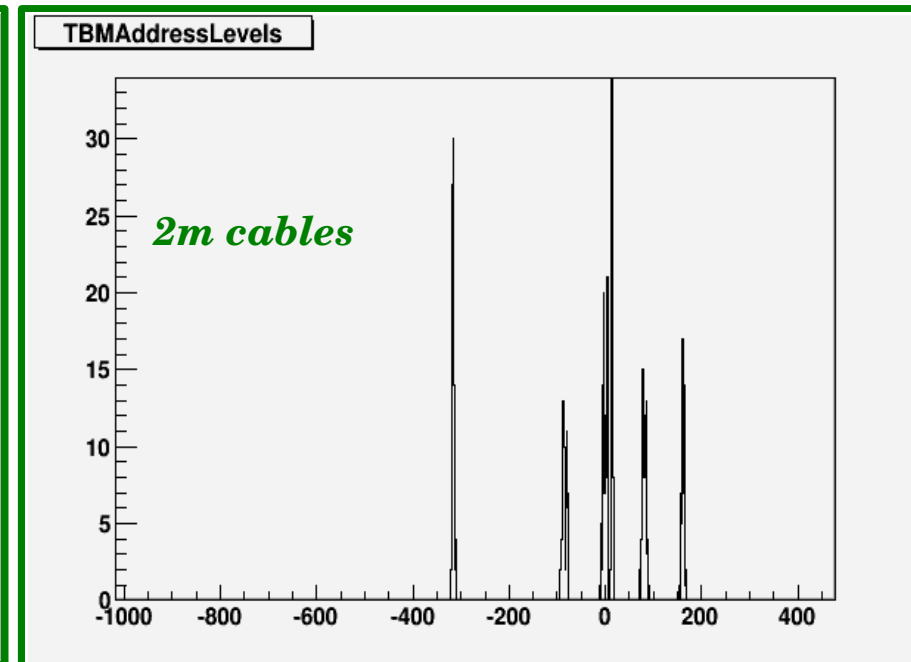
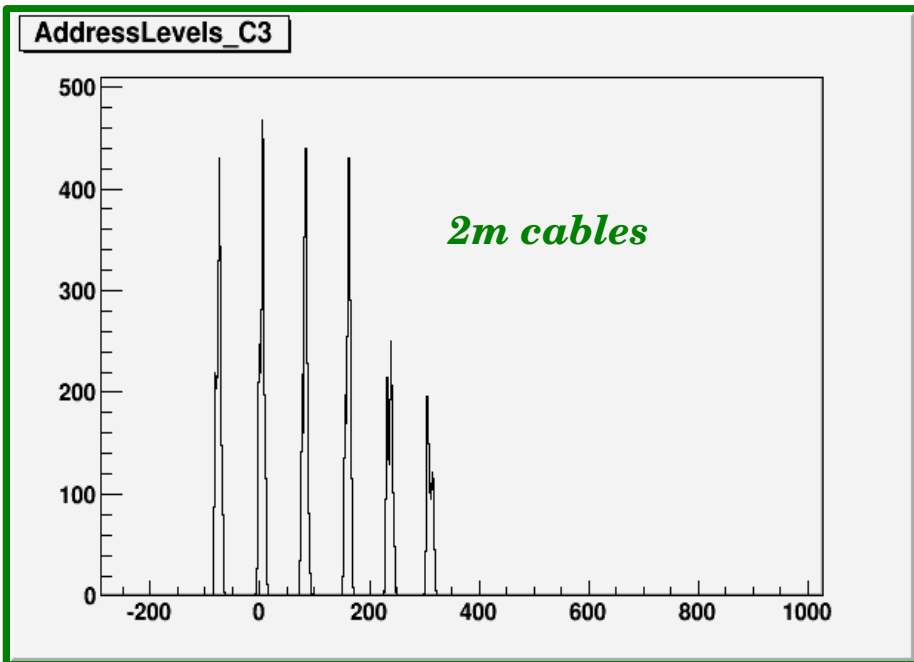


Mod-side

SDA_IN: 180Ω
CTR: 180Ω
CLK: 180Ω

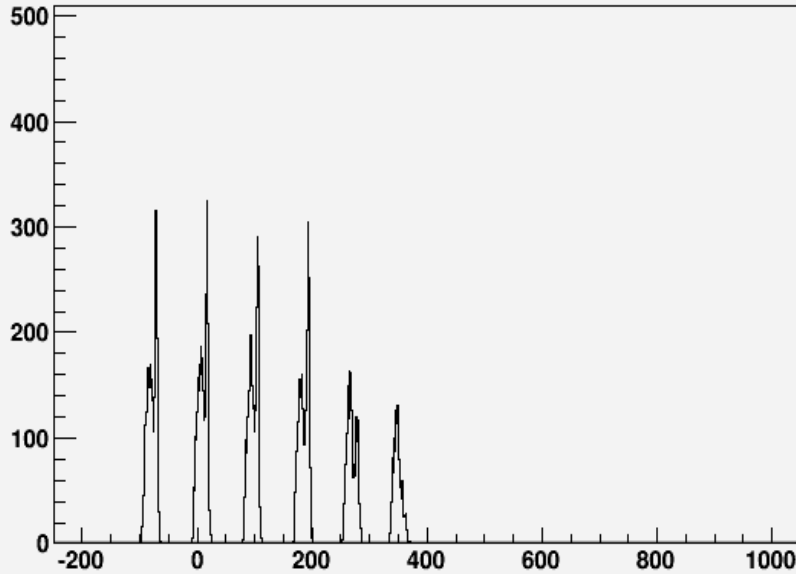
Adapter-side

SDA_O: 110Ω
AOUT1: 110Ω
AOUT2: 110Ω

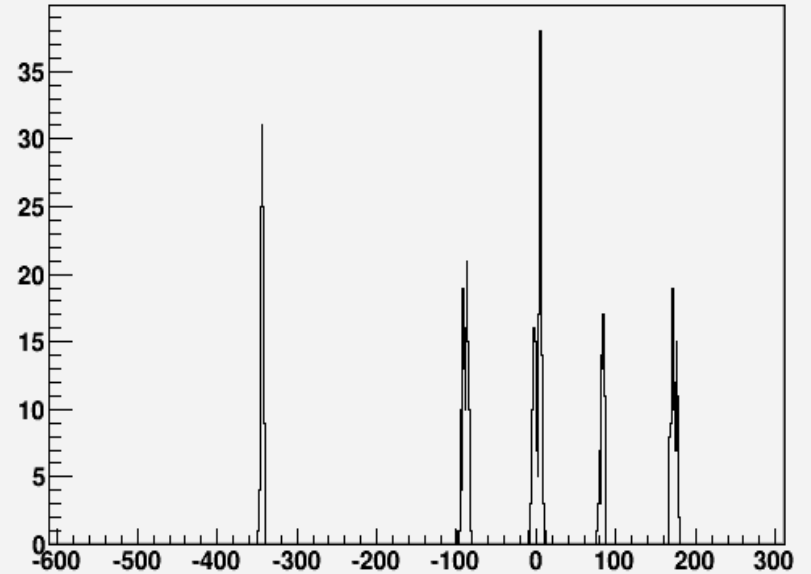


2m cables

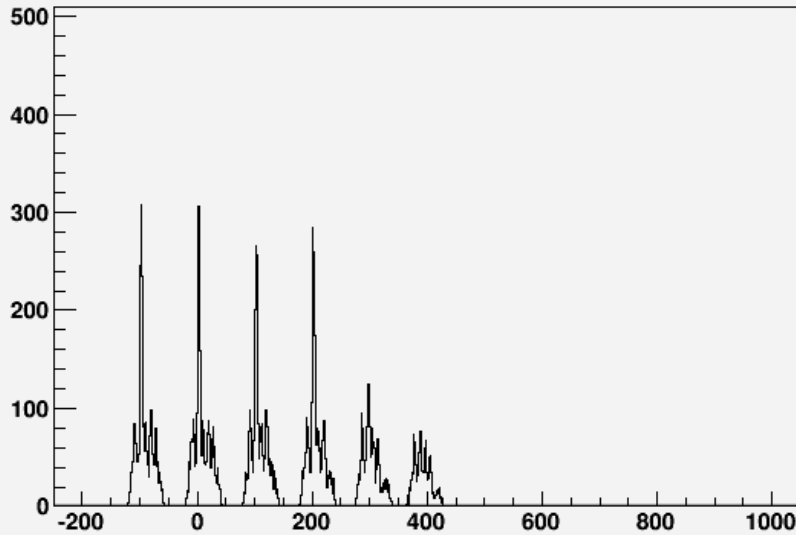
AddressLevels_C3



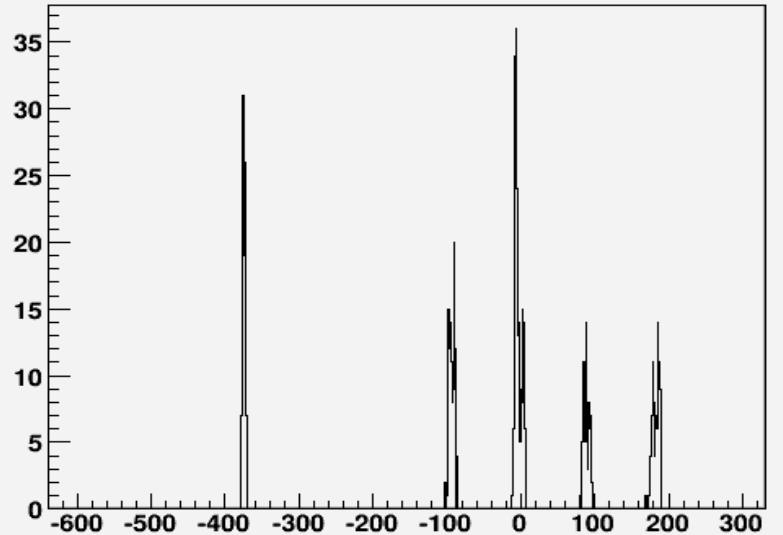
TBMAddressLevels



AddressLevels_C3



TBMAddressLevels



R_{TERM}

Mod-side

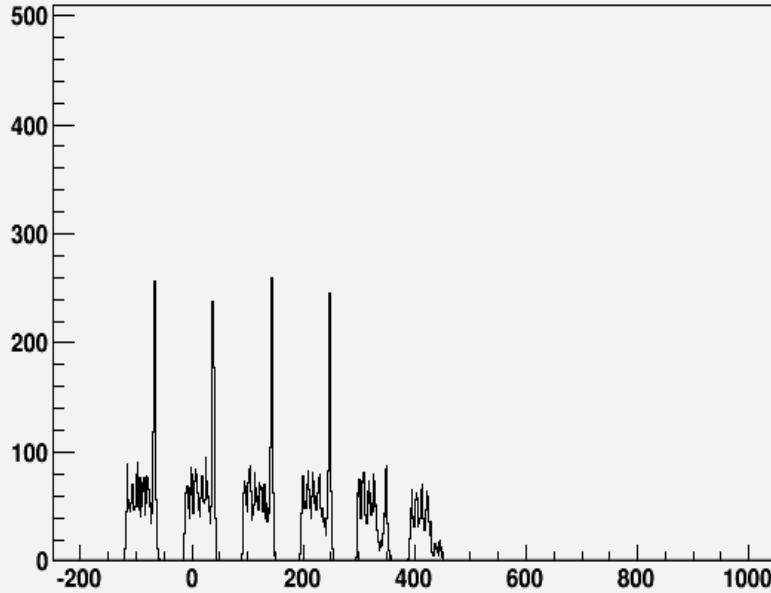
SDA_IN: 180 Ω
CTR: 180 Ω
CLK: 180 Ω

Adapter-side

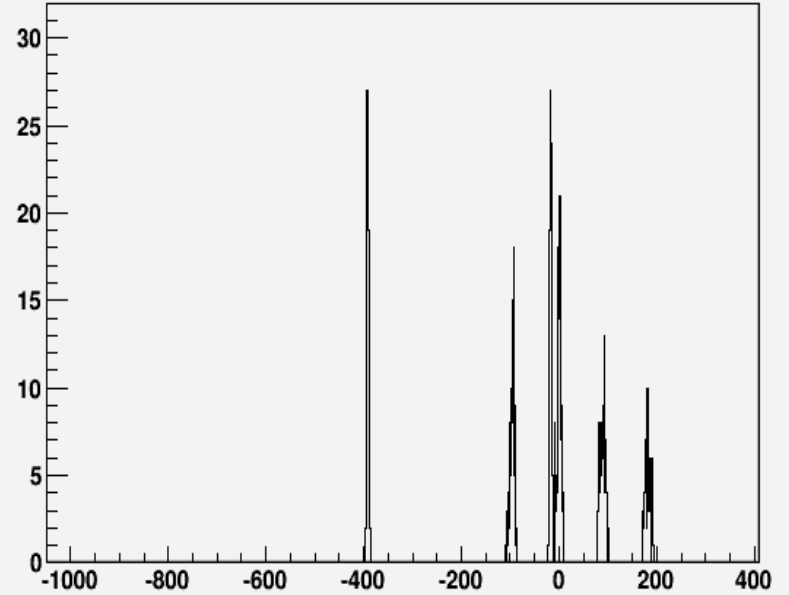
SDA_O: 160 Ω
AOUT1: 160 Ω
AOUT2 : 160 Ω

2m cables

AddressLevels_C3



TBMAddressLevels



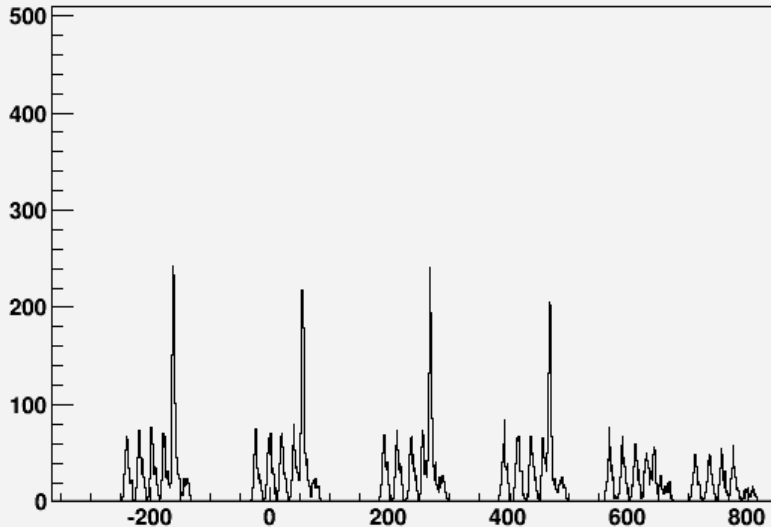
Mod-side

SDA_IN: 180Ω
CTR: 180Ω
CLK: 180Ω

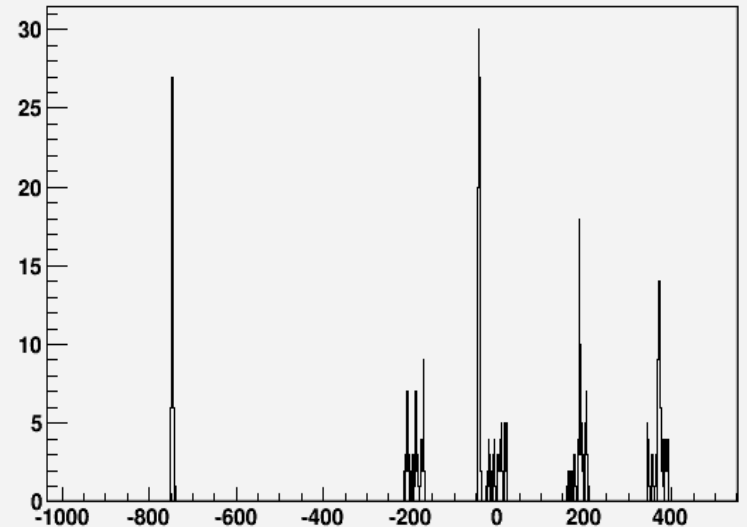
Adapter-side

SDA_O: 180Ω
AOUT1: 180Ω
AOUT2: 180Ω

AddressLevels_C3



TBMAddressLevels



Mod-side

SDA_IN: 180Ω
CTR: 180Ω
CLK: 180Ω

Adapter-side

SDA_O: 200Ω
AOUT1: 200Ω
AOUT2: 200Ω

2m cables

Mod-side

SDA_IN: 180Ω
CTR: 180Ω
CLK: 180Ω

Adapter-side

SDA_O: 240Ω
AOUT1: 240Ω
AOUT2 : 240Ω

