Interpixel Capacitance Measurements

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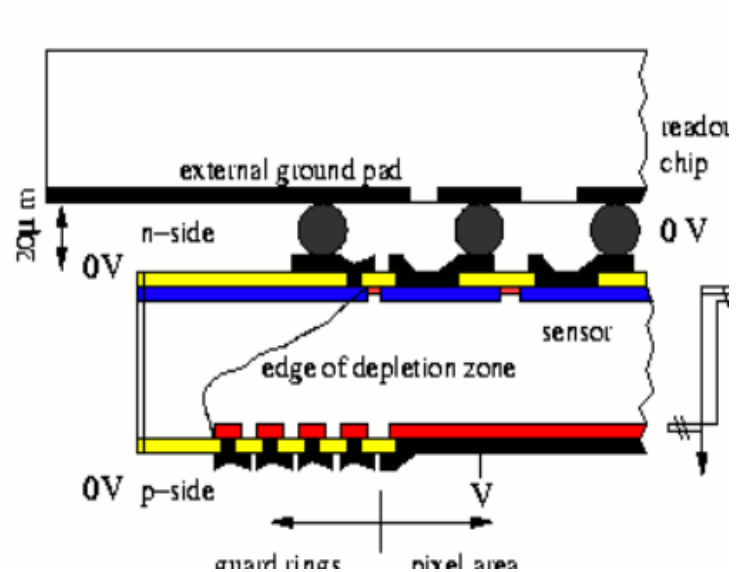
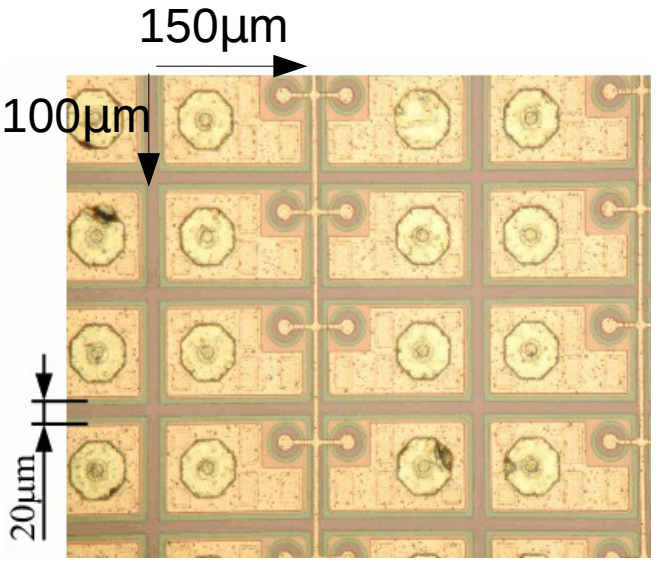
Present barrel sensor characteristics:

Implants	n+/n
pixel implants	150x100µm pixel
interpix isolation	p-spray (uniform medium dose of p impurities covers the whole structure)
Gap	20 µm (distance between pixel implants)
Si crystal	<111>
Si substrate	DOFZ (standard FZ material enriched with oxygen on wafer)
bulk resistivity	3.7 KΩcm
thickness	285 µm
back side	p+ layer and guard rings





Motivation:

The sensor pitch (is fixed) --> spatial resolution
The implant width --> capacitance between neighboring pixels

- contributes to the noise in the pixel preamplifier
  lower cap. --> lower noise
- contributes to the analogue current I_{ana}
  for a given peaking time lower cap. --> lower I_{ana}

Early Studies at PSI on R&D structures --> an increase of Gap from 20 to 30 µm leads to a capacitance decrease of ~20%

Barrel sensor group strategy for the Phase I Upgrade is to stay with the present sensor geometry, characteristics and vendor **eventually change the gap size from 20->30 µm**

Plan of the current study:

1) The sample: single barrel chips with different Gap design (from test structures on the same wafer of barrel sensor production)

2) Fan out mask for interpixel capacitance measurements: designed by Jennifer in April 09 produced end May 09

3) First measurements on a small sample (20chips) of capacitance, conductance, leakage current before and after irradiation with a Co60 at 17KGy (Asma July 09, Tilman in August 09)

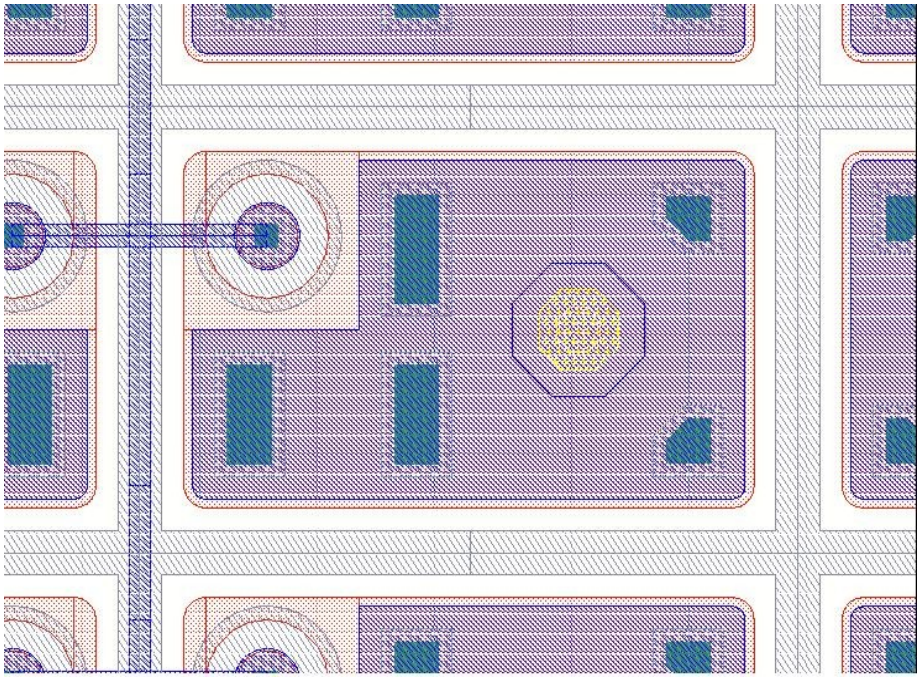
4) Scurve-Noise and Pulse Shape rising time measurements on single chip +ROC (myself and Jennifer Sept. 09)

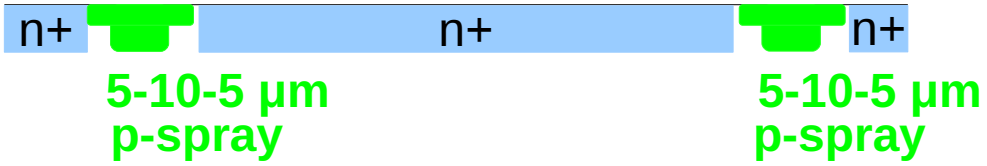
5) Simulation with the Synopsis-TCAD package (Jennifer and maybe 1 PIRE stud. help her during Summer)

6) Plan to have some Fpix chips (p-stop technique: high dose p+ implant ring around each pixel) and 3D sensor.

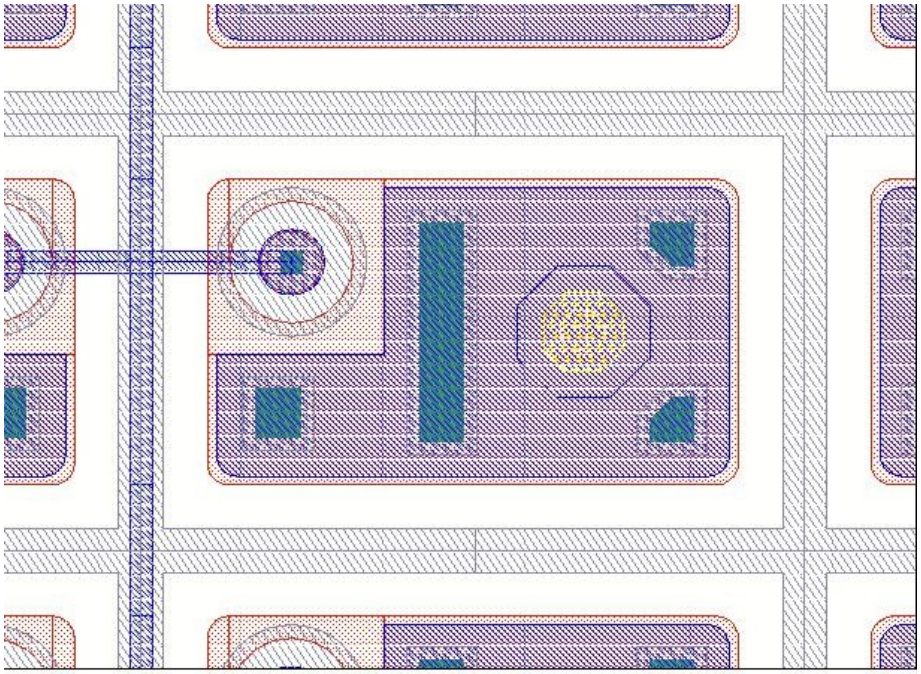
The sample:

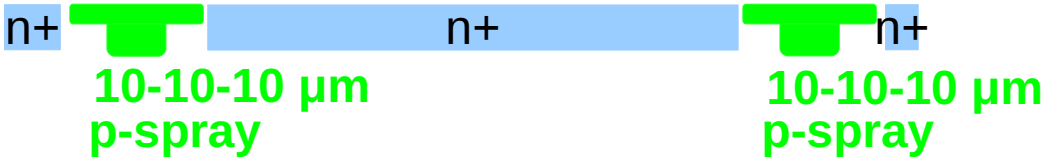
Gap 20 or Dot 1





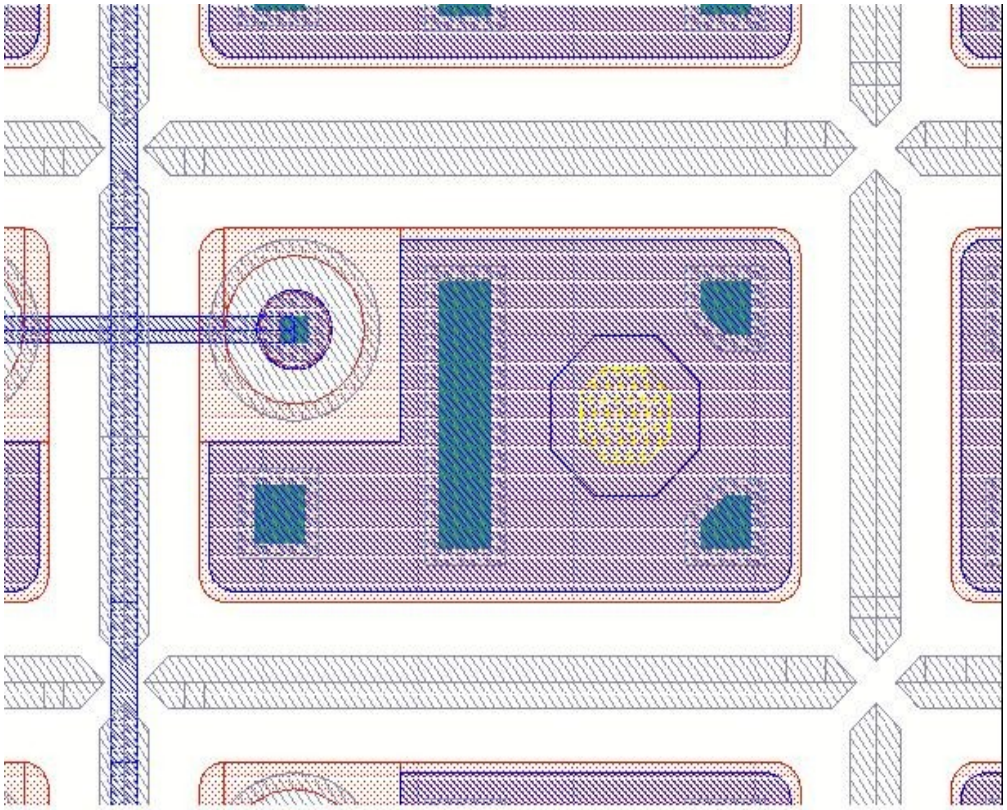
Gap 30





The sample:

Gap 30 - 2

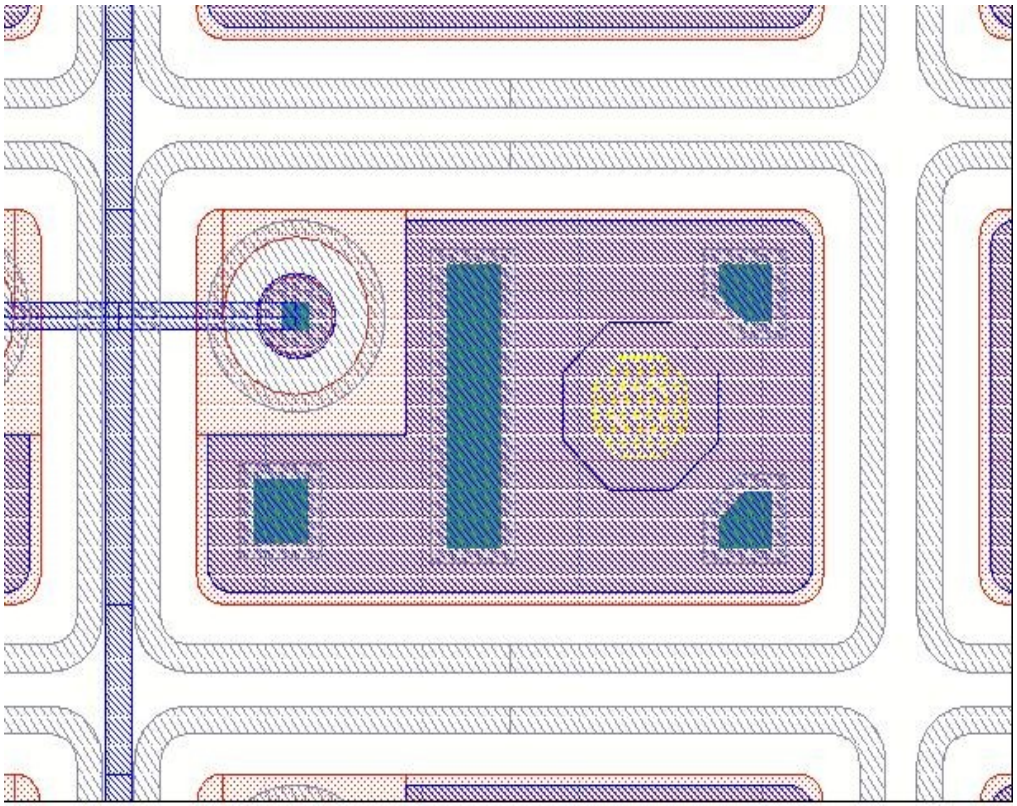


n+ n+ n+

10-10-10 µm p-spray

10-10-10 µm p-spray

Gap 30 - 3



n+ n+ n+

5-7-6-7-5 µm p-spray

5-7-6-7-5 p-spray

Fan out mask:

Interpixel Capacitance measurements:

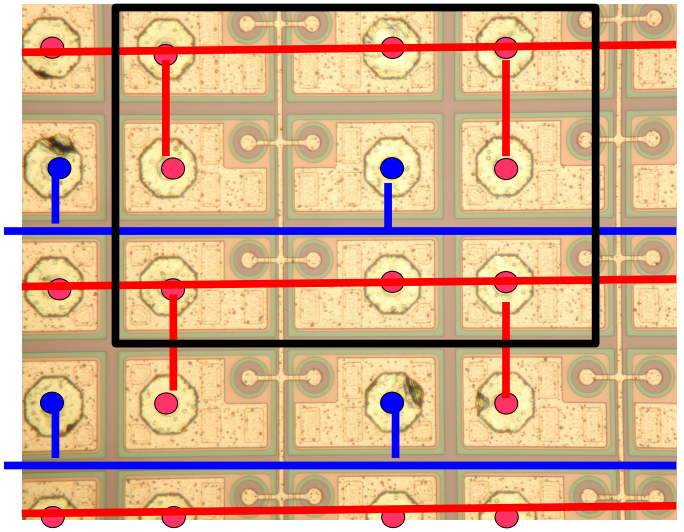
fan out mask simple technology 3 layers: (metal, passivation, bumps)

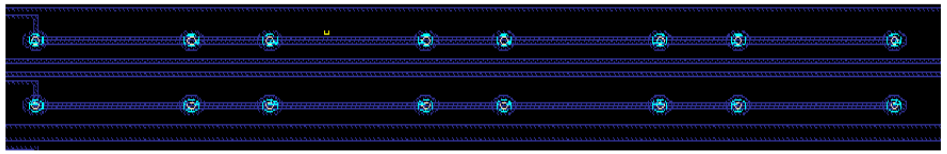
1 pixel (blue) surrounded by 8 neighbors (red)

Cmeasured = Σ Cinter-pixel + Cstray

= (# blue pixels) * Cinter-pixel + Cstray

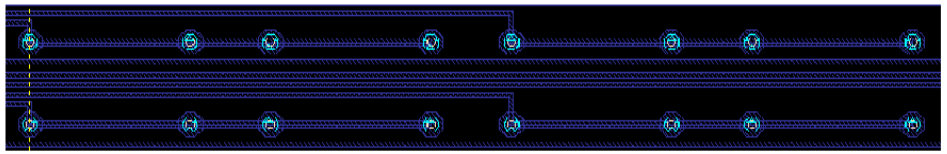
Cstray is the cap of the readout structure, bond wires...



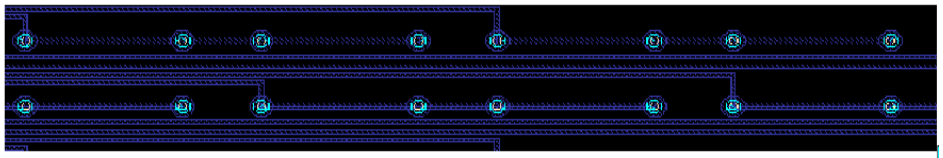


8 pixels connected, parallel

Macropixel structures: for Phase II



4 pixels connected, parallel



4 pixels connected, offset

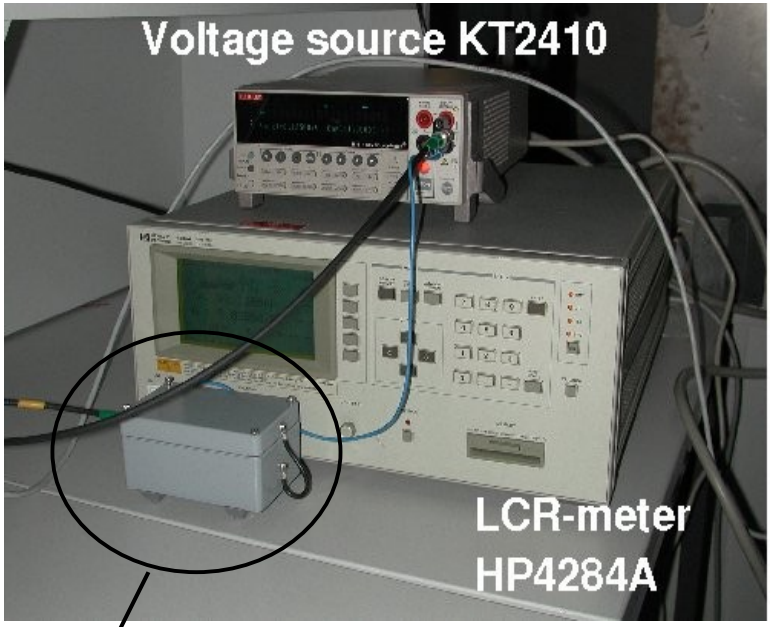
4 or 8 pixels connected together and routed to a wire bond pad

Bond pattern fits to strip APV hybrids pitch (by Alan Honma)

Also “bricked” pattern, macropixel lenghts proposed for the Strawman A for **Phase II**

Measurement setup and procedure:

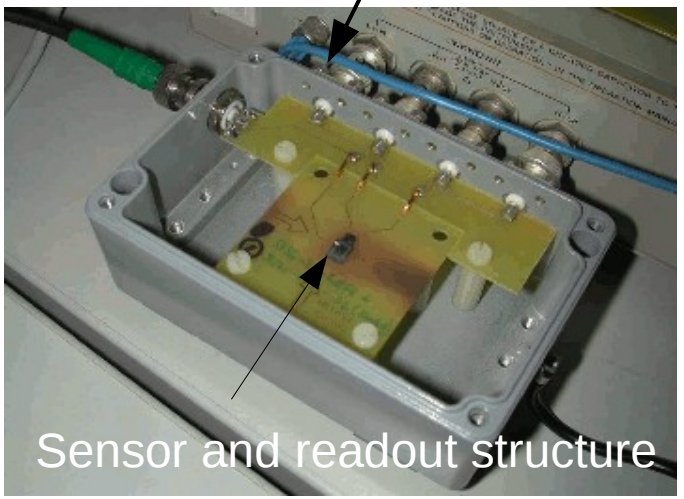
Capacitance measurements set up (F. Bechtel and T. Rohe)



- Single chip sensors are bumpbonded to a “fan-out” chip
- The chip is glued on a vetronite support and wire bonded
- A small box, containing the chip, is connected to the LCR meter

- Signal level 100 mV
- Measurement frequencies 1 kHz, 10 kHz, 100 kHz
- Bias voltage 0 V – 500 V

1. Capacitance, conductance and leakage current on samples
2. Remeasured after Co60 irradiation @ 17KGray --> saturation of fixed surface oxide charge
3. The sensor is removed and stray capacitance measured



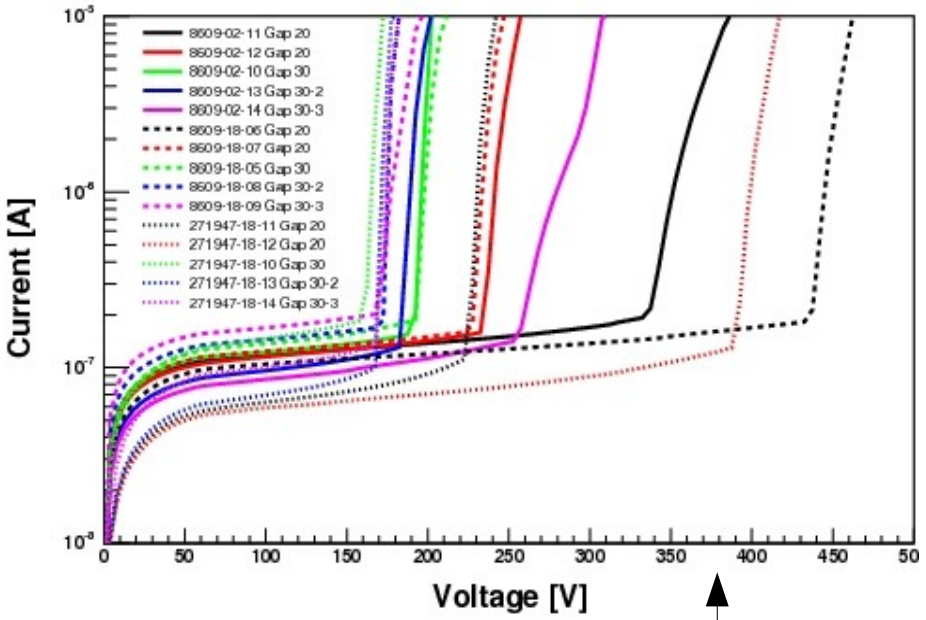
Results – Leakage Current:

- *larger gaps break down earlier*
- *Irradiation increases the surface currents (Co60 doesn't damage the bulk)*
- *Irradiation shifts break down to higher values*

Gap 30
Gap 30-2
Gap 30-3
Gap 20

8609-02
8609-02
271947-18

BEF. iRR

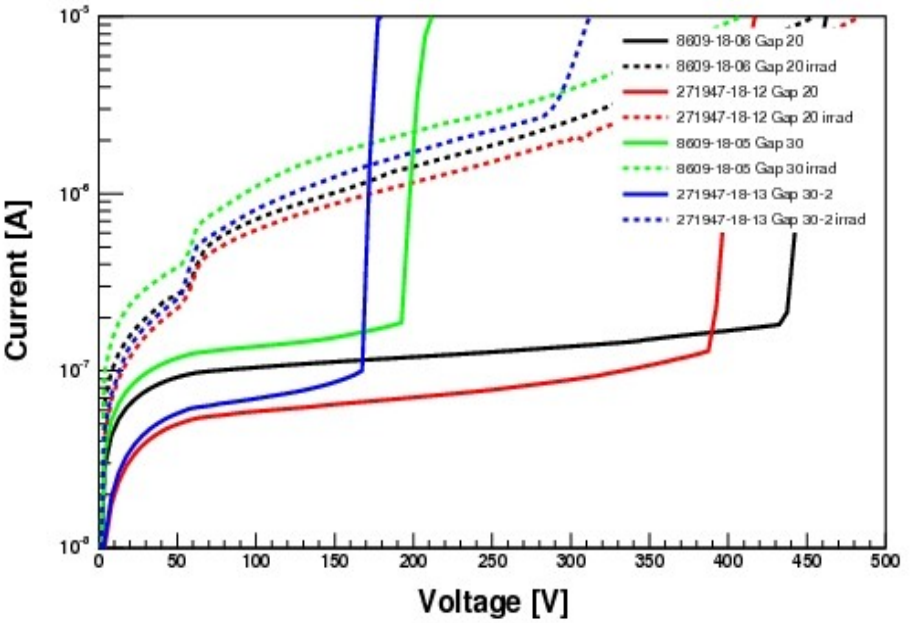


Full Depletion

Break Down

BEF-AFT. iRR

BEFORE
AFTER



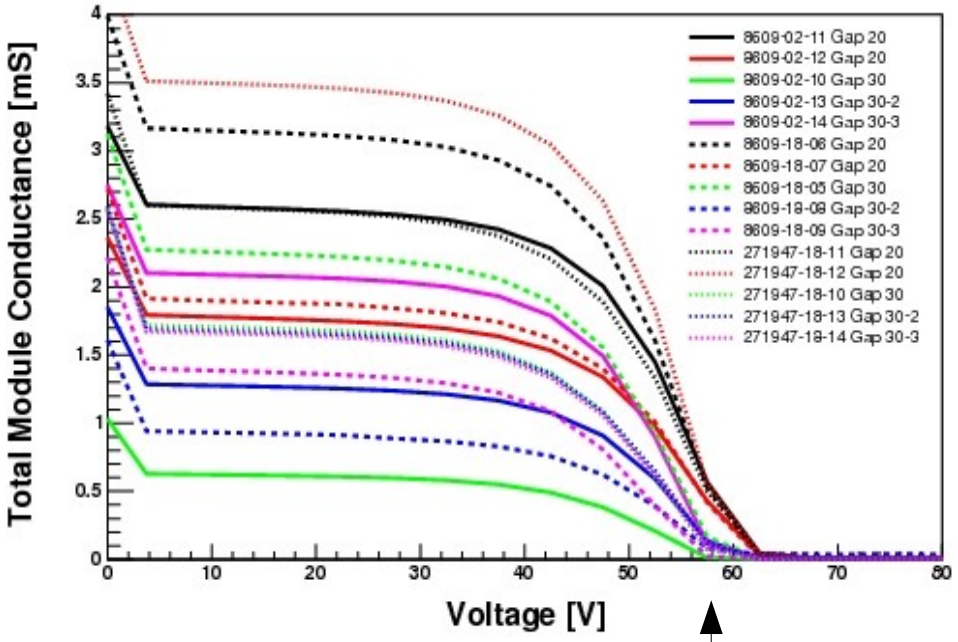
Results - Conductance:

- *The pixel isolation when full depletion is reached can be seen nicely*
- *No change with irradiation*

Gap 30
Gap 30-2
Gap 30-3
Gap 20

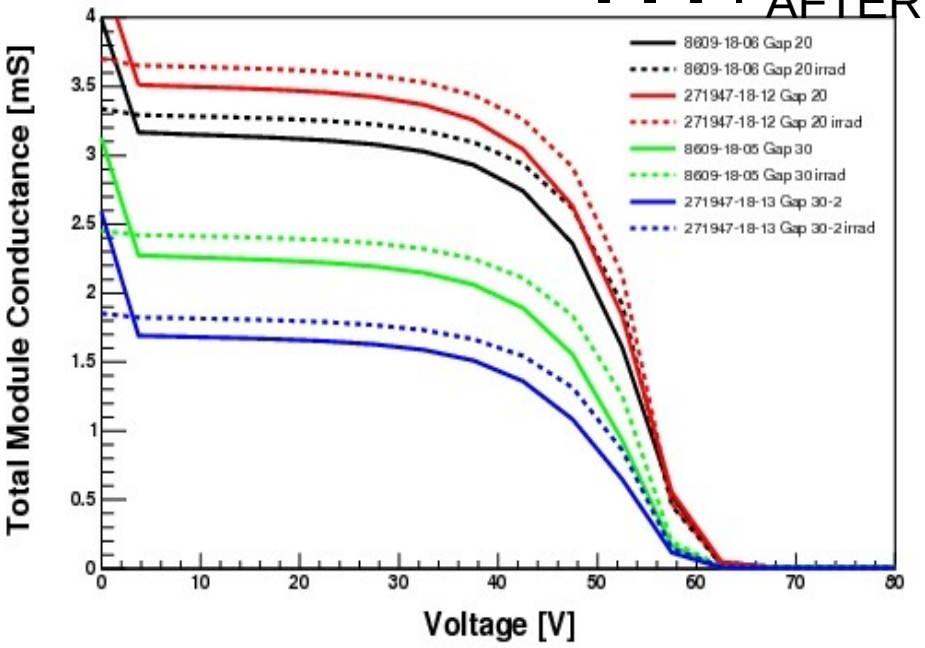
8609-02
8609-02
271947-18

BEF. iRR



BEF-AFT. iRR

BEFORE
AFTER



Full Depletion

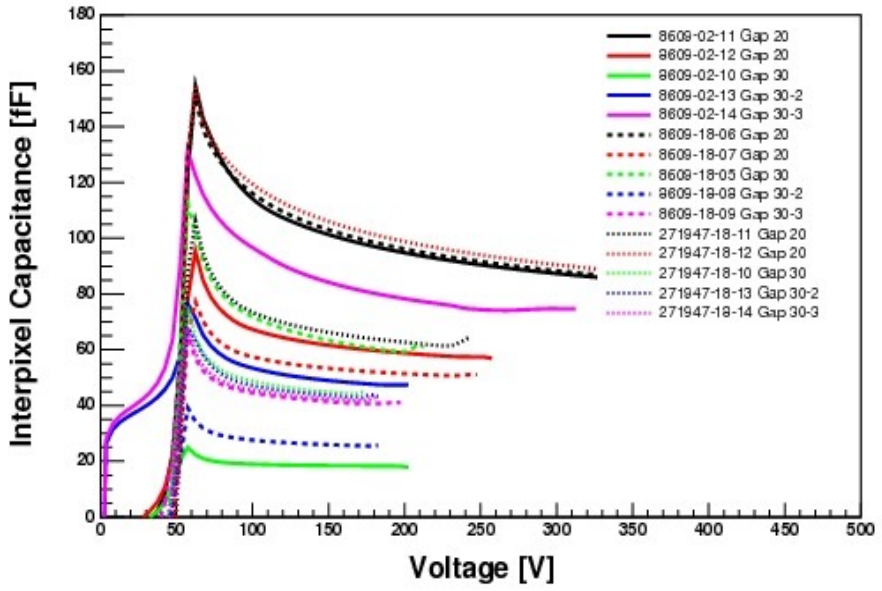
Results – Interpix Capacitance:

- *n+ pixels are isolated only @ $V_{bias} > V_{dep}$ (not type inv.)*
- *After V_{dep}, C_{int} decreases with bias voltage due to the steady depletion of the interpixel p-spray layer.*
- *Gap 30 show a lower value even if large spread!!!*
- *Irradiation makes C_{int} less voltage dependent (fixed interface charges deplete the p-spray layer already at low V_{bias})*

Gap 30
Gap 30-2
Gap 30-3
Gap 20

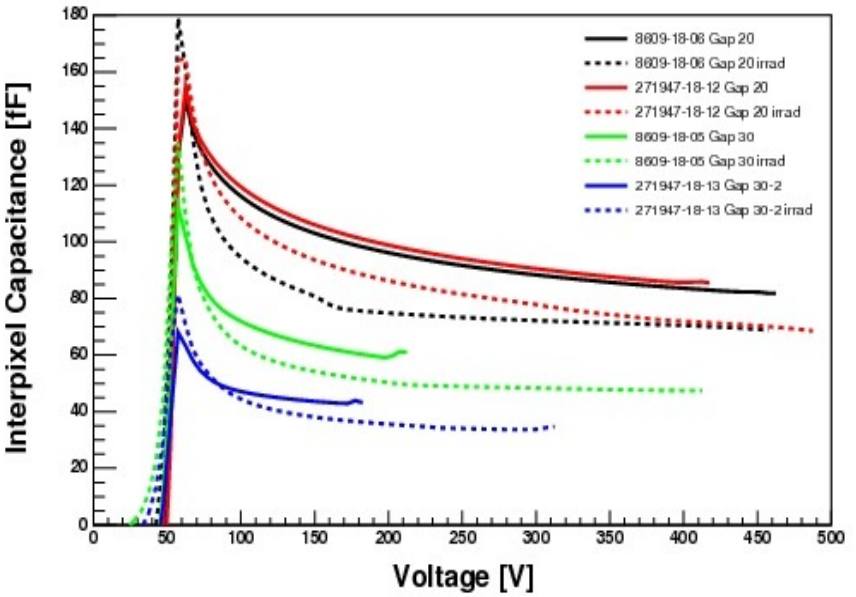
8609-02
8609-02
271947-18

BEF. iRR



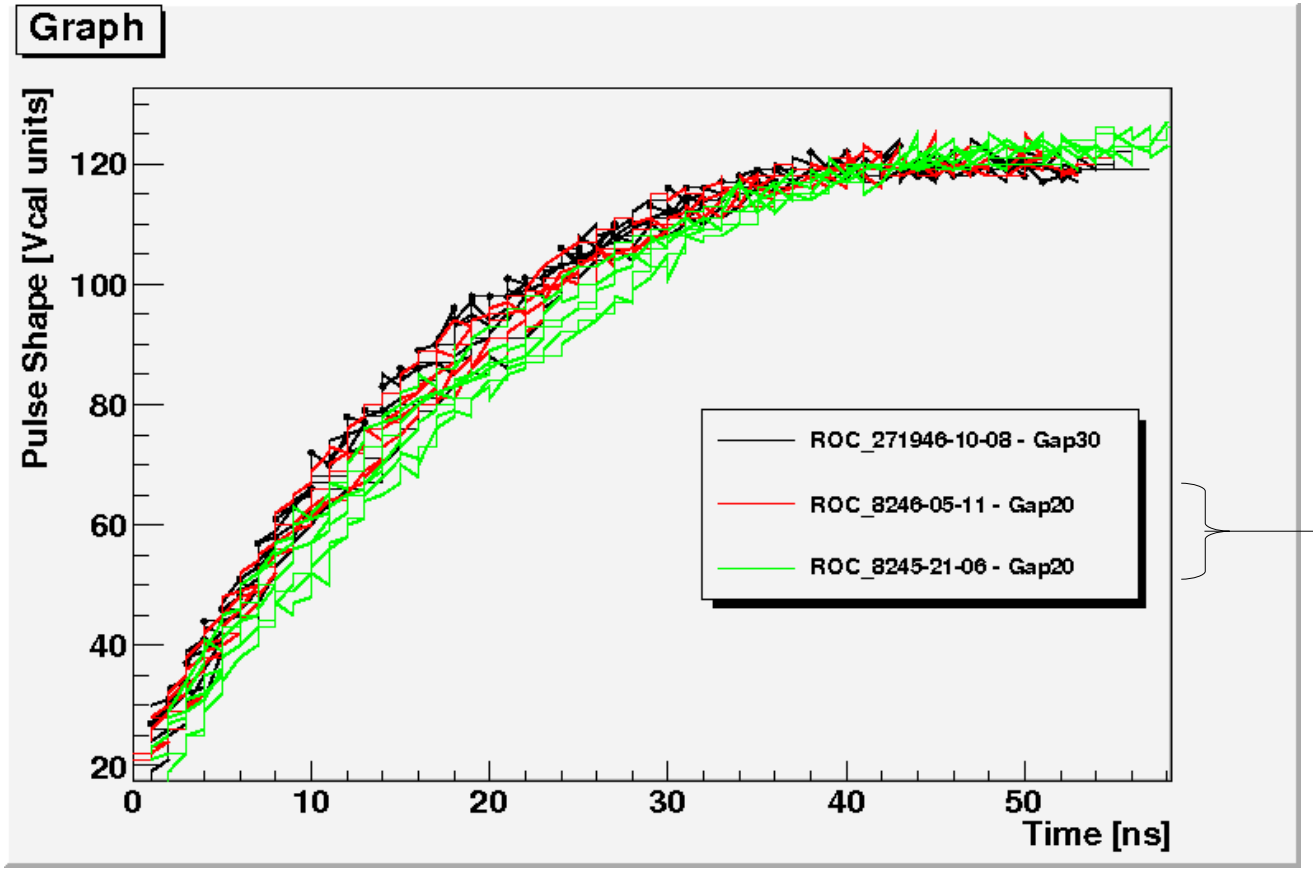
BEF-AFT. iRR

BEFORE
AFTER



Results – Pulse Shape (unirr.)

- *V_{ana} optimized by Pretest --> Analogue current to be 24mA*
- *No difference in the rising time between Gap30 and Gap20*



Two single chips sent to UIC!

Thanks to Samvel and Eric for providing the instructions and code to obtain the Pulse Shape.

Future plan

- make more samples

- measure the Noise (with the Scurve method) on chips with different design. Can we see any difference considering the accuracy of this measurements?

- measure the pulse shape (Samvel and Eric's procedure). Earlier simulations have shown a faster rising time of the signal in Gap 30s. Can we see this effect?

- simulate with the Synopsis-TCAD package the different designs evaluating the electric field, coupling/pixel capacitances...

- compare those results (measurements and simulations) with the one measured on the Fpix (pstop)

- we also asked for some 3D chips!