CMS Pixel Detector Upgrade: Analog to Digital Converter

Dane Oleson

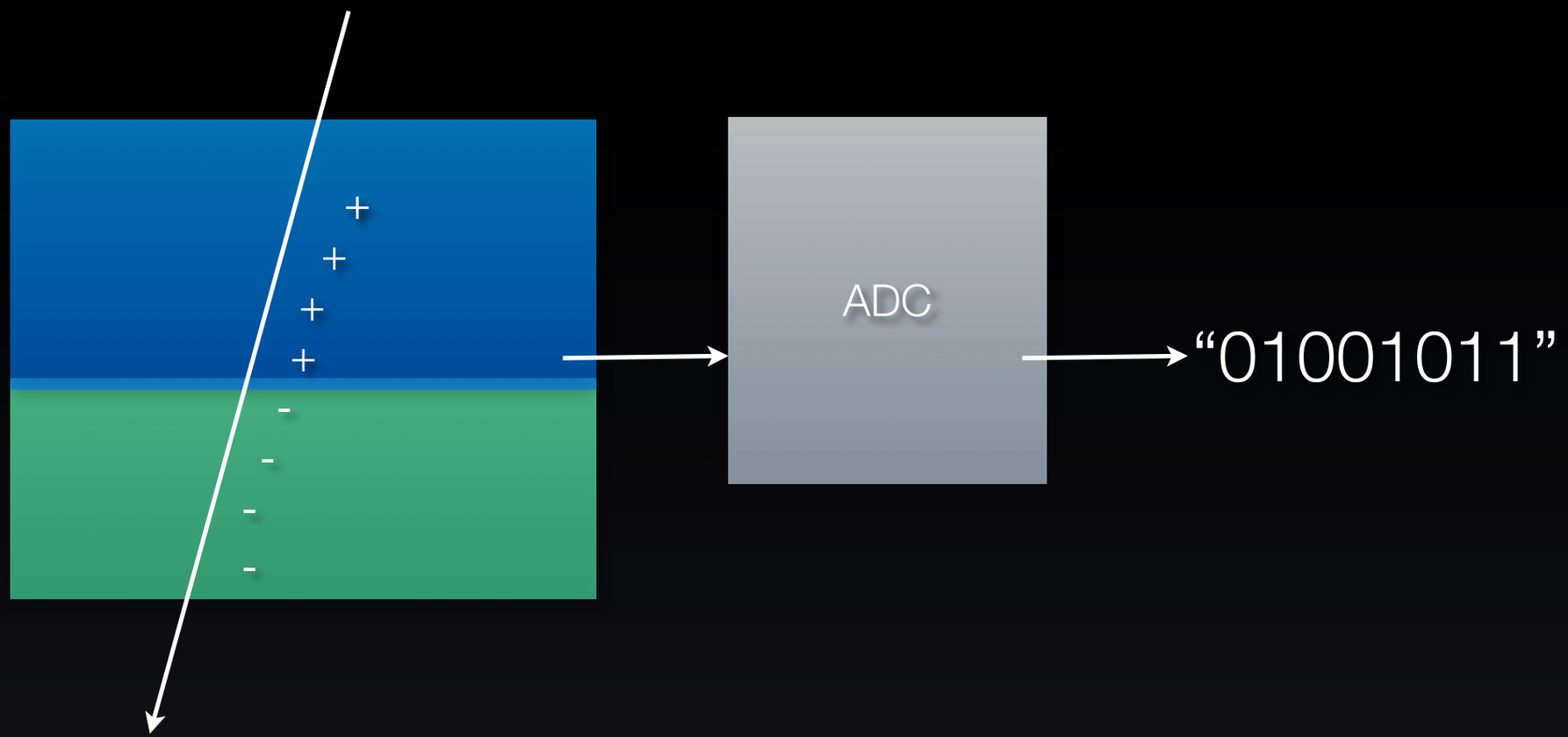
Questions to Answer:

- What is an ADC?
- Why use an ADC?
- What knowledge exists about the ADC?
- How do you test the ADC?
- What was discovered about the ADC this summer?

What is an ADC?

What is the ADC

- ADC stands for analog to digital converter. It converts liberated electrons (analog current) into a digital value based on the magnitude of the current. The ADC circuit will be used to send pulse-height information in a digital signal. The current chip sends pulse height as an analog signal. It is hoped that the digital signal will provide a faster transfer of data.
- The ADC is a clocked integrated circuit. Specifically, it uses a successive approximation method to find a digital value.



Charged Particle Ionizes Silicon
ADC Converts to “Computer Language”

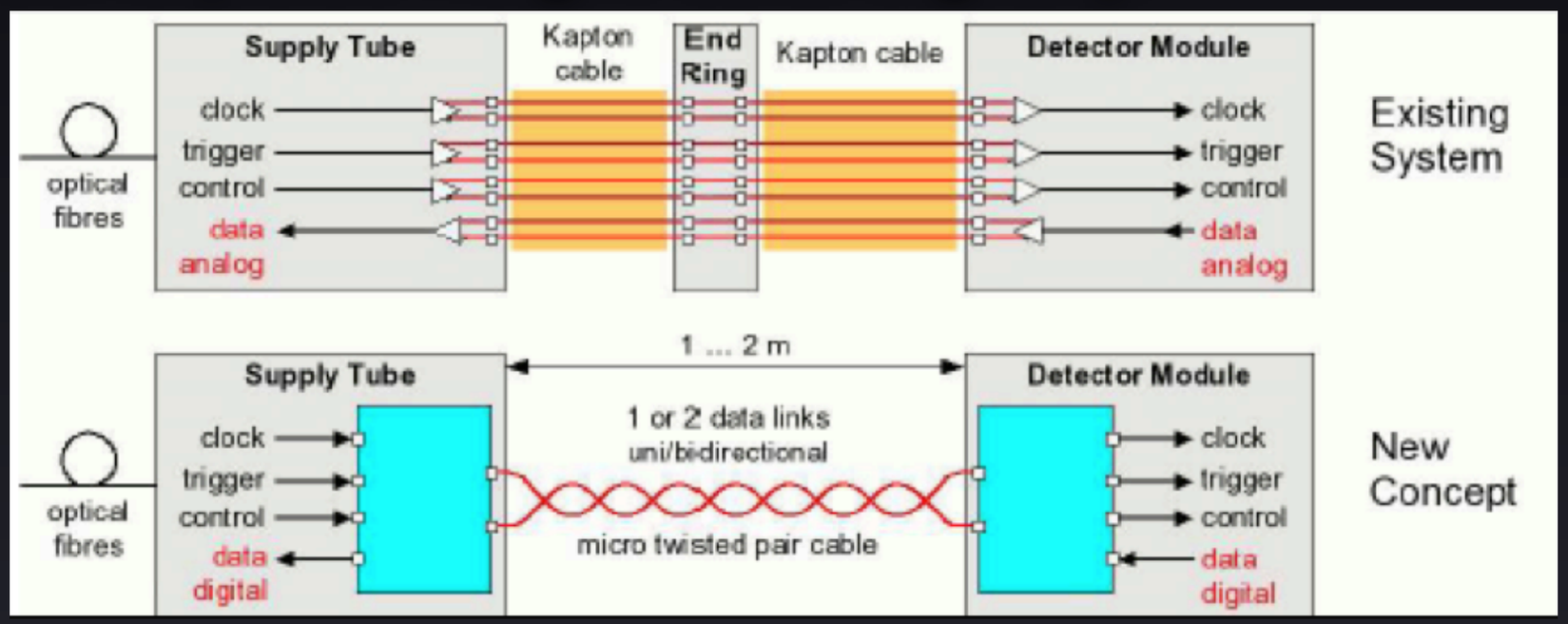
ADC Details

- Typical range of 0 to 80 microamps (4-bit), 0 to 120 microamps for 8-bit. (Based on reference current)
- Typical LSB (resolution) of 5 μA on 4-bit. (reference current)
- Typical LSB of 0.5 μA on 8-bit. (reference current)

Why use an ADC?

Motivation: SLHC

- The current detector will suffer radiation damage in coming years. New detector will be needed.
- Higher luminosity means increased rate of data collection.
- Need faster readout electronics. One way to do this is to send pulse height data digitally.



What knowledge exists about the ADC?

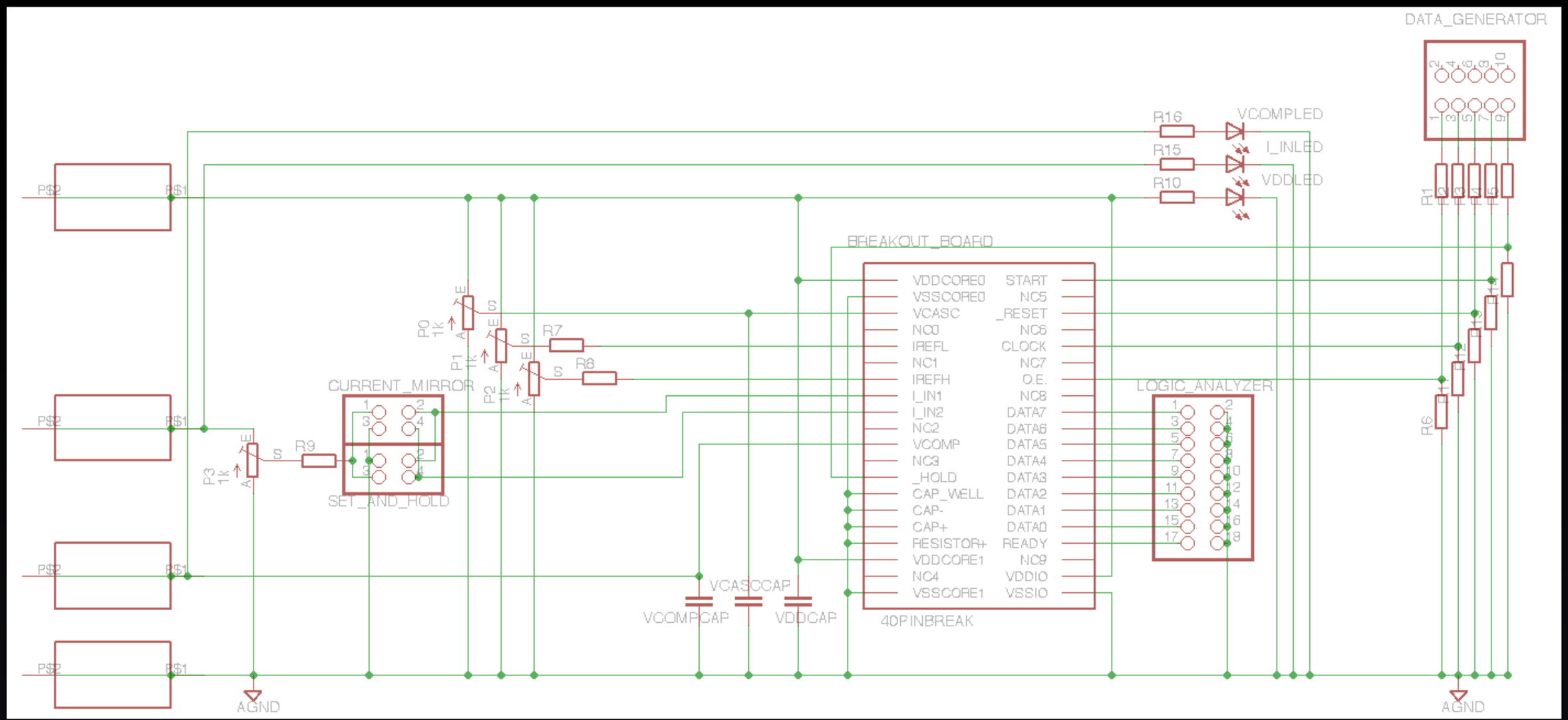
Results from last summer

- Irakli studied a previous generation of ADC last summer.
- Used an FPGA to send signals and readout the ADC.
- Found increasing frequency caused some steps to get narrower and some to get wider.
- Beat modified the ADC design for 8-bits, added a sampled and hold circuit, and added the ability to disable output.
- These changes were done to increase the linearity.

How do you test the ADC?

ADC Periphery Board

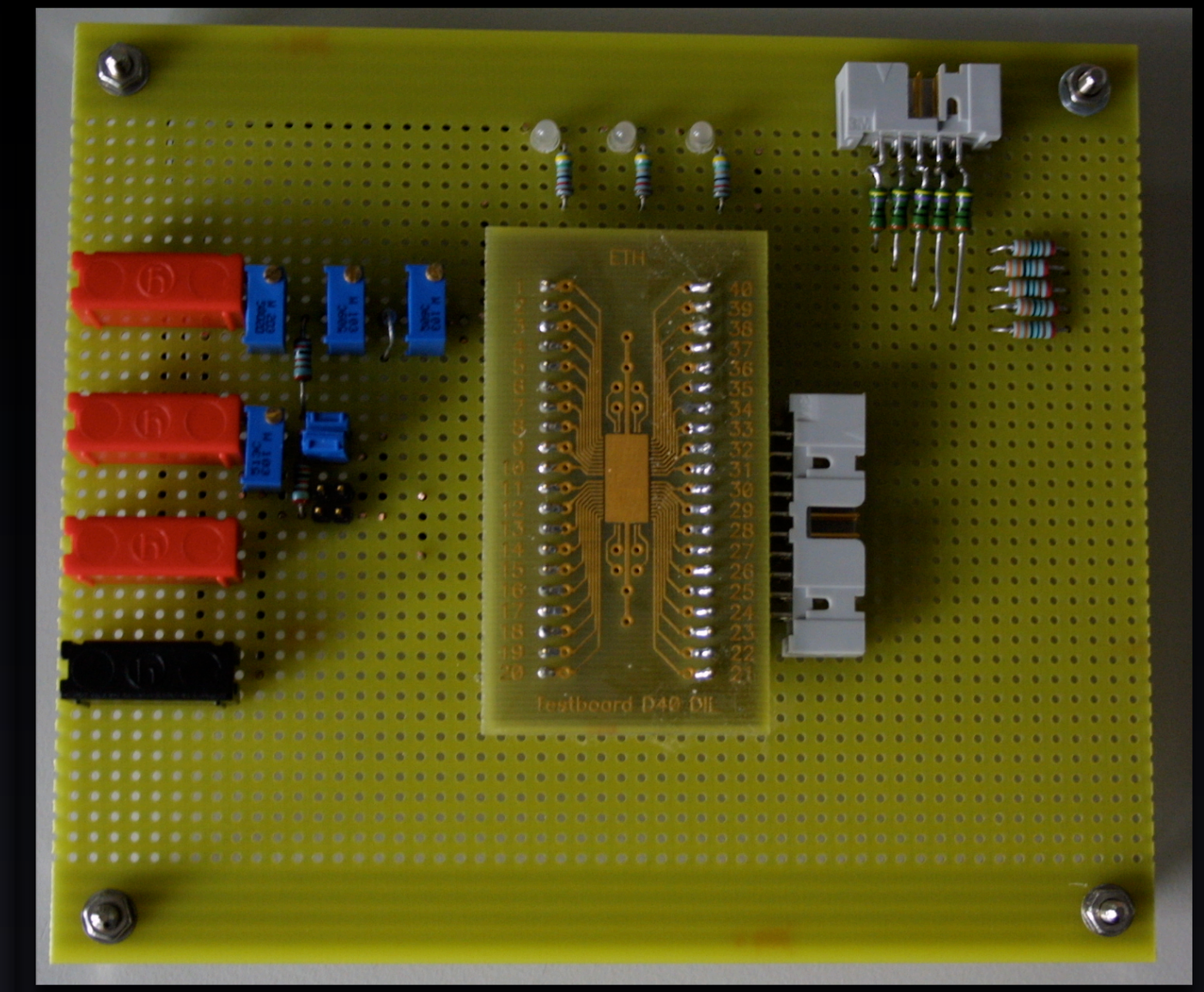
- ADCs for testing come on small silicon chips from an IC fab.
- These chips have been wire-bonded to a carrier board in order to make connections possible.
- 4-bit and 8-bit carrier boards plug into universal periphery board that will supply power, input test currents and allow attachment for monitoring digital output.


DATA_GENERATOR
R16
R15
R10
VCOMPLED
I_INLED
VDDLED
R1
R6
BREAKOUT_BOARD
VDDCORE0
VSSCORE0
VCASC
NC0
IREFL
NC1
IREFH
I_IN1
I_IN2
NC2
VCOMP
NC3
_HOLD
CAP_WELL
CAP-
CAP+
RESISTOR+
VDDCORE1
NC4
VSSCORE1
START
NC5
_RESET
NC6
CLOCK
NC7
O.E.
NC8
DATA7
DATA6
DATA5
DATA4
DATA3
DATA2
DATA1
DATA0
READY
NC9
VDDIO
VSSIO
40PINBREAK
LOGIC_ANALYZER
CURRENT_MIRROR
SET_AND_HOLD
P0
P1
P2
P3
R7
R8
R9
VCASCCAP
VCOMPCAP
VDDCAP
P$2
P$1
AGND

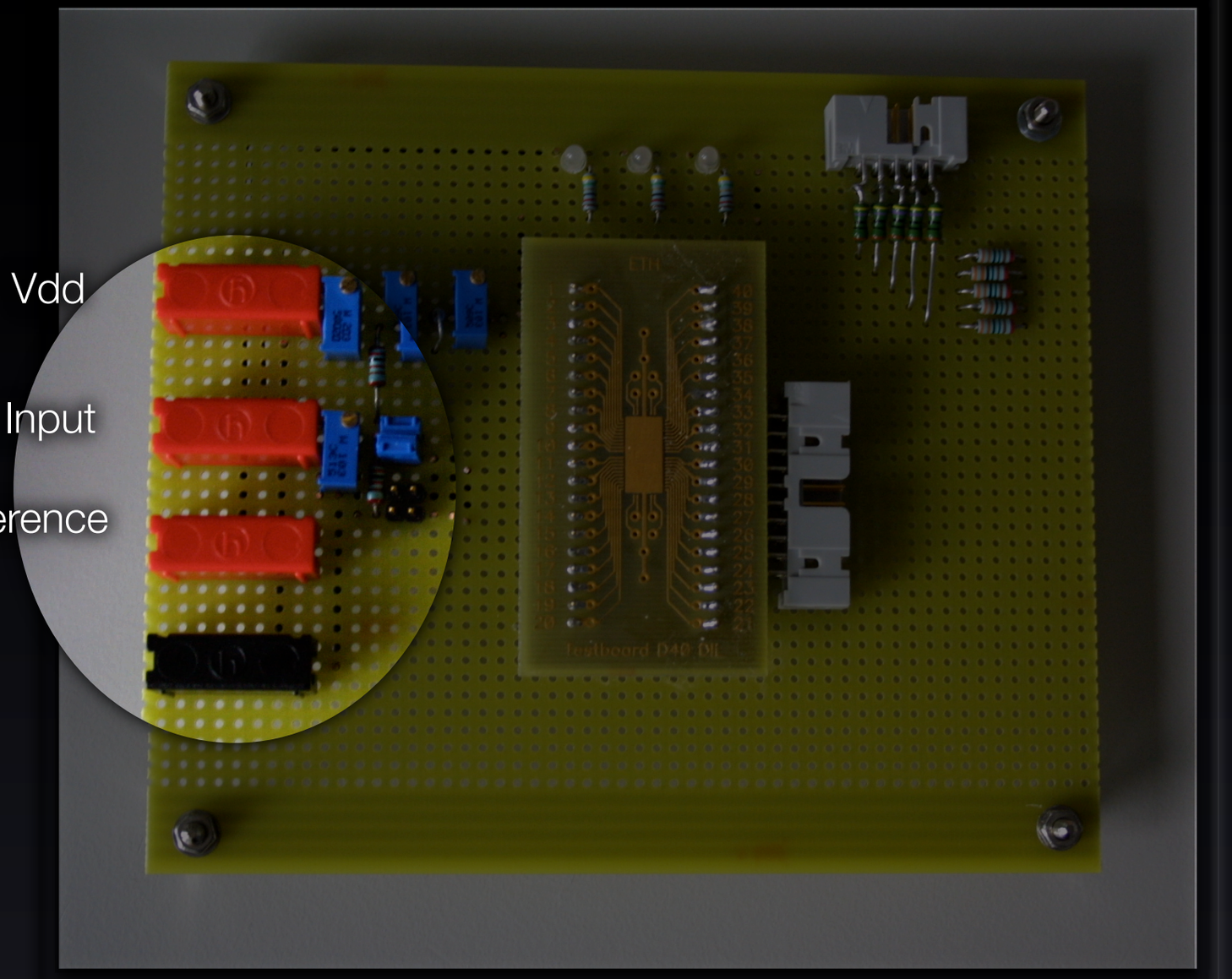
Schematic

ADC Periphery Board

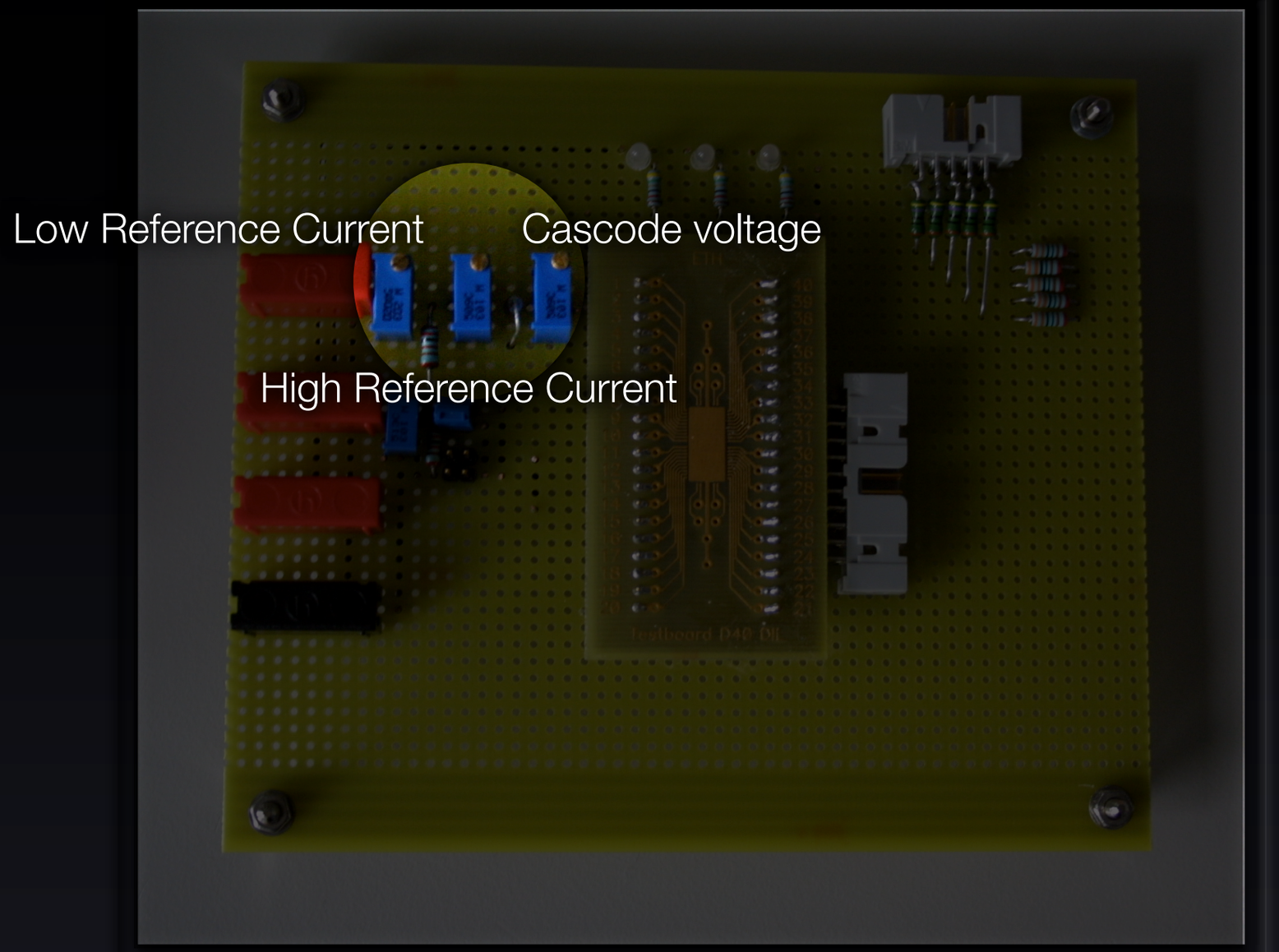
- The ADC periphery board allows easy connections to be made to the ADC chip. The ADC requires many analog and digital inputs. The various inputs have been organized by type on the periphery board. Besides offering a simple connection, the periphery board is also equipped with potentiometers to adjust analog signals.
- The periphery also allows for easy connection to the ADC's digital output. The output contains either 4 or 8 data bits as well as the "ready" signal.



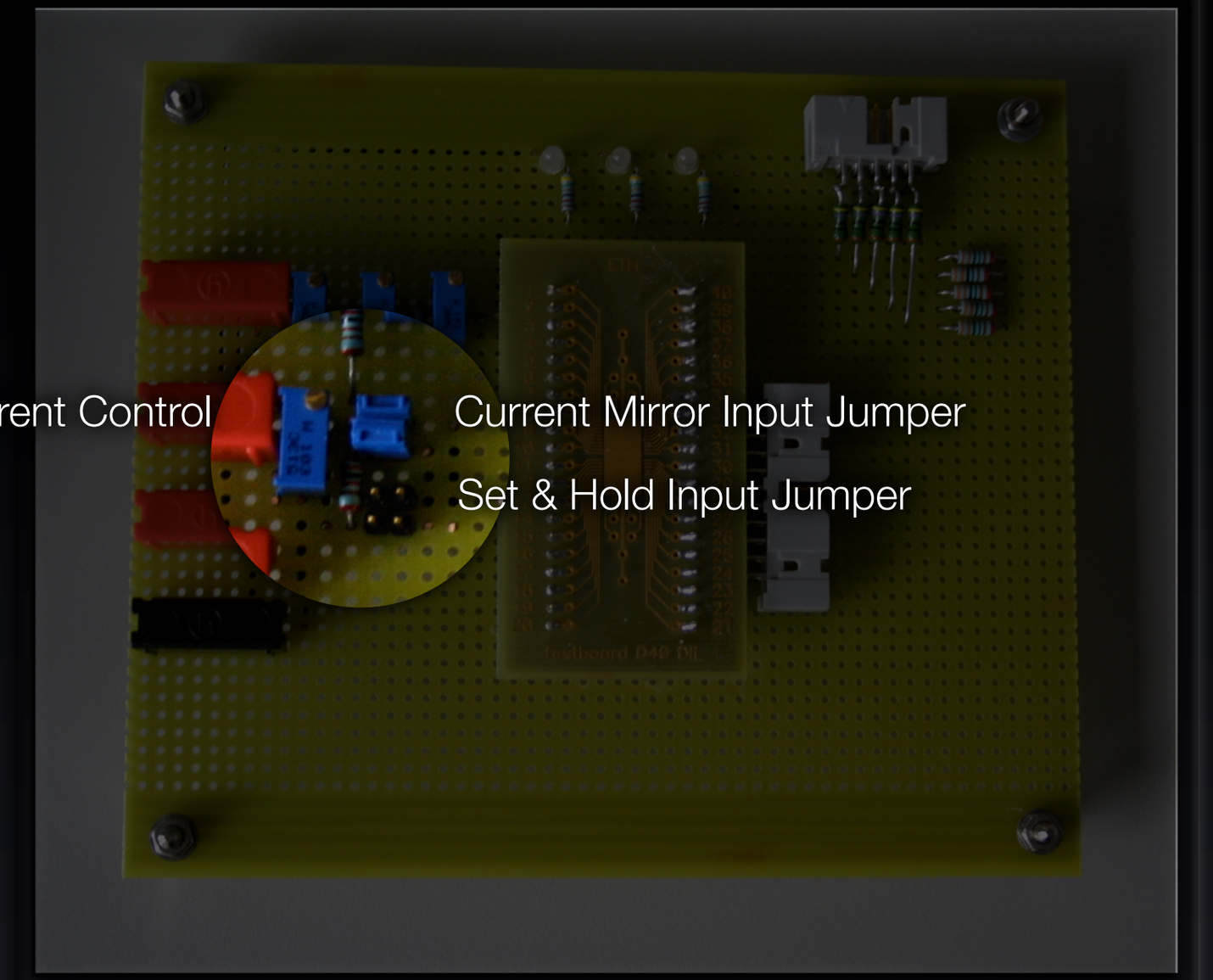
Periphery Board



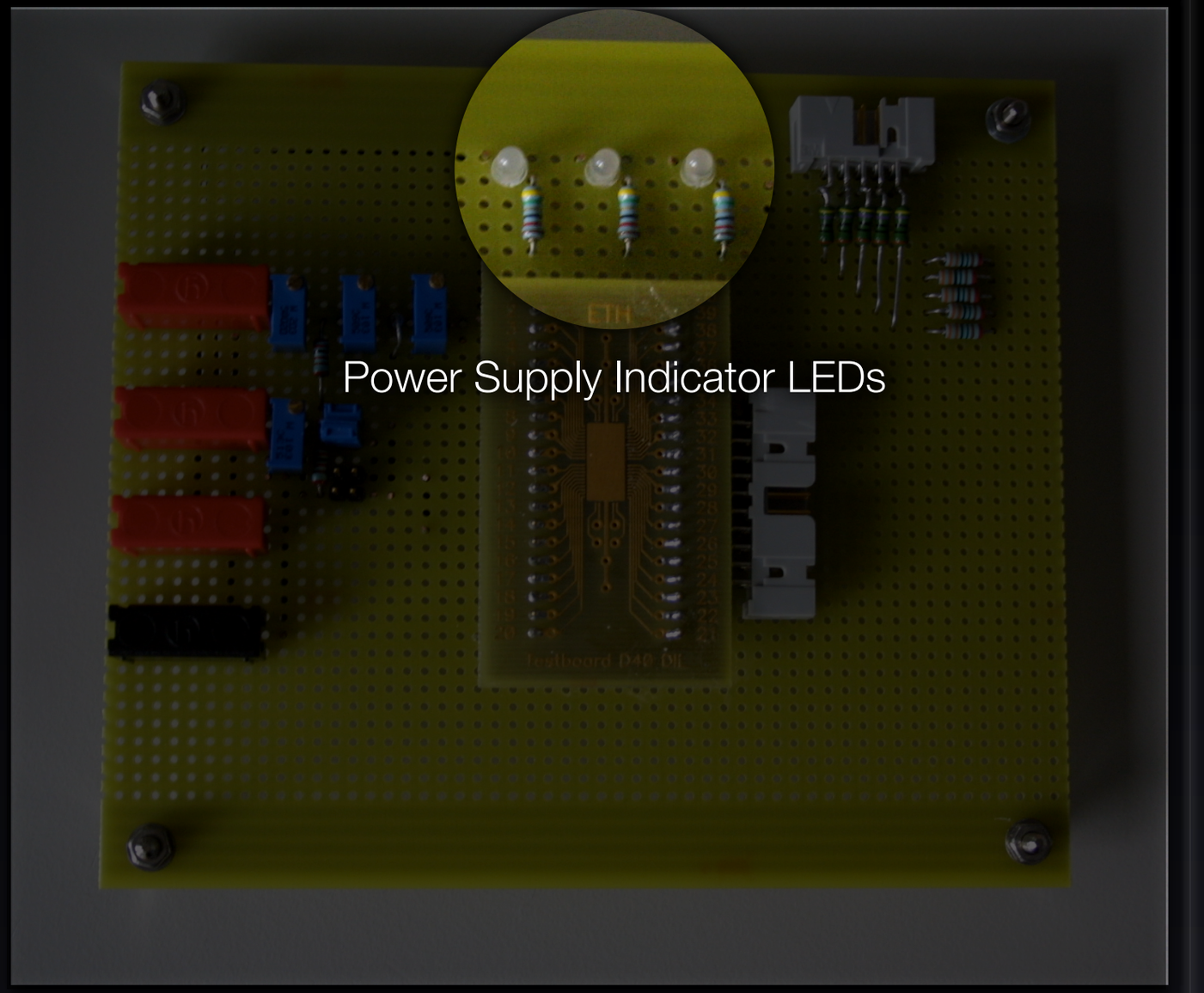
Independent power supplies



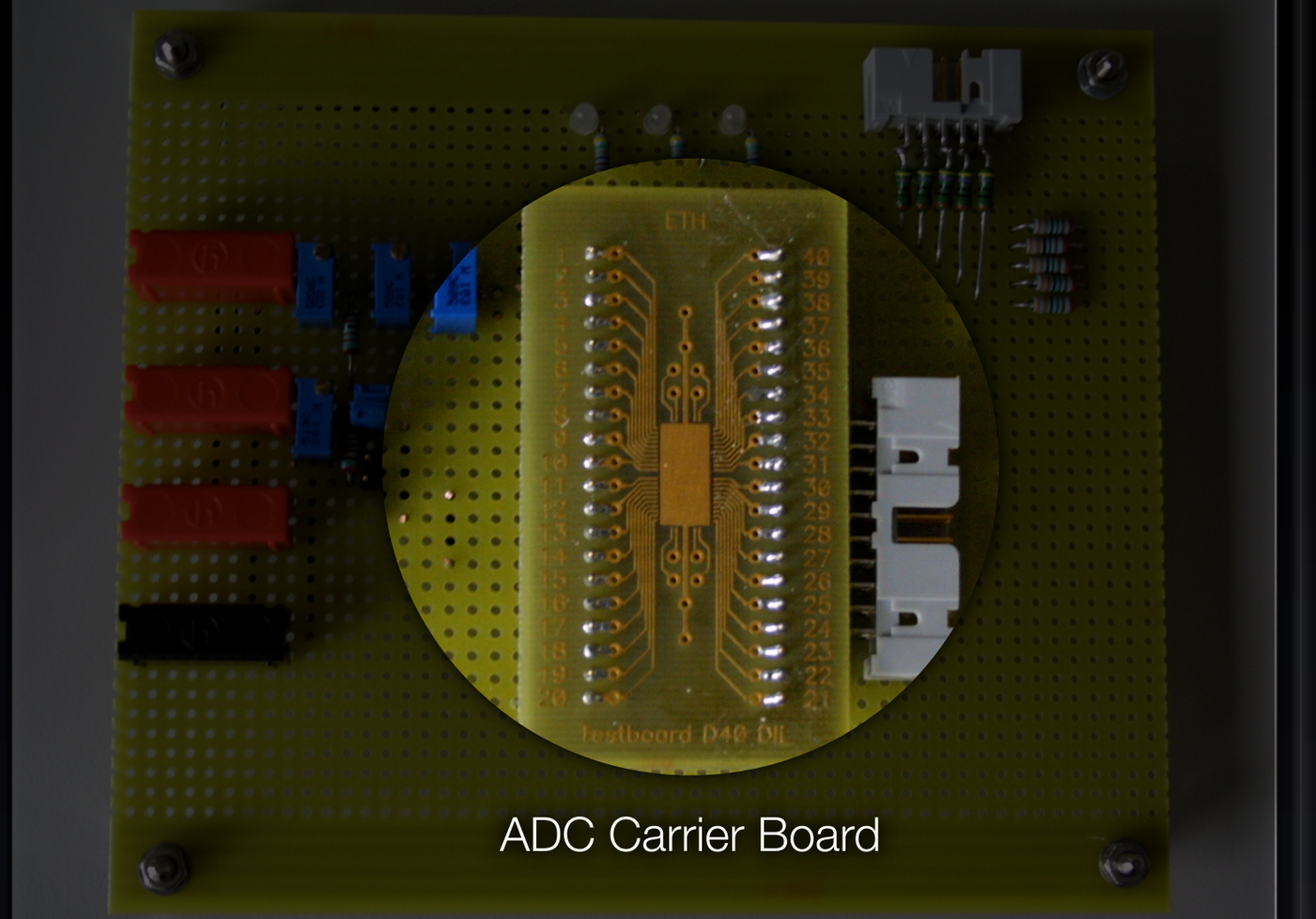
Dependent Sources (Vdd)



Current Input

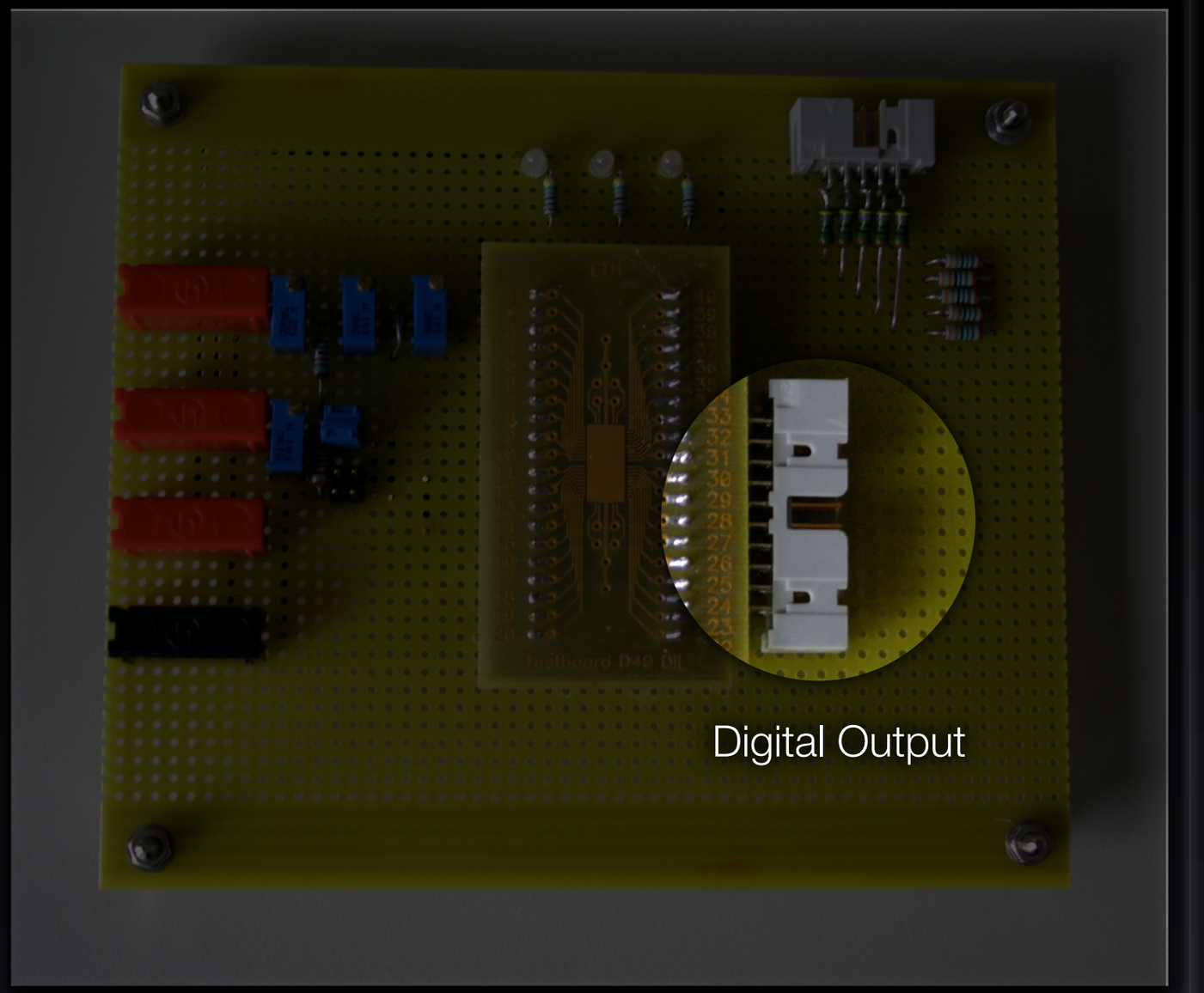


Indicator LEDs

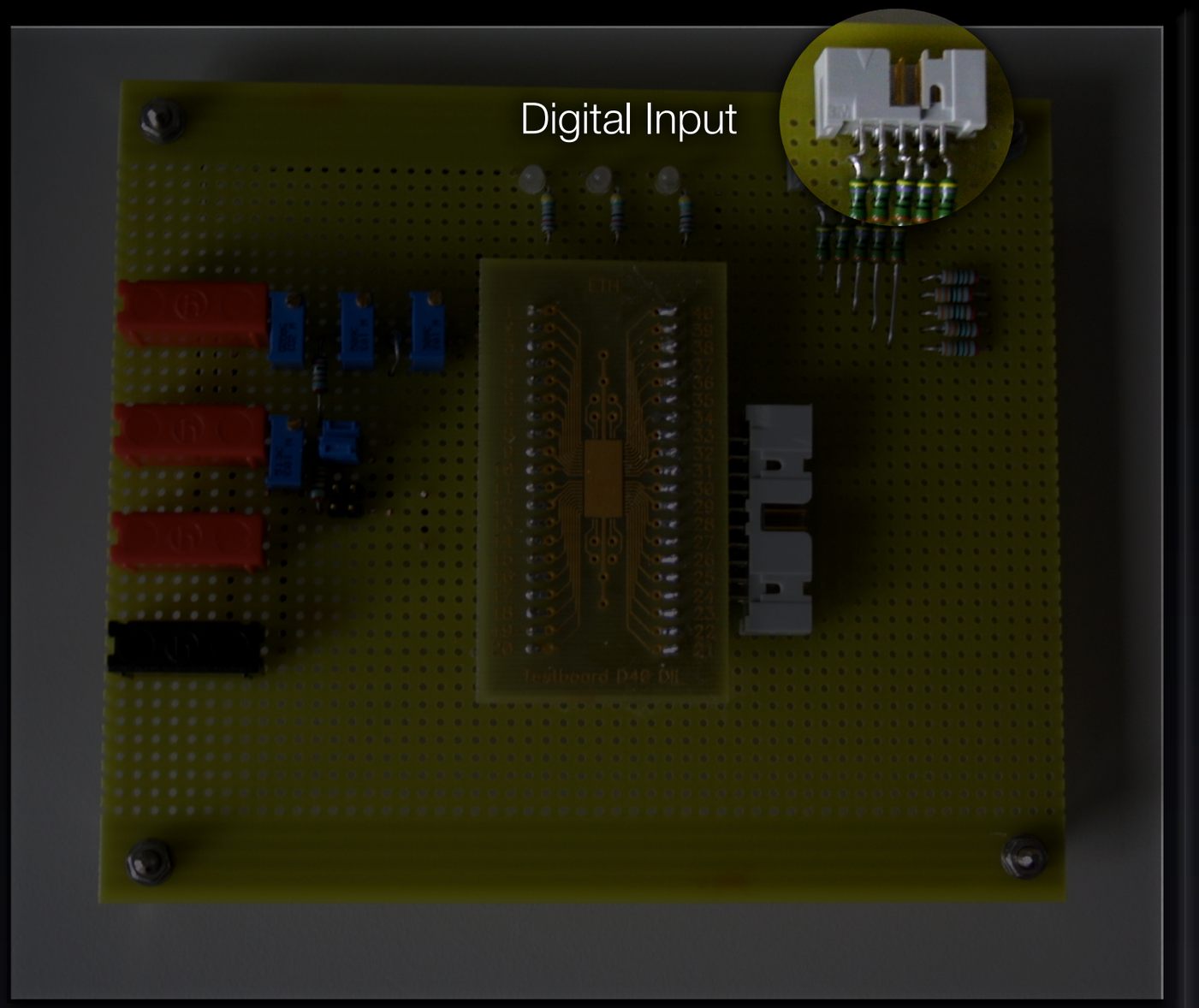


ADC Carrier Board

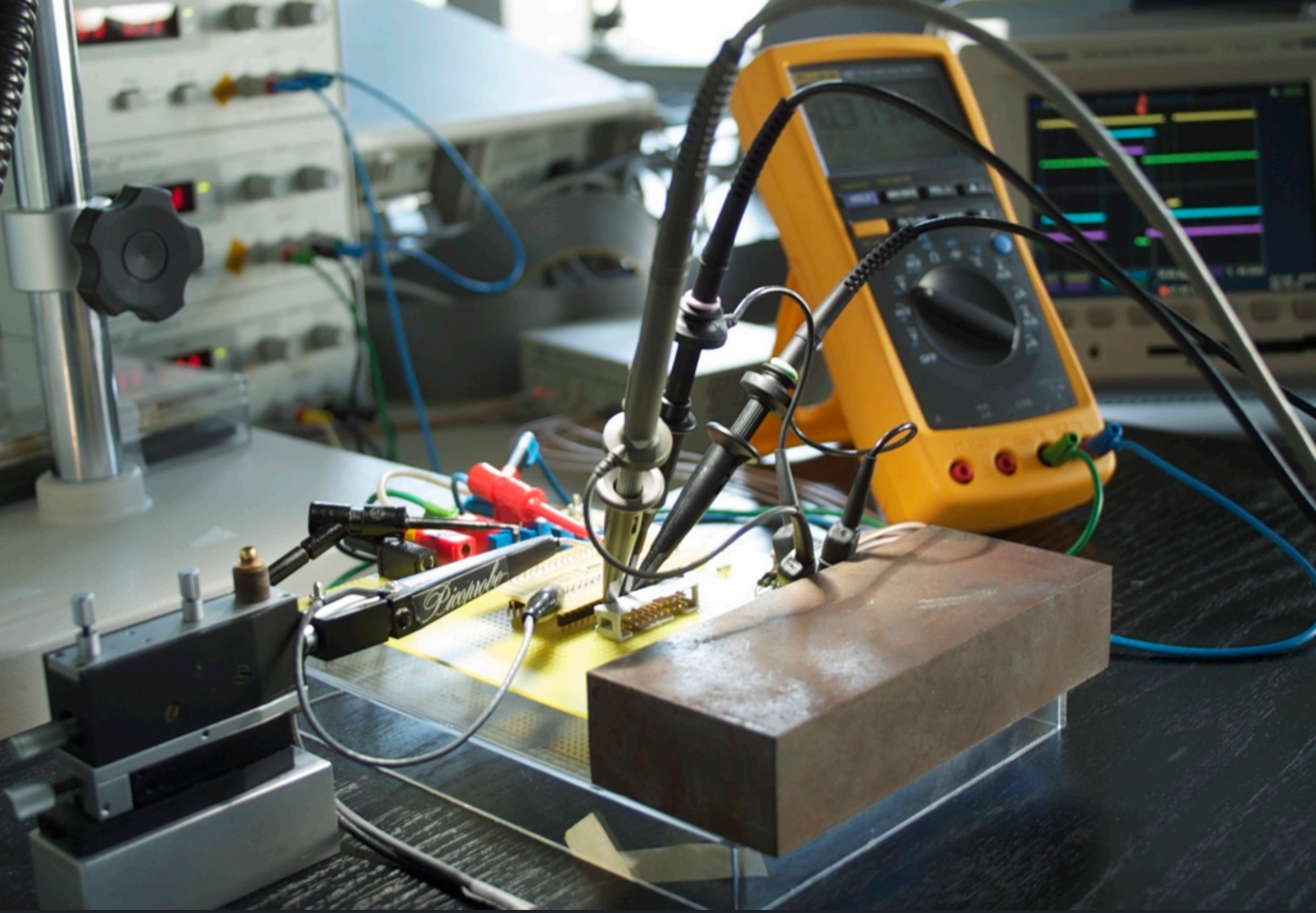
Carrier Board

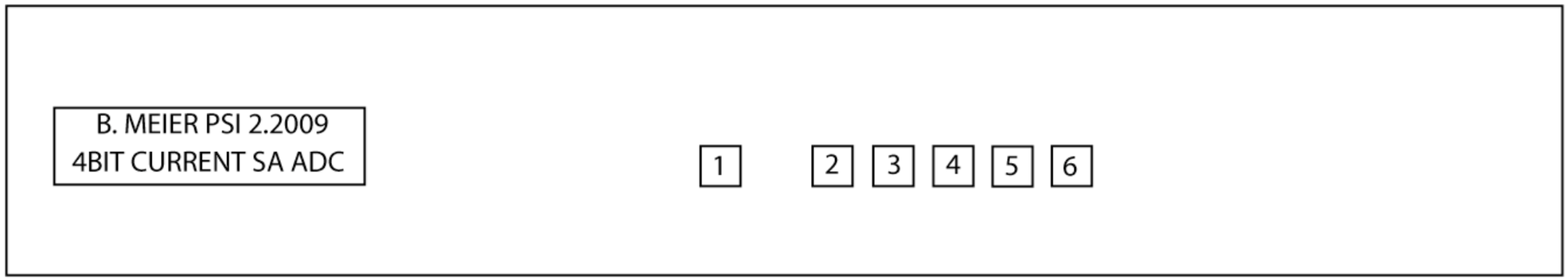


Digital Output



Digital Input





Spy pad layout

What was discovered about the ADC?

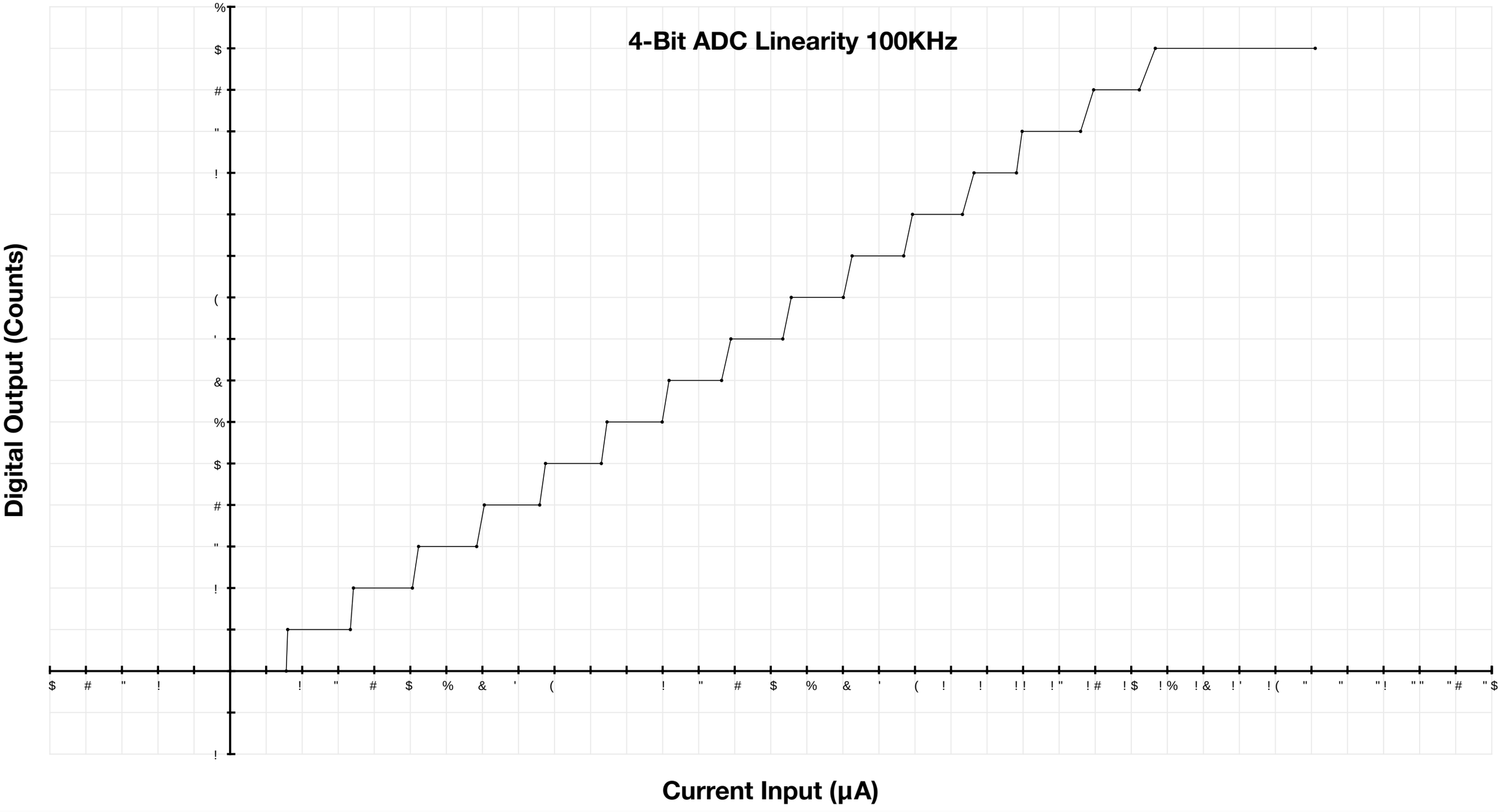
Functionality Verification

- For 4-bit and 8-bit ADCs,The following functionalities have been verified:
  - Basic conversion
  - “Ready” signal output
  - Output Enable (disable) - New this generation
  - Current Mirror input - New this generation
  - Set and Hold input - New this generation

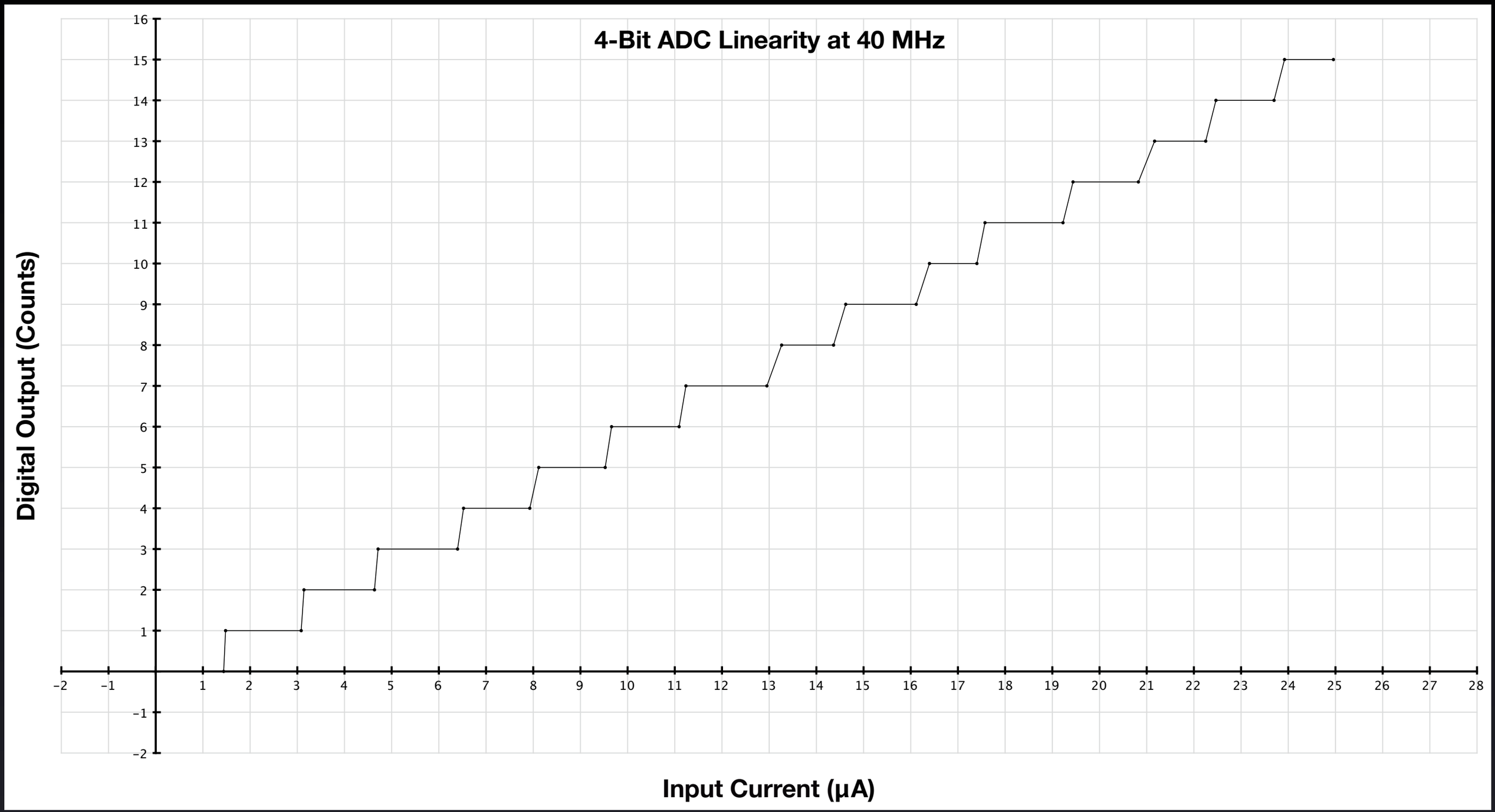
Linearity Tests

- Linearity tests run on 4-bit ADC.
- More-even step widths = Better Linearity
- Frequencies of 100kHz, 40MHz, 80MHz, 160MHz tested.
- Tested with and without the output enabled during conversion. Disabling output during conversion expected to increase linearity at higher frequencies.

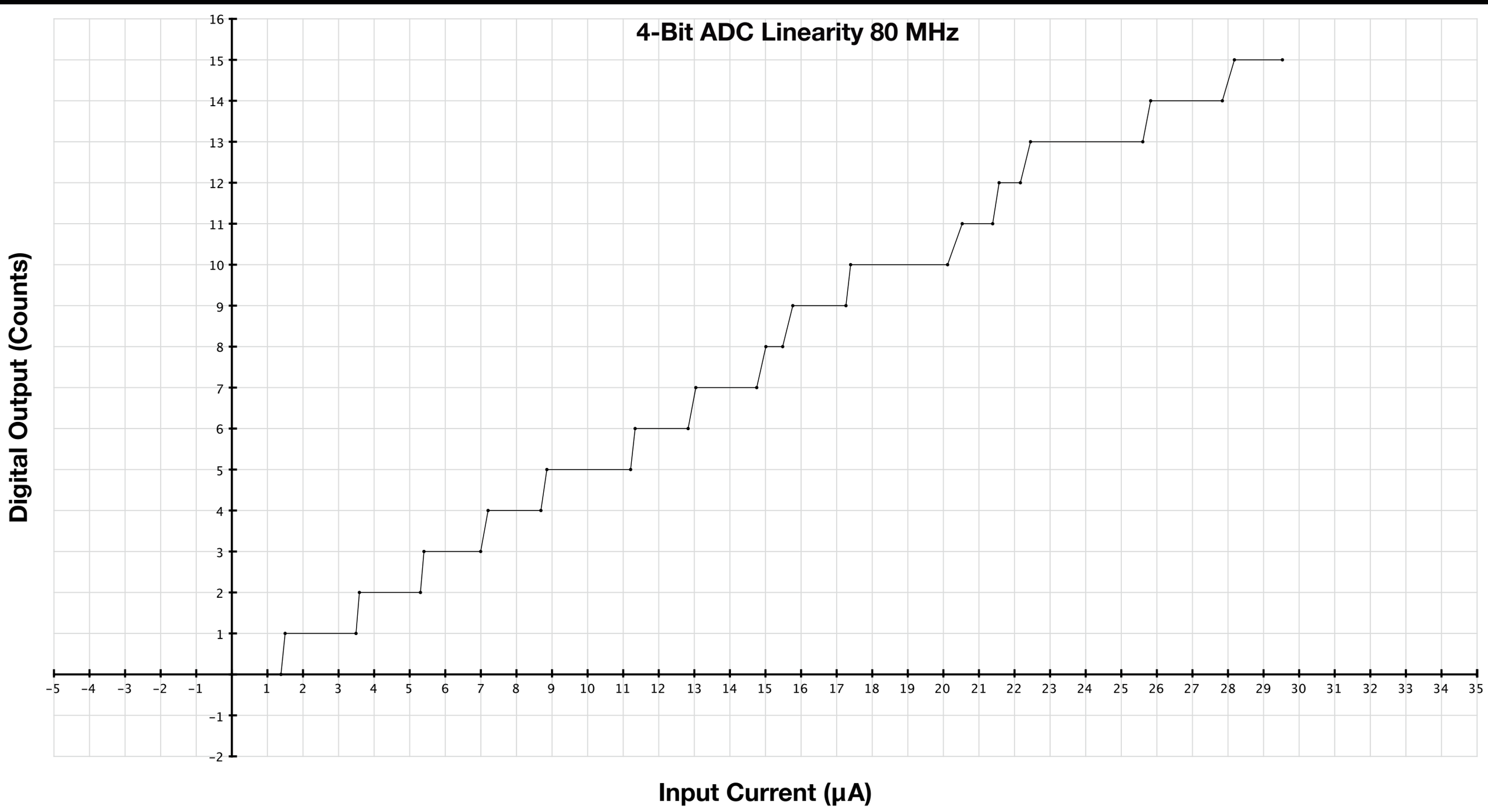
Output Enabled



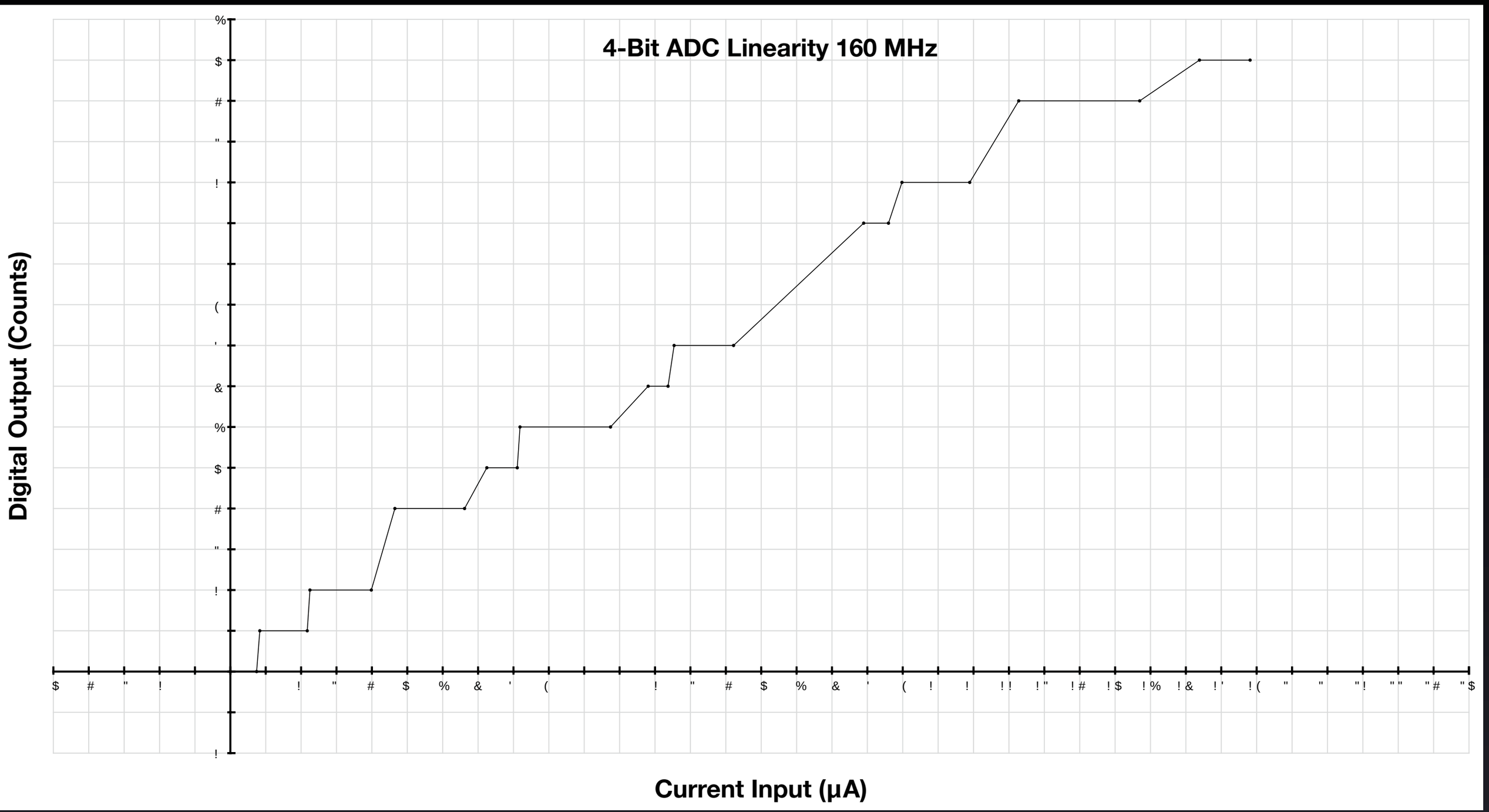
Output Enabled



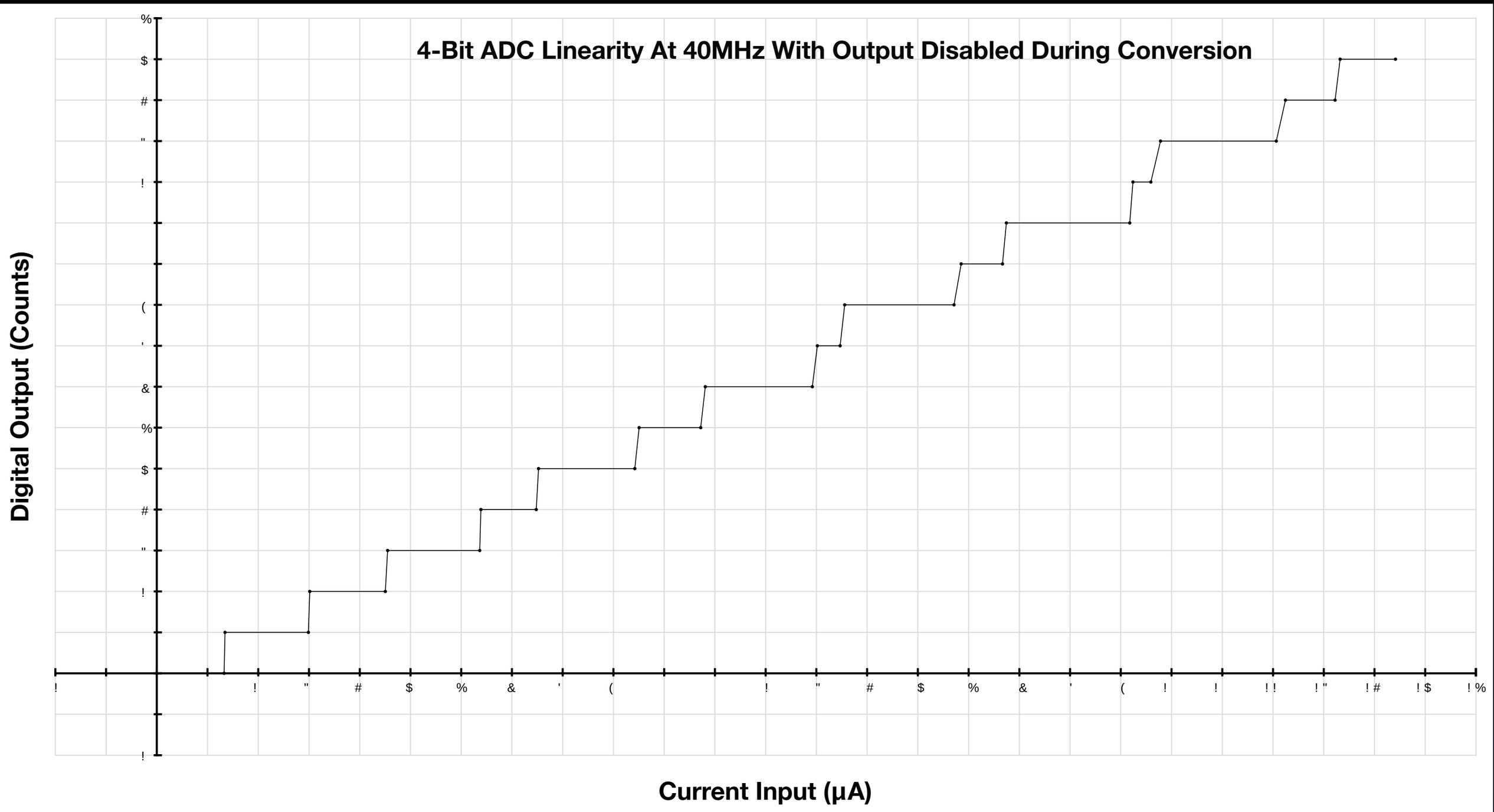
Output Enabled



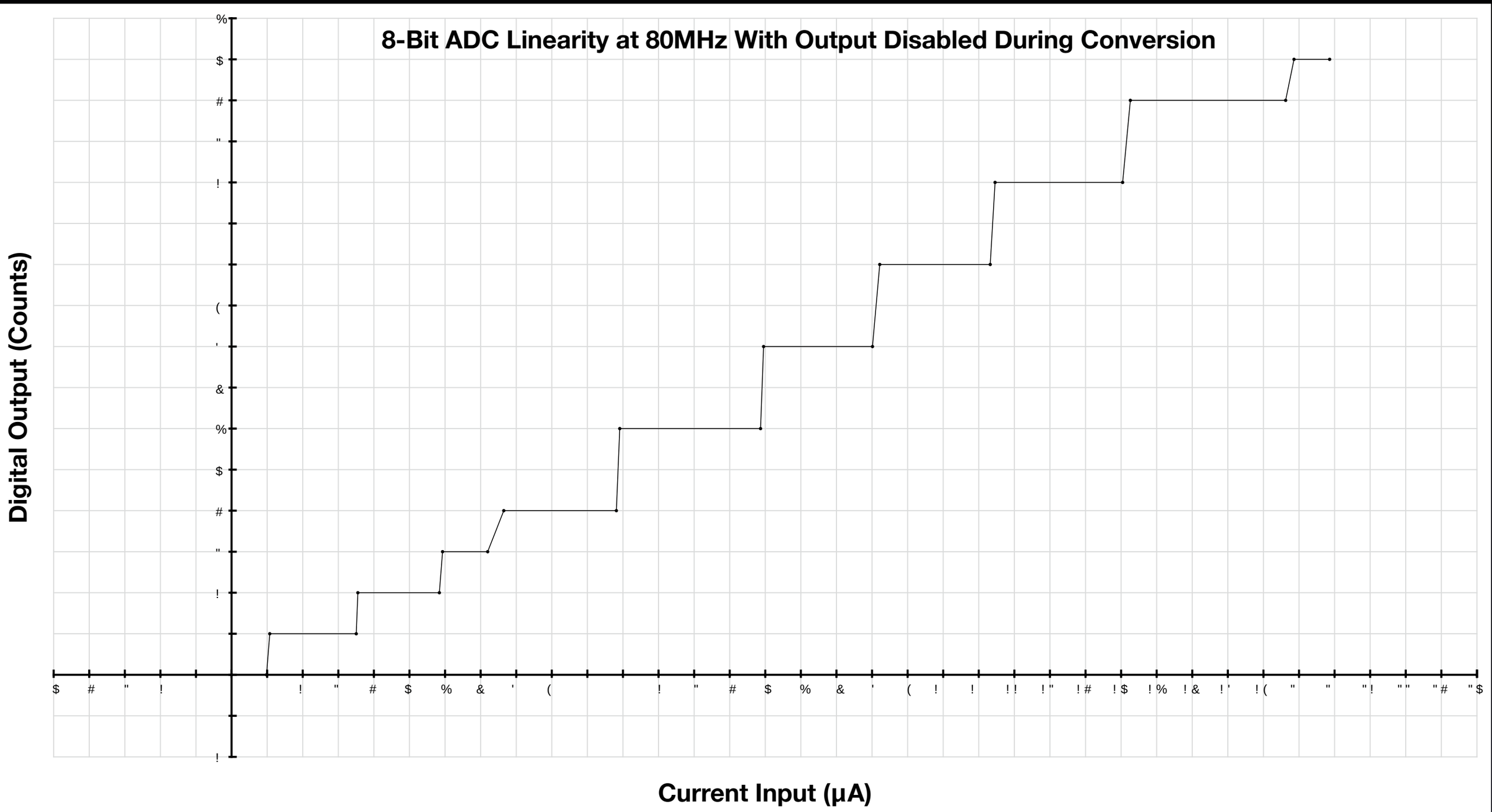
Output Enabled



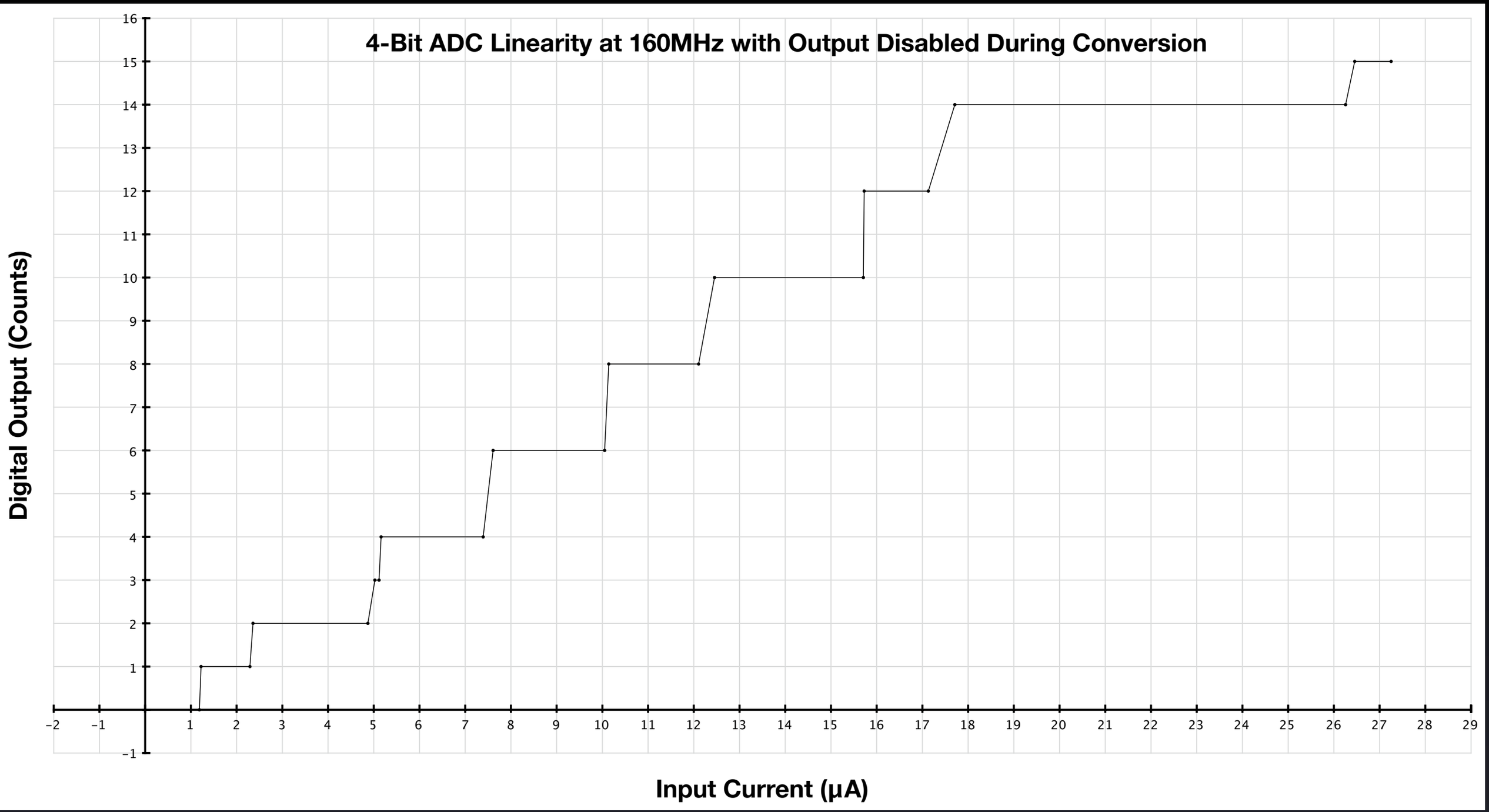
Output Disabled



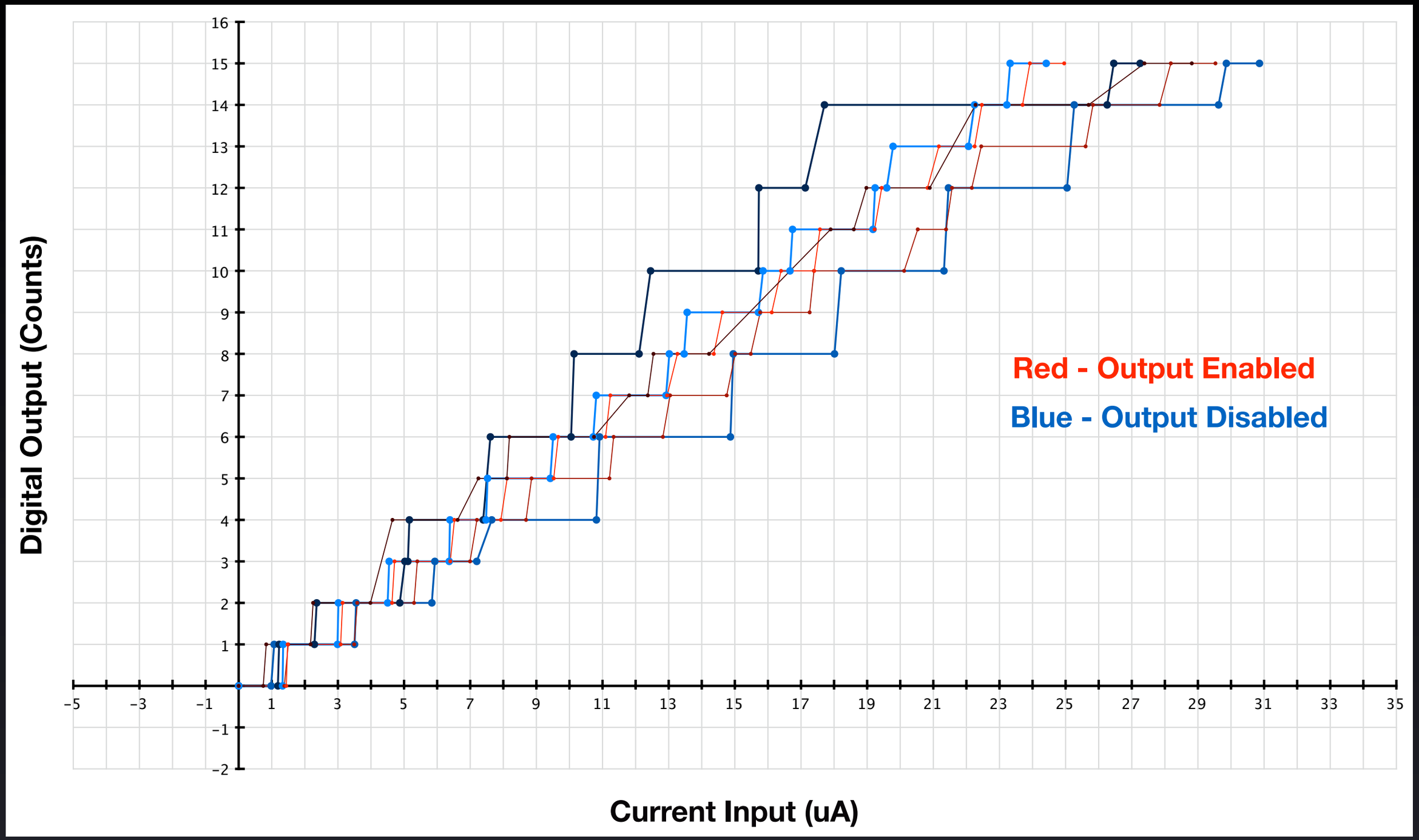
Output Disabled



Output Disabled



All Graphs


Digital Output (Counts)
Current Input (uA)
Red - Output Enabled
Blue - Output Disabled
16
15
14
13
12
11
10
9
8
7
6
5
4
3
2
1
−1
−2
−5
−3
−1
1
3
5
7
9
11
13
15
17
19
21
23
25
27
29
31
33
35

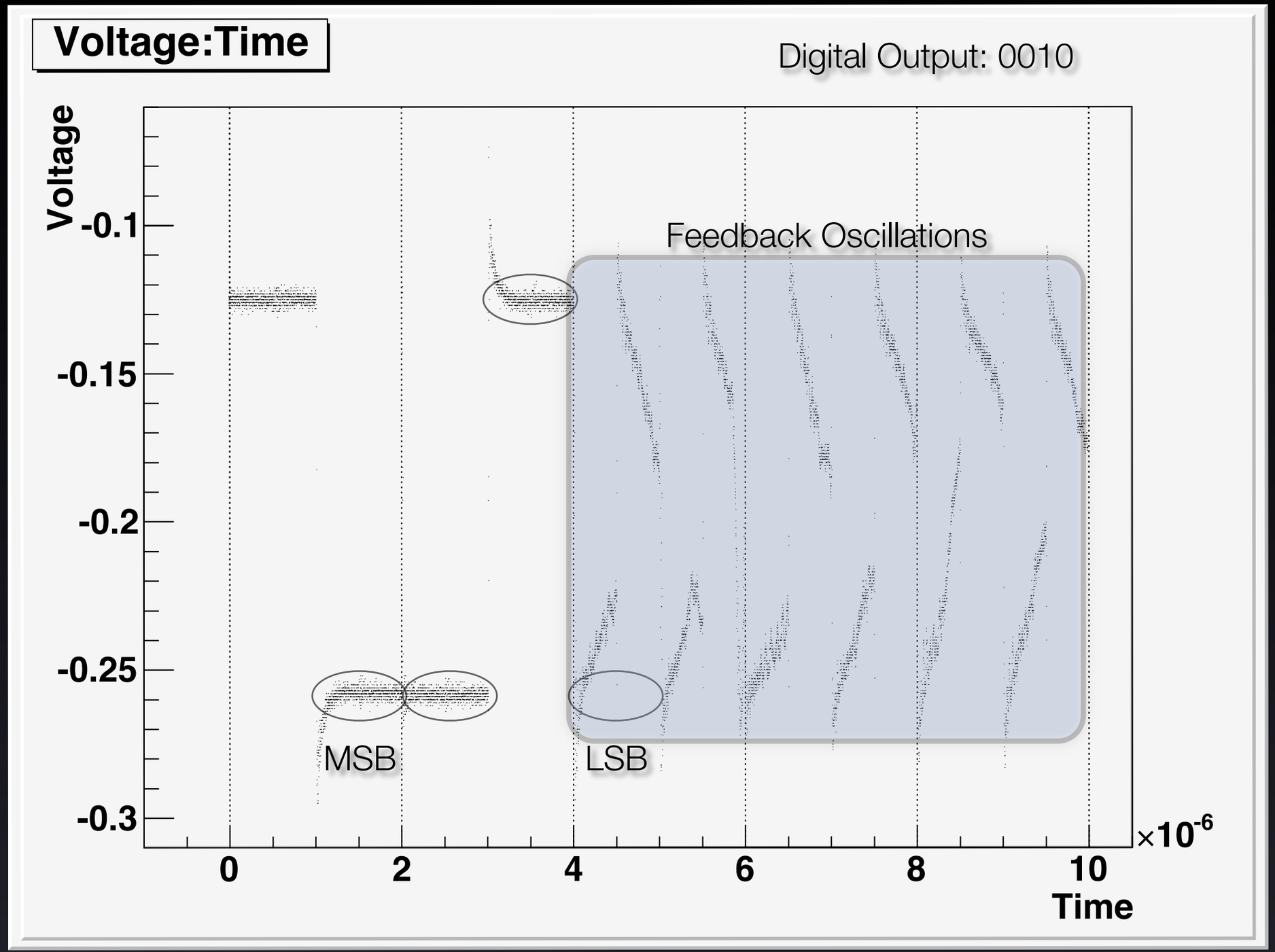
Findings

- Turning off the output during conversion actually decreased linearity.
- The ADC must function at 80MHz to be used in the pixel read out chips. Currently, the linearity is not up to specification.
  - Varying step widths
  - Missing steps
- 8-bit ADC based on same design, same problems assumed to occur

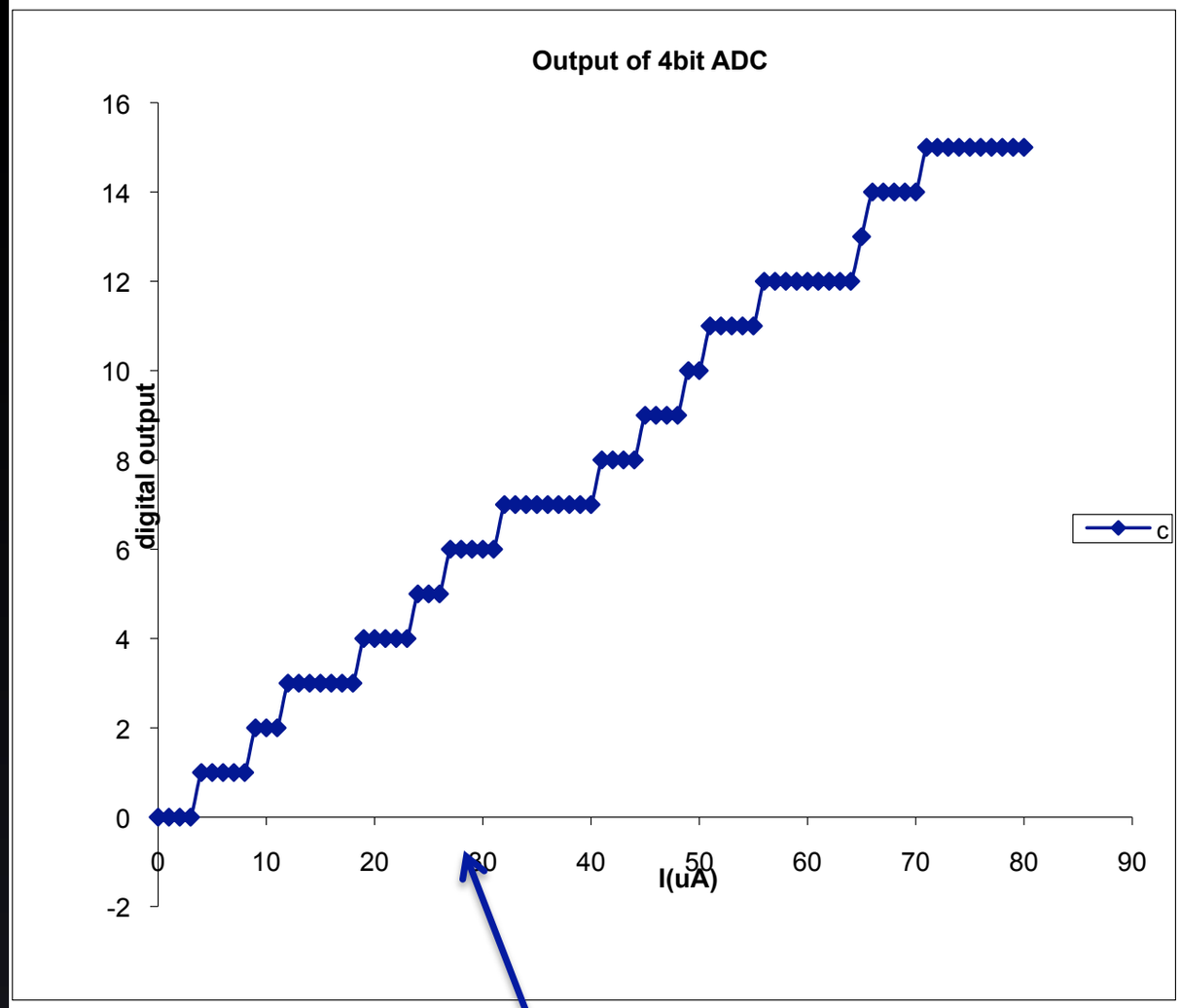
What now?

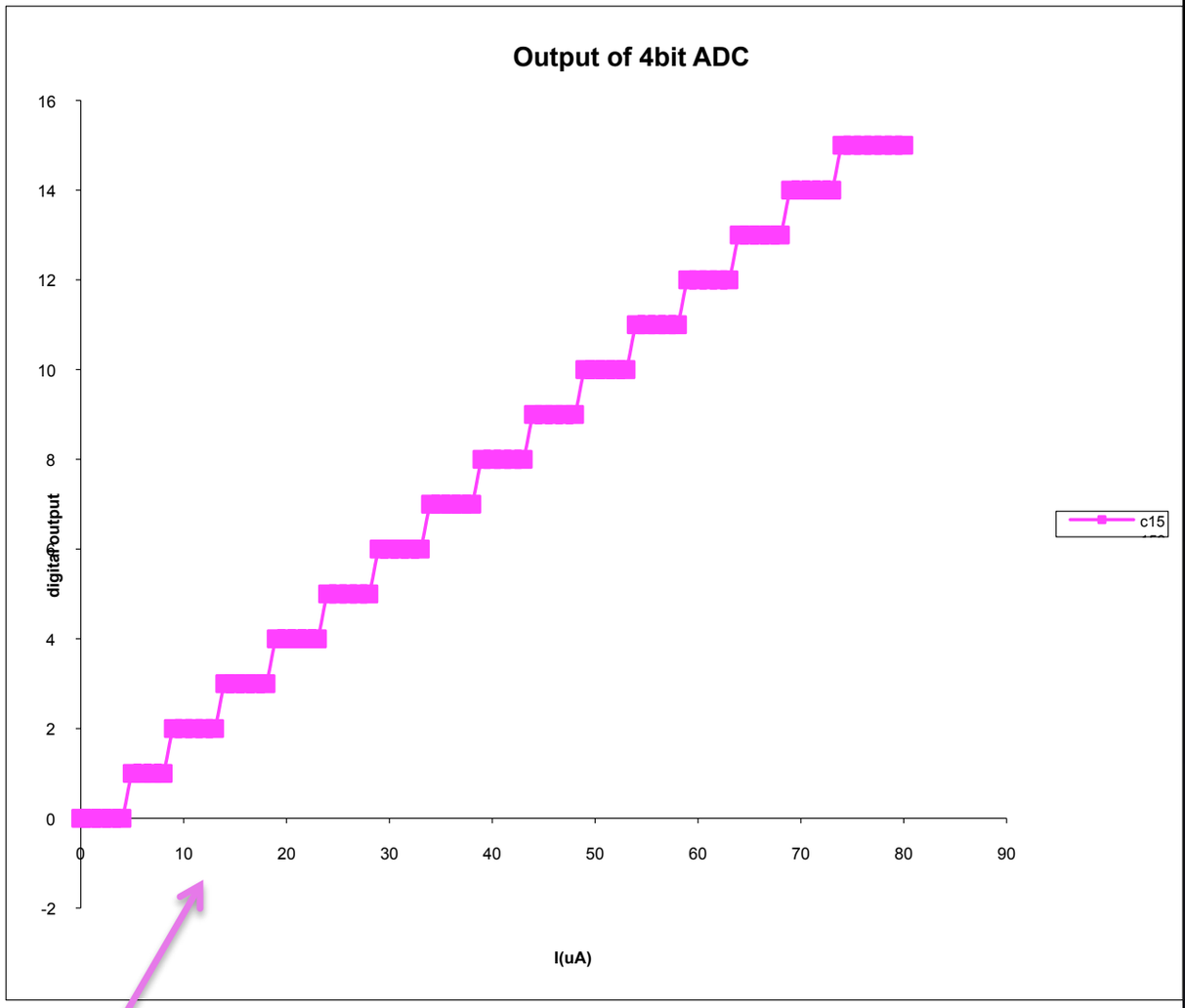
- Started investigating reasons for varying step widths.
- Attached pico probe to view comparator output.
- Observed strange feedback oscillations.
- Suspected cause: parasitic capacitance between comparator input and output. Modeled in computer and found an oscillation.
- Try to prove that this feedback oscillation is causing variation in step widths.

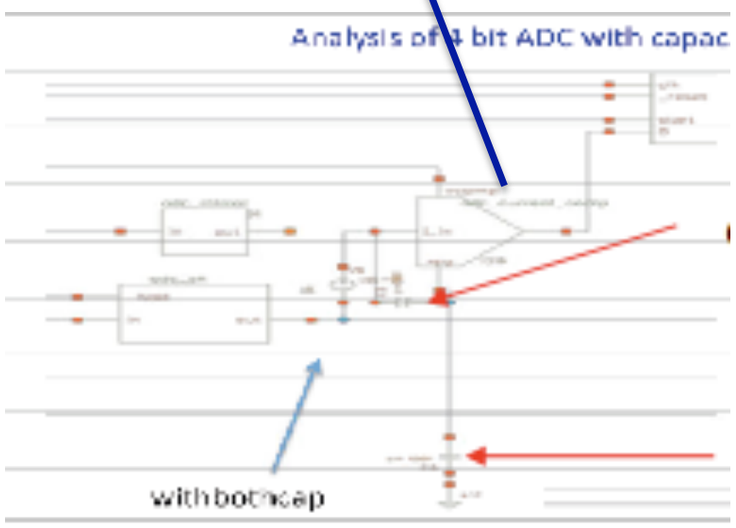
Example of Feedback Oscillation on Comparator output



Analysis of 4bit ADC with capacitor across the comparator







C1=15fF , 15fF

C2=50fF, 150fF

Current status

- Left periphery board at PSI for further research there.
- Built a similar periphery board for UNL.
- Will program an FPGA to send digital signals and readout ADC.

Questions?