Upgrade of Calo FE electronics: AIM of STUDIES

- **Since the L0 trigger is either non existent or less restrictive=> concentrate on ECAL/HCAL (PS SPD perhaps not needed)**
- **For ECAL/HCAL front end 2 main changes**
- **PMT Gain has to be reduced by about 5 to reduce PMT current => redesign amplifier integrator => Barcelona studies**
- **Readout at 40 MHz => no CROC + Fiber readout per FE card => redesign digital part => LAL study**
- **Common proto cards**

Analog specifications

- **X5 in gain => input noise has to be about ÷ by 5 =>≈ 5 fcoulomb at input if clipping at PMT conserved.**
- **Input impedance has to be well controlled (reflection after 2X 12.5 m coax should be < about 1-2%)**
- **Two solution studied => simulation+prototype**
  - **Commercial Op amp + delay line**
  - **Asic + switch system**

Digital specification

- Keep signal treatment (dynamic pedestal subtraction)
- Keep present trigger construction
- Save space => 8 channels/FPGA
- Decrease Fiber number by data compression in FE cards FPGA
- Find FPGA without ProAsic-Plus problems => proto test