Enhancement Presentation

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Barcelona September, 9th 2009

Enhancement Presentation

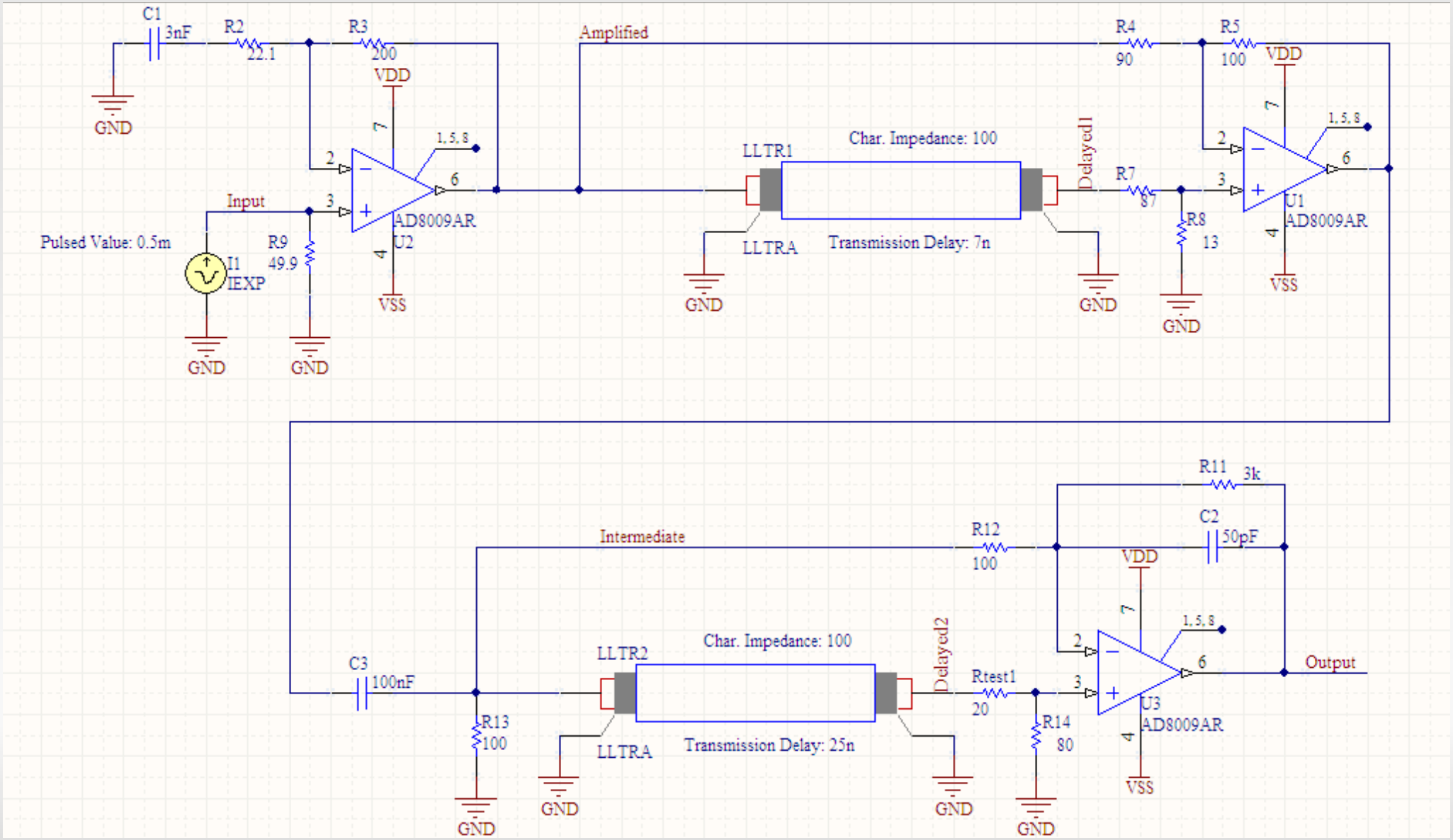
- Summary
  - Discrete components
  - Testing differential amplifier solution
  - ADC selection
  - Analogic Prototype

Discrete Commercial Parts

- Testing differential amplifier solution
  - As discussed in last meeting using a single operational amplifier and the same polarity of the integrating and disintegrating signal is not a good option.
  - Instead it would be interesting to use a differential operational amplifier to do the job. This gives us the advantages of differential signals. Noise immunity and easy ADC interfacing as main features.

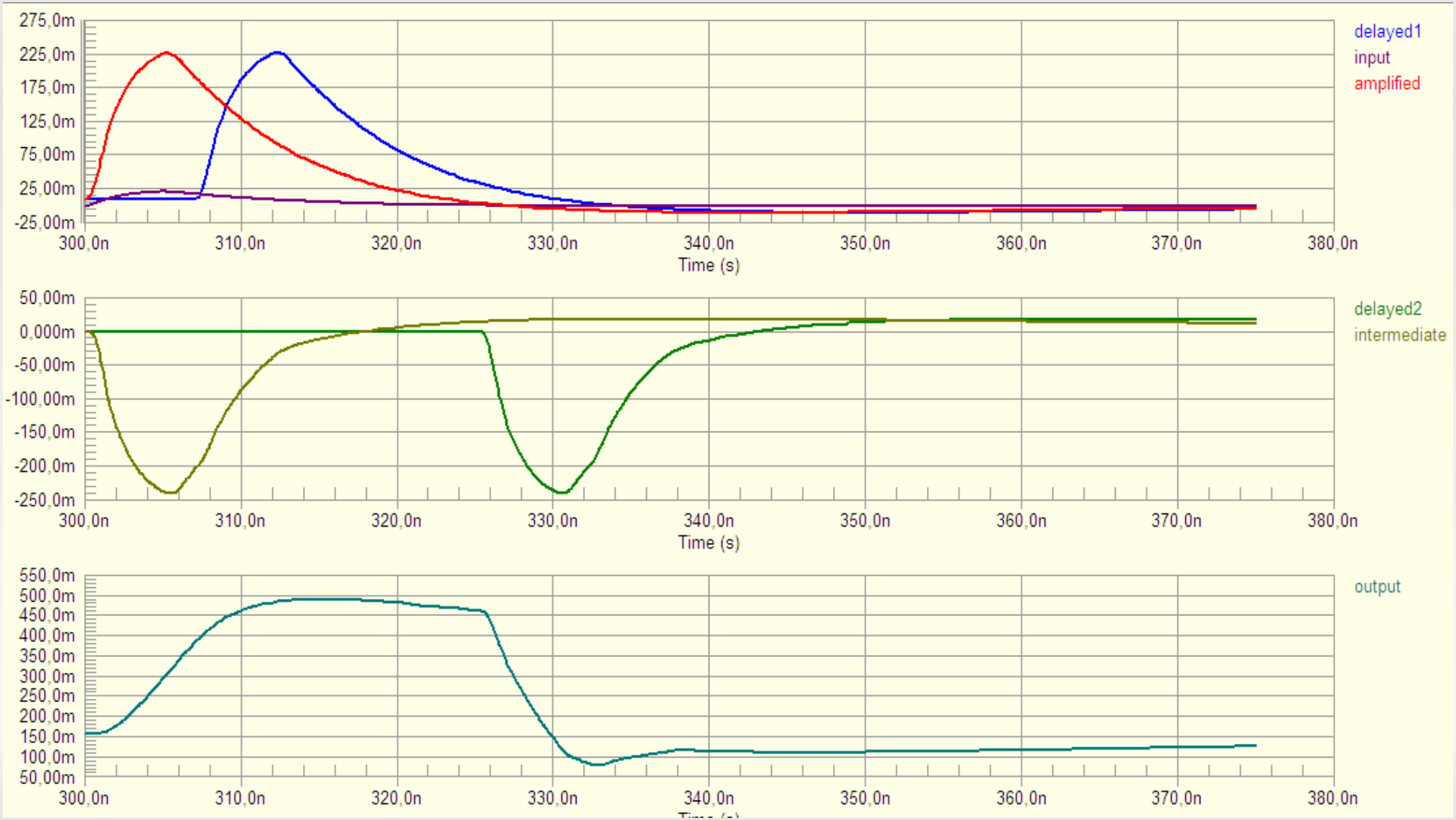
Analogic Part

- Last meeting's configuration



Analogic Part

- Last meeting's results



Analogic Part

- Last meeting's problem

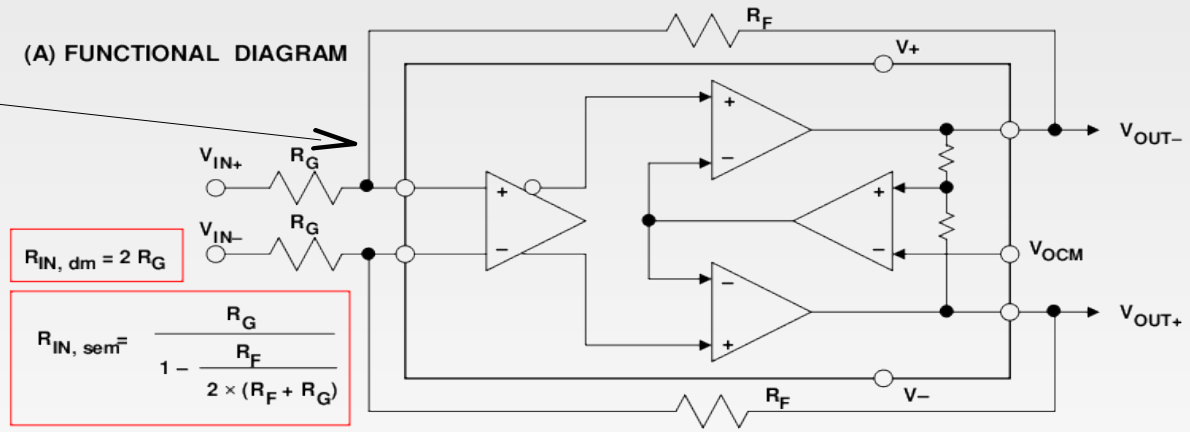
$$Output = \frac{1}{\tau} \int (Intermediate - Delayed2)\, dt + Delayed2$$

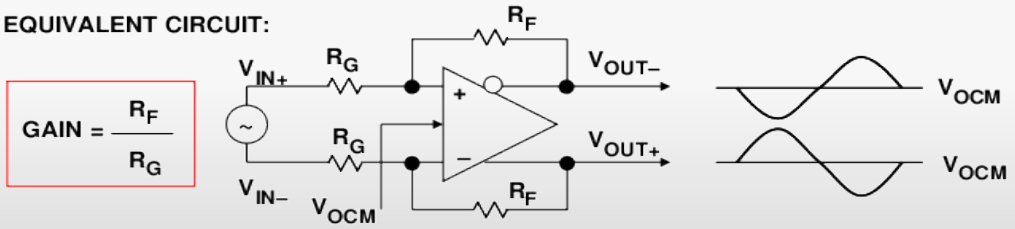
- The output shape is not symmetric due to the addition of the Delayed signal to the output. This may lead to a problem if the Delayed signal is not zero. This may be a problem because reflections would happen at a 25ns multiple.
- This is because both signals are treated in different ways, by using a differential amplifier we may treat both signals in the same way.

Analogic Part

- Differential operational amplifiers
  - Acts like a normal operational amplifier but with two outputs accomplishing some restrictions:
    - (Voh+Vol)/2=Vcm
    - Signals have the same amplitude but are 180º de-phased
  - Equivalent model

Va



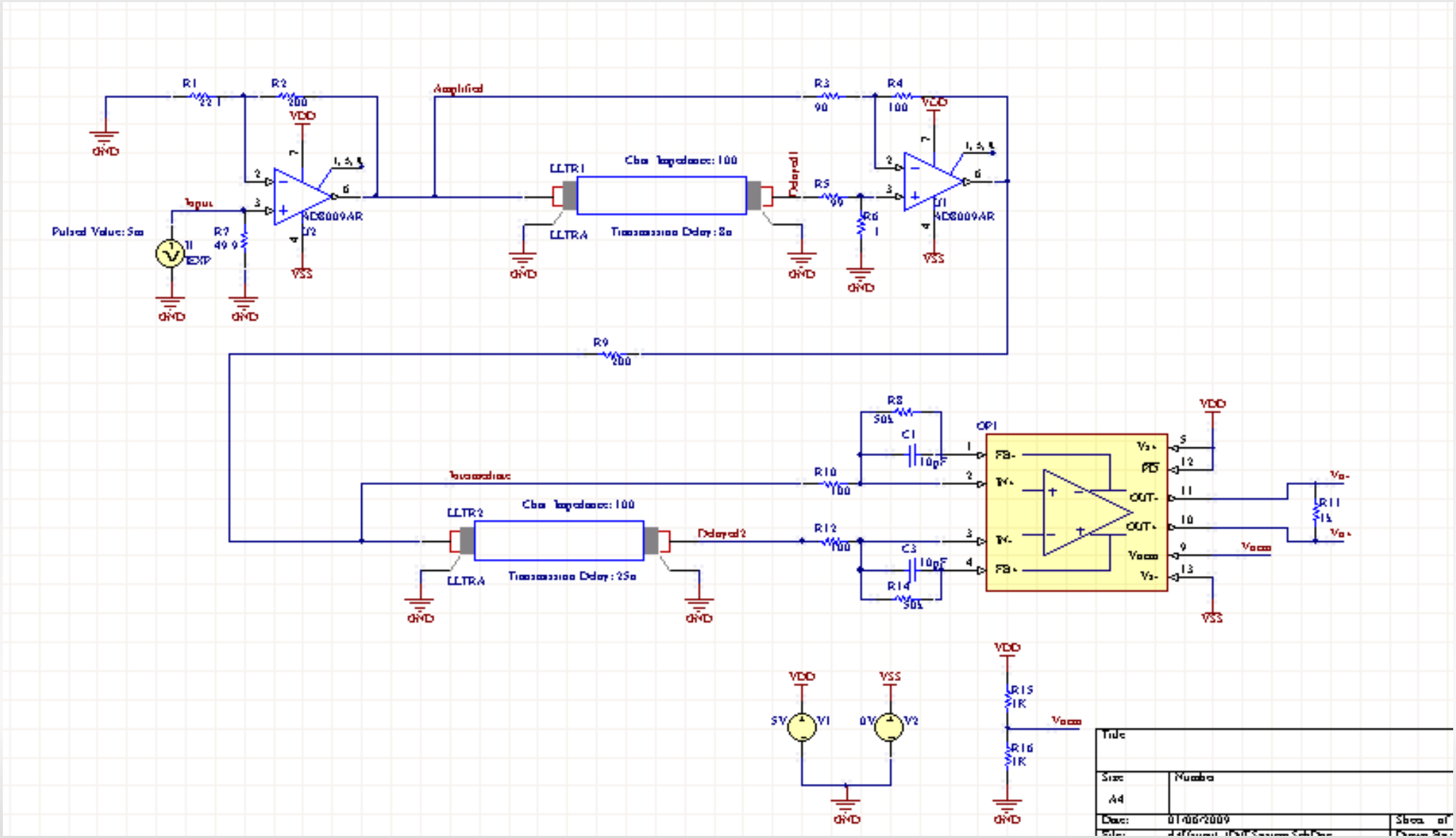


Analogic Part

- Differential operational amplifiers
- Problems found
  - These amplifiers are thought to be used with strong inputs which is not our case. Instead we have an input with 50Ω or 100Ω depending on the delay line used. This is harmful because of the internal loop restrictions. They force an immediate current response to the input signal through the other input leading to interferences. Let's see an example:

Analogic Part

- Scheme with Differential operational amplifier



Analogic Part

- Results with Differential operational amplifier

Analogic Part

- Other problems with this scheme
  - Not possible to have controlled impedance seen by the delay lines. (Impedance depends on both voltages on + and - inputs). This leads to ask for high impedance and terminate with a resistor.
  - Possible to ask the system to have Va=0, but then the relation between positive and negative sides is removed and capacitors act separately and end up never discharging themselves.
  - It is not possible to make the system work with this scheme. We may find a possible solution.

$$V_a = \frac{2V_{CM} + \alpha'^{-'} V_i'^{-'} + \alpha'^{+'} V_i'^{+'}}{2 + \alpha'^{-'} + \alpha'^{+'}}$$

Analogic Part

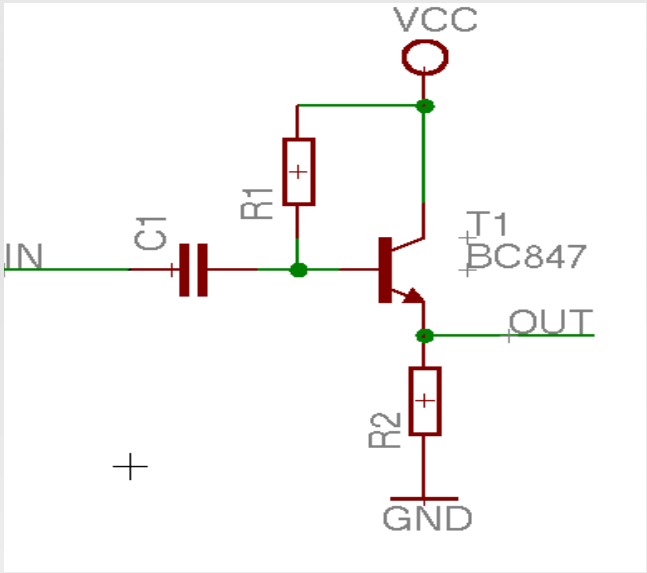
- Alternatives
  - Using and impedance adaptation. Like for example a common collector BJT and very few components.
    - Should take a look on the component matching problems it could lead to.
  - Using different scheme
    - Anatoli's one has the problem of not being differential. Approximately same power consumption. He has a Prototype. Noise performance?
    - Other schemes have been taken into account, but still it hasn't been found one good enough to replace the current one.
    - Completely duplicated differential solution, it implies duplicating the delay lines, not easy to fit in the available space.

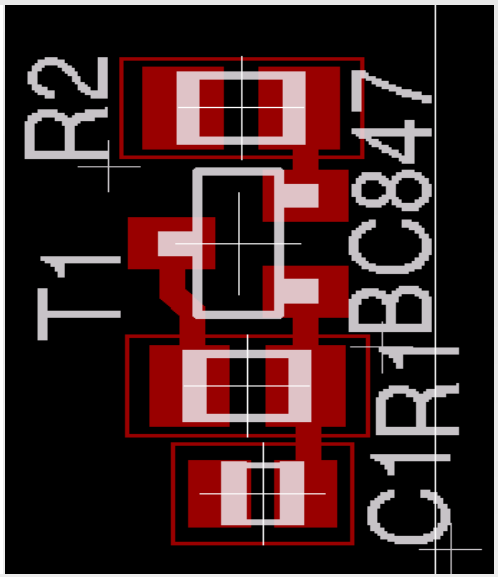
Analogic Part

- Impedance Adaptation
  - Using a common collector BJT is an inexpensive way to do this.
  - A good candidate could be a BC847C, that is fast enough (100MHz) and is only 3X2,5 mm. We would also need 2 resistors and a capacitor (none of them dissipates much power so it could be small smd).
  - The actual calculations estimate about 230KΩ input impedance and about 2Ω output impedance with 3mW power consumption. Also variations on such extreme values may not be important for the design.

Analogic Part

- Schematic of the adaptation system





- Equations of the system

$$Z_B = R_B \| (r_d + R_L)(hfe + 1)$$

$$Z_{OUT} = R_L \| r_d + \frac{Z_0 \| R_B}{hfe + 1}$$

$$r_d = \frac{hie}{hfe + 1}$$

$hie \approx 100$
$hfe \approx 500$
$r_d \approx 0.2$
$R_L \approx 1\text{K}5$
$R_B \approx 416\text{K}$

$Z_B \approx 230\text{K}$
$Z_{OUT} \approx 2$
$Gain \approx 1$
$C \approx some\ nF$
$Power\ Consumption \approx 3\text{mW}$

Analogic Part

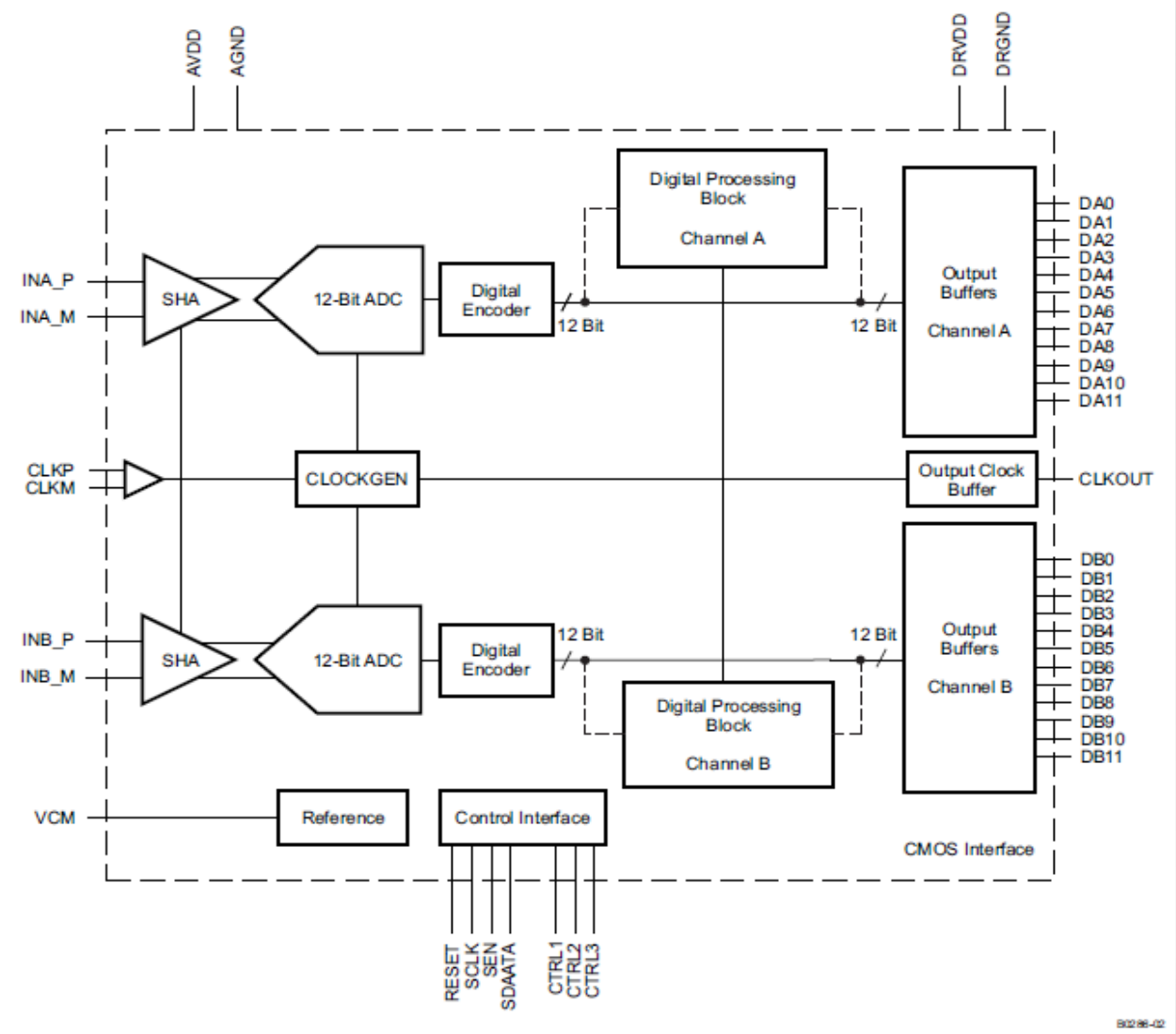
- Comments about this option
  - This circuit is inherently non linear. It should be linearised by fitting the error down to an acceptable value, which is quite low as we are attempting to use 12 bits ADC.
  - It may have problems with noise coming from the power supply and may be affected by small variations of it.
  - There should be a study about the dispersion of parameters in the transistors and how would it affect to the precision of the system.
  - All these handicaps make this option not desirable.
- Status of the analogical part
  - Nowadays Anatoli's way is the only one working fine. Although it needs one more OP amp and consumes a bit more of power than the other ones it is still the best one in performance.

ADC Selection

- In order to make the proper interface between the analogical part and the ADC it is necessary to have it previously selected.
- Our ADC needed 12 bits resolution, at least 40MHz conversion frequency and it was also desirable a small package due to space restrictions.
- The more suitable components for our application where:
  - Texas Instruments ADS6122
    - 1 ADC/Chip but 5x5mm only, LVDS, DDR!
  - Texas Instruments ADS6222
    - 2 ADC/Chip, LVDS, DDR!
  - Analog Devices AD9238
    - 2 ADC/Chip, LVTTL.

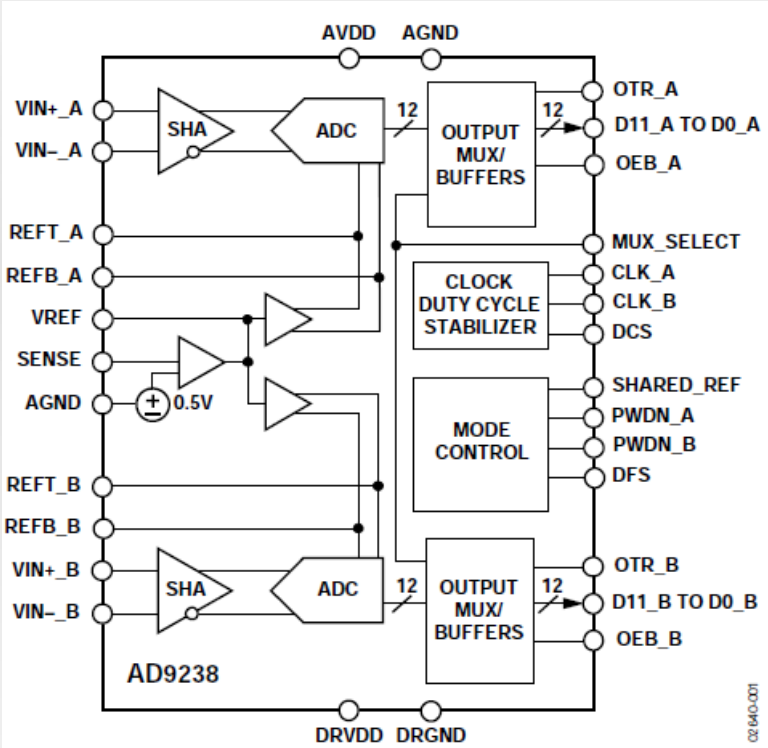
ADC Selection

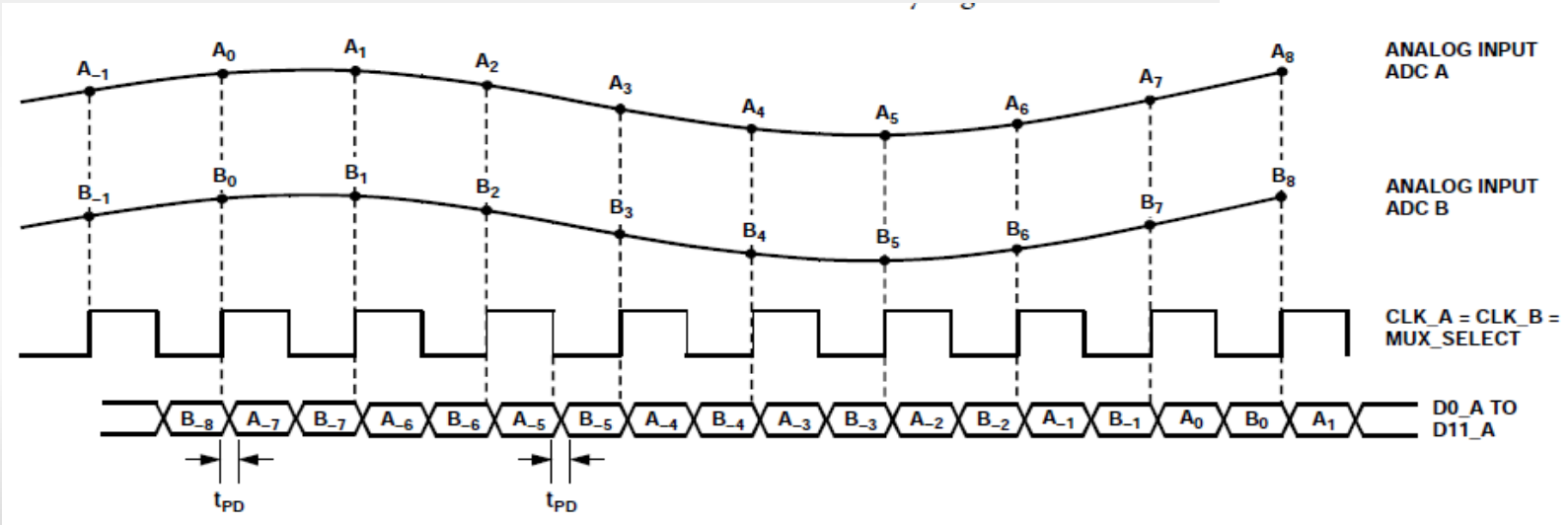
- Texas Instruments ADS6122 / ADS6222



ADC Selection

- Analog Devices AD9238
  - One sampling clock per channel
  - Optional multiplexing
  - No RAM configuration





ADC Selection

- Texas Instruments ADS6122/ADS6222
  - Both options very interesting because of LVDS and DDR, this meant having the advantages of LVDS but using the same amount of wires. The problem was that it had RAM configuration problematic with SEU. It may be solved by being aware and reconfiguring if needed but is uncomfortable. Also the dual ADC has single clock, so only useful if switched system used, not useful for delay lines system.
- Analog Devices AD9238
  - Easier option than the other ones, it also has a multiplexing feature that could be used in switched mode and would save half of the wiring.
  - One clock per ADC, suitable for all options.
  - It is selected as the baseline for our application.

Analogic Prototype

- Analogic prototype in progress
  - A first prototype was planned, it should be useful to:
    - Measure real errors and noises
    - Help with the digital part test by generating realistic inputs for them
    - Test if the architectures have any flaw
    - Realistically measure power consumption
    - Give an idea of the space needed
  - The idea is a mezzanine that will connect to a digital “mother board”.
  - The final design is thought to be 8 channel board it helps both testing a whole FPGA and the interaction between different channels.

Analogic Prototype

- Drawing of the prototype