Laboratoire de l'Accélérateur Linéaire (IN2P3-CNRS) Orsay, France

Olivier Duarte

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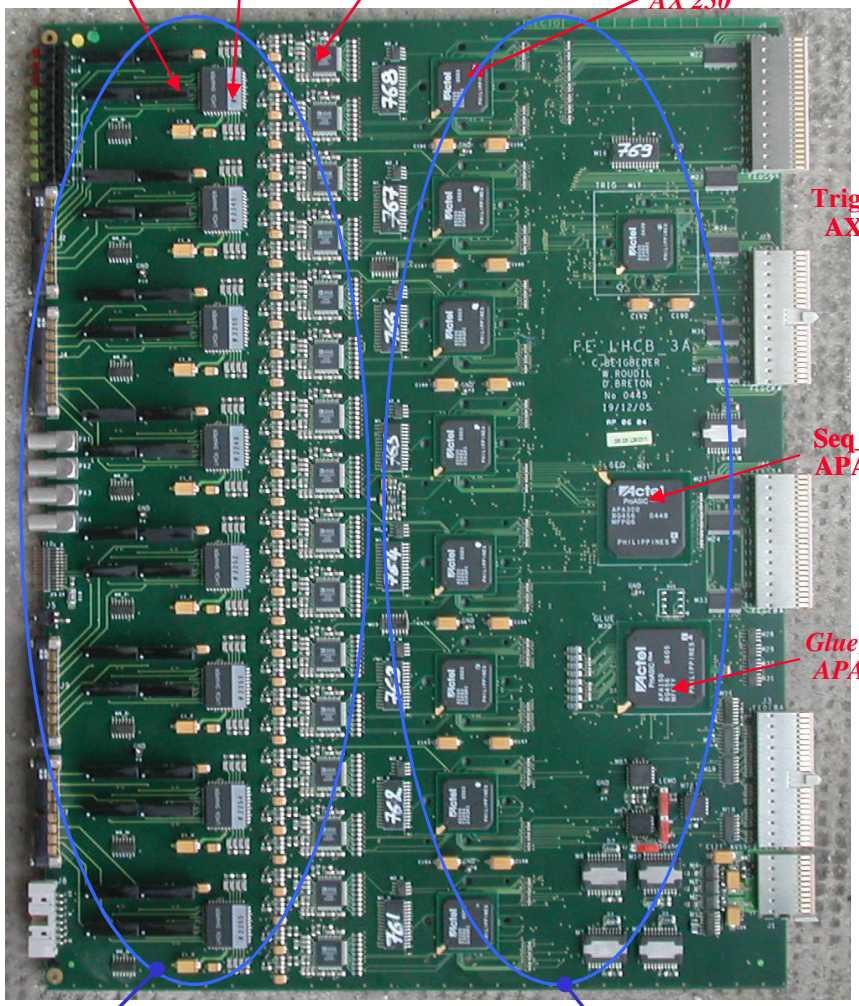
FEB Upgrade digital Electronics status

- LHCb FrontEnd board and upgrade
- Choice of the FPGA family and target
  - Requirement and choice of the FPGA family
  - Requirement and choice of the target
- Choice of the target : A3PE1500
- A3PE1500 post layout simulation
  - Implementation of the current firmware inside A3PE1500
  - Implementation of specifics functions that will be used for the data compression
- Necessity of a test board
- Test board architecture
- Test board schedule

LHCb Front-End Board and upgrade



Curent FEB

- *New Analog part : ASIC or discret (Barcelona team !)*
- *FEPGA :*
  - *Rad-tolerant and re-programmable Family (it's better and flexible) !*
  - *8 channels for each FEPGA (driven by the number of optical links)*
- *Optical transmitter on the board*
  - *GBT*

Upgraded FEB

Choice of the FPGA family and target

- Requirement and choice of the FPGA family
  - We want to use Rad-tolerant FPGA
    - ⇨ Implies Actel family Axelerator or ProAsic 3
  - The readout of the experiment will be done at 40 MHz, the component must do a lot of operations in 25 ns
    - ⇨ high speed components – Axelerator is the best !
  - It's easier to use reprogrammable components (flexibility)
    - ⇨That supposes ProAsic 3 Only !
  - For the "simplicity and legibility" of the architecture, we will use 8 Channels per FPGA and one optical fiber per FPGA
- Requirement and choice of the target (FE_PGA)
  - 32 Channels per FEB and 4 FEPGA
    - ⇨ Size of the chip (large number of IOs)
    - ⇨ cheap chip (up 1100 chip)
  - Data compression and standard IOs of the GBT
    - ⇨ Number of IO Bank (one standard per bank !)
    - ⇨ Number of block RAM (the compression will use a lot of RAM Block)
    - ⇨ Speed of the components

Choice of the target FPGA : A3PE1500

- A good candidate A3PE1500
  - Advantage
    - Reprogrammable
    - …

ProASIC3E Devices	A3PE1500
Cortex-M1 Devices	**M1A3PE1500**
System Gates	1,500,000
VersaTiles (D-Flip-Flop)	38,400
RAM kbits (1,024 bits)	270
4,608-Bit Blocks	60
FlashROM Bits	1,024
Secure (AES) ISP	Yes
Integrated PLL in CCCs[1]	6
VersaNet Globals[2]	18
I/O Standards	Pro
I/O Banks (+JTAG)	8
Maximum User I/Os	444
Speed Grades	-F, Std., -1, -2
Temperature Grades	C, I
Single-Ended I/O / Differential I/O Pairs	
PQ208	147/65
FG256	
FG324	
FG484	280/139
FG676	444/222
FG896	

  - Disadvantage
    - No debug tools as silicon explorer for AX
    - SSN / SSO problems ! (Simultaneous Switching Noise Simultaneous Switching Output)

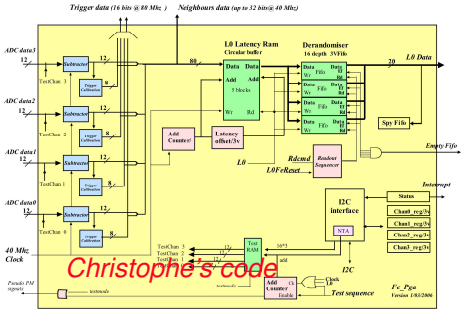
- SSN (Simultaneous Switching Noise)
  - When too many bits flip altogether and quickly, the signal seen after the input buffers of the FPGA are corrupted. This is hardly documented by the manufacturers and the acceptable limit (number of bits flipping, average rate) depends on the implementation.
  - SSO reduces the performances of the chip

- Backup solution AX family !

But problem with the number of block RAM, maximum 16 blocks in AX500 !!

Data compression possible ?

A3PE1500 : post-layout simulation



Christophe's code

- Implementation of the current firmware inside A3PE1500

Compile report:

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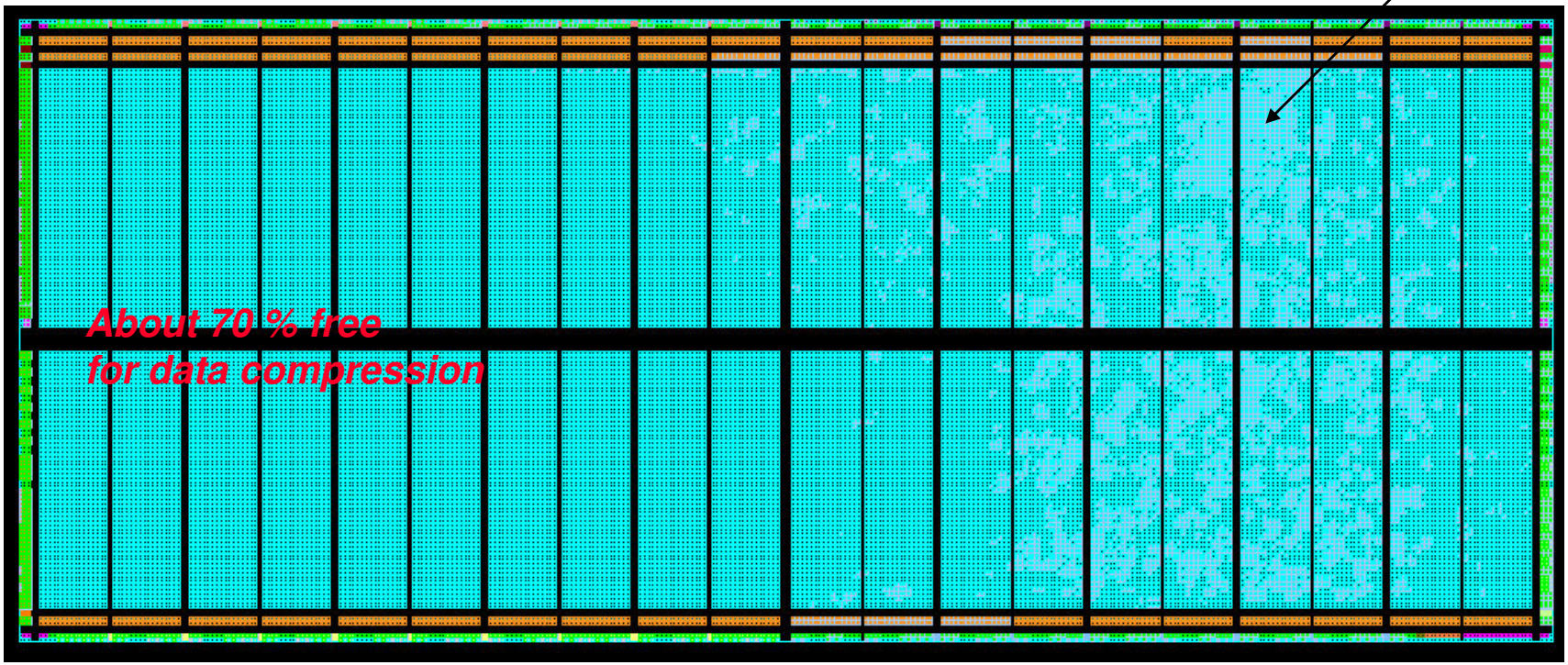
CORE	***Used:***	***5374***	Total: 38400	(13.99%)
IO (W/ clocks)	***Used:***	***147***	Total: 280	(52.50%)
Differential IO	Used:	0	Total: 139	(0.00%)
GLOBAL (Chip+Quadrant)	Used:	6	Total: 18	(33.33%)
PLL	Used:	2	Total: 6	(33.33%)
RAM/FIFO	***Used:***	***16***	Total: 60	(26.67%)

…

Occupancy rate (4 channels)



A3PE1500 : post-layout simulation

- Implementation of specific functions that will be used for the data compression

(actel Macro was used no custom implementation)

- 12 bits counter ⇨ maximum speed 205 MHz
  (86 /~38 400 VersaTiles {basic cell} used)

- Writing and reading RAM in different configurations (aspect ratio)

(We wrote the block RAM in size of 8x512 bit and read in other size 1x4k bit)

- Multiplexer and adder ⇨ maximum speed 131 Mhz (-2)

(109 / ~38 400 VersaTiles used)

It should be possible to increase the performance of the function by “a custom" multiplexer and adder

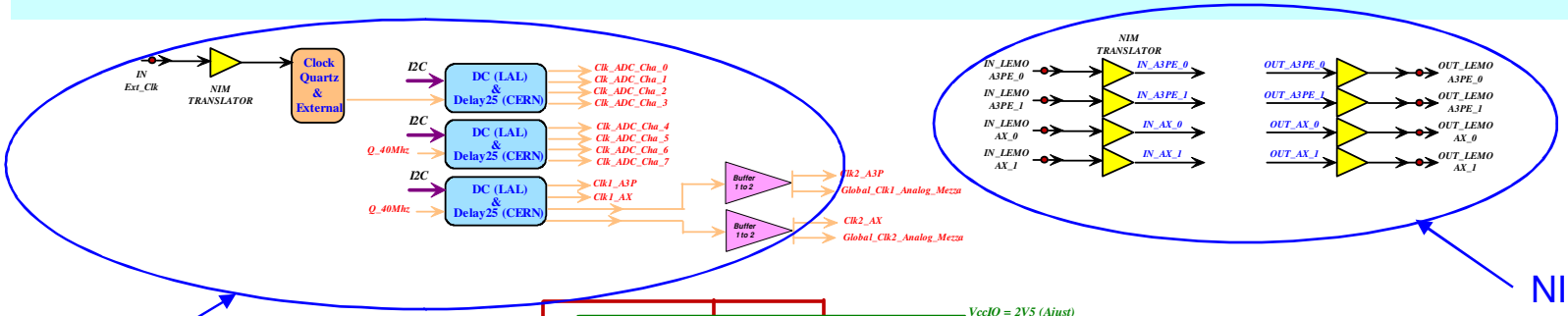
Necessity of Test board

- If we want to used a A3P family, it is necessary to test many major characteristics of this components
  - SSO : It is imperative to measure this effect on this new family, because if this problem is important that require major modification on the design of the board
  - I/O configurations / bank
    - ⇨ There are a lot of possible standards, but generally a single one per bank
  - Maximum speed of specific function for data compression
  - On the CROC board with the ProAsics Plus family we have a lot of timing problem. We must check this part with the A3P family

- With this board we will test time adjustment with Delay chip

- This test board will do the readout for several analog mezzanines (based on delay line and switch methods)

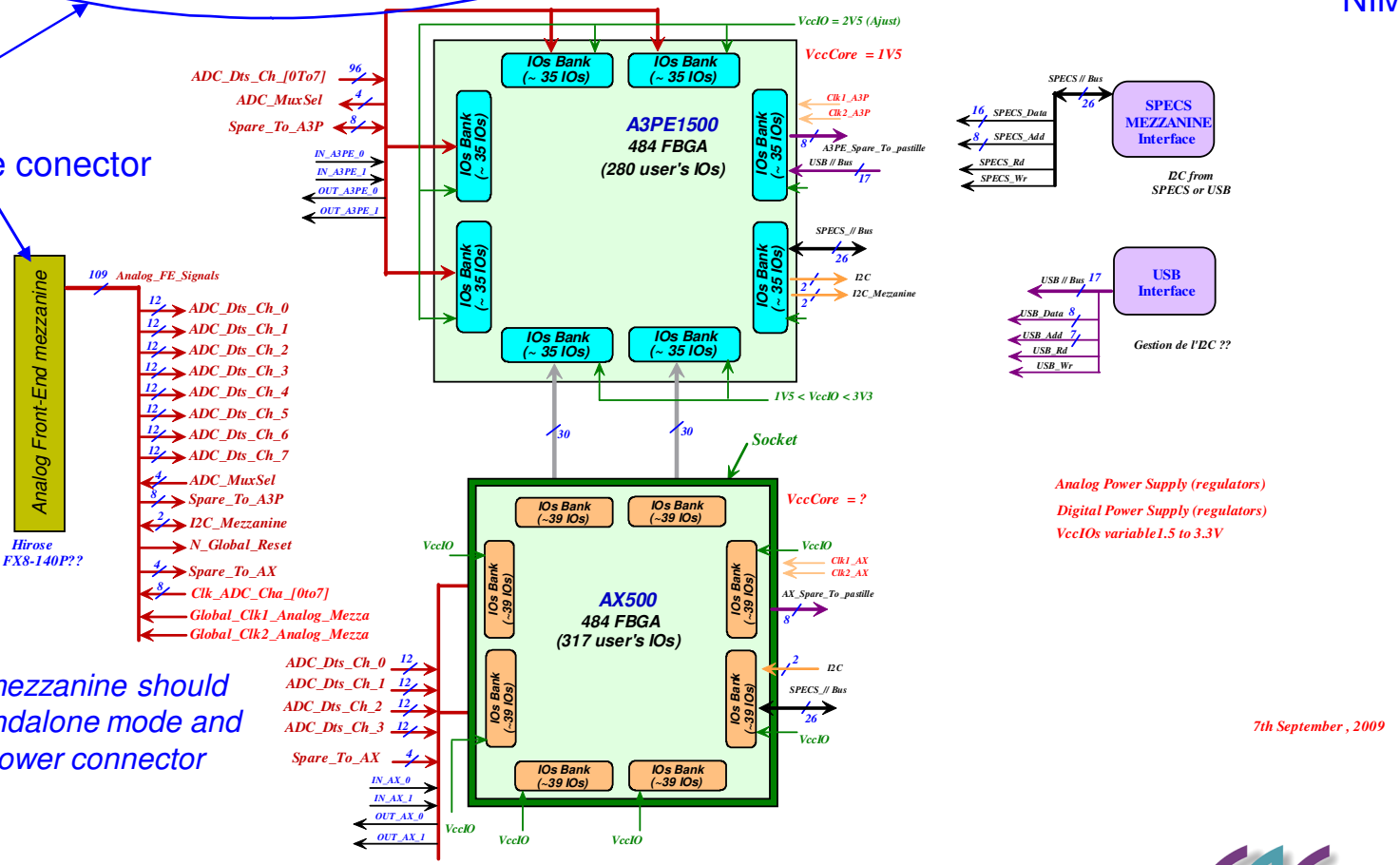
Test board architecture



Clock Tree

NIM I/Os

Mezzanine conector



The Analog mezzanine should work in a standalone mode and has its own power connector

Analog Power Supply (regulators)
Digital Power Supply (regulators)
VccIOs variable1.5 to 3.3V

7th September , 2009

Tests board schedule