# SPD status and last operations

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- Cable Problems
- Temperature Probe Calibration
- The phase of the MIERDA line for time alignment
- Noise levels
- Plans



## Cables problem

- Communication problems between some CB and VFE due to control/clock cables problem addressed long time ago.
- A bundle of 4 cable got jammed between the 2 cable chains. The bundle somehow got stretched and was able to sneak to one side of the cable chain.
- Repaired "in situ" by cutting ~10 cm and soldering back.
- One of the repaired cables still showed failures in the reflectometer when shaking.
- 3 other spare cables in use. Two of them with a 5m extension at the Gantry.



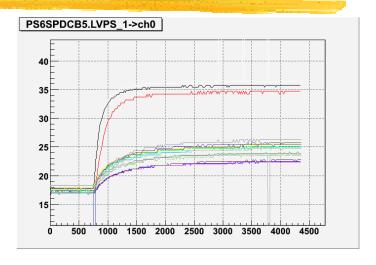


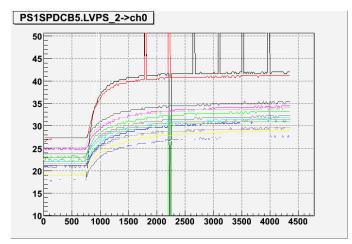
Thanks to Albert for his great work on top of the cherry picker and to Pascal for all his support and nice pictures.



### Temperature calibration 1

- Theoretical calibration curve:
  - T = A\*S+B
  - S = ADC reading
  - $A = 0.4588 \pm 0.014$
  - B = 279.38 ± 15
- We had calibration values for side A, not for C.
- We tried to find a way to do a rough and reliable estimation of the calibration curves for side C. Read the temps. at two different stable points.
- We've found some other issues: glitches in the readings with a periodicity of 440 s. To be understood a bit better but Albert claims that it is a feature of the RB. This implies that we'll have to implement a kind of filtering or re-try mechanism.

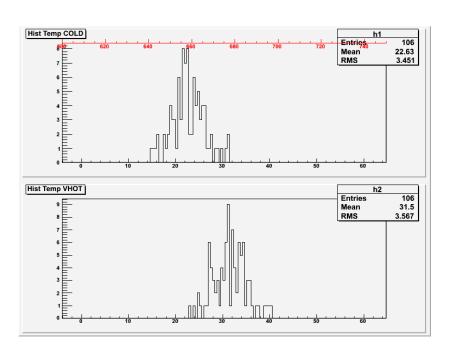




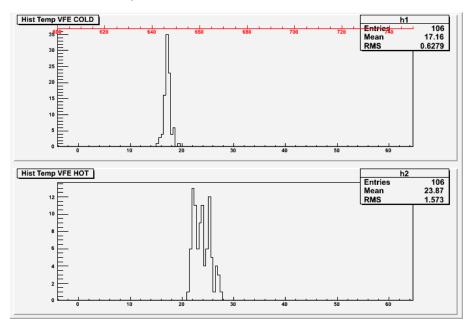


### Temperature calibration 2

# Histogram side A, theoretical temperatures.



Histogram side A, old calib. RMS is smaller, but the mean differs considerably from the theo. values



 The values obtained with the calibrations are much more reasonable: <temp> closer to real mixed water temp. and RMS lower.



### Temperature calibration 3

- We need two points to define the curve:
  - 1st point: when the electronics is cold.
  - 2<sup>nd</sup> point: when the electronics temperature is stable after long time running.
- We will assume that all the boards are at the same temperature in both cases, which is less true for the 2<sup>nd</sup> point...
- We have the ADC readings, but which is the real temperature?. We decided to use the values obtained with the old calibrations, the RMS is lower which indicates that the measurements may be better. That is: 17.5°C and 24°C for the VFE and 17°C and 35.5°C for the regulators boards.
- It's not that bad, we only want to know whether the boards are burning (overheating for the refined people) or not, ☺
- We will remove the dead channels.

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#### Phase of MIERDA line

- In order to time align the VFEs their source clock will be delayed in the CB by means of the delay chips.
- The MIERDA line carries fast control signaling for the VFE.
   Basically the VFE sub-channel reset. This signal has to arrive at
   the VFE with the right phase wrt to the clock in order to be
   latched properly (no timing violations).
- The CB only allows to time shift the MIERDA line by half a period. The results show that the half a period is actually 8 ns...
- After the VFE optimum timings are known we have two choices:
  - Try them and see if any VFE doesn't respond properly. Not very gentle...
  - Know beforehand which are the not valid ranges for the clock phases.
     We're currently measuring it for all of them (40/100 done).

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# Sample of phase measurements

VFE	PRSO, CB16	Invalid rank	PRSO, CB5	Invalid Rank
0	Bot	[13,17]		
1	Bot	[13,16]	Bot	[10,17]
2	Bot	[13,16]	Bot	[8,15]
3	Тор	[14,19]	Bot	[10,16]
4	Тор	[13,20]	Тор	[16,18]
5	Тор	[16,20]	Тор	[17,21]
6	Тор	[16,21]	Тор	[17,20]
7			Тор	[17,19]

- There is no real difference between long and short control cables.
- Where we had the cable extension the range spans over ~ 8 ns.
   That's quite undesirable as we can only time shift ~8 ns.



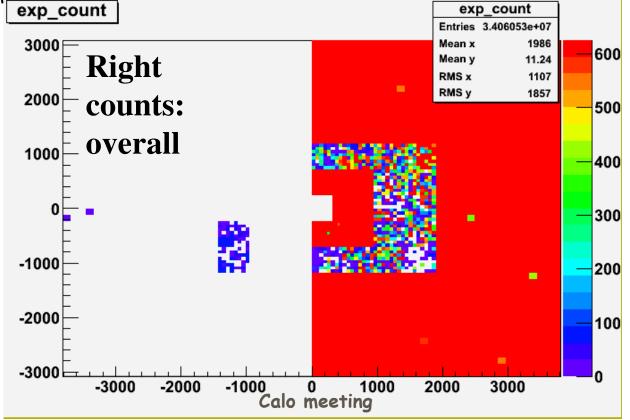
- Alessandro is developing a task for the calibration farm for led data monitoring for the SPD
- First tests done with some specific runs. Results commented in following slides
- Problems found:
  - Calibration B signal doesn't work. The calibration command is hardcoded in the Odin, it doesn't take the value in the PVSS panel. Richard promised to fix it soon.
  - Some timing issues found. Many of the events found in previous. A timing scan revealed a timing shift of 25 ns. Addressed to a bug in the TFC system. We have to repeat the timing scan and set the proper timings.
  - Many channels do not "flash" always or at all. Around 25% in side A and few single channels in side C.Our guess is that it has to do with the led bias.

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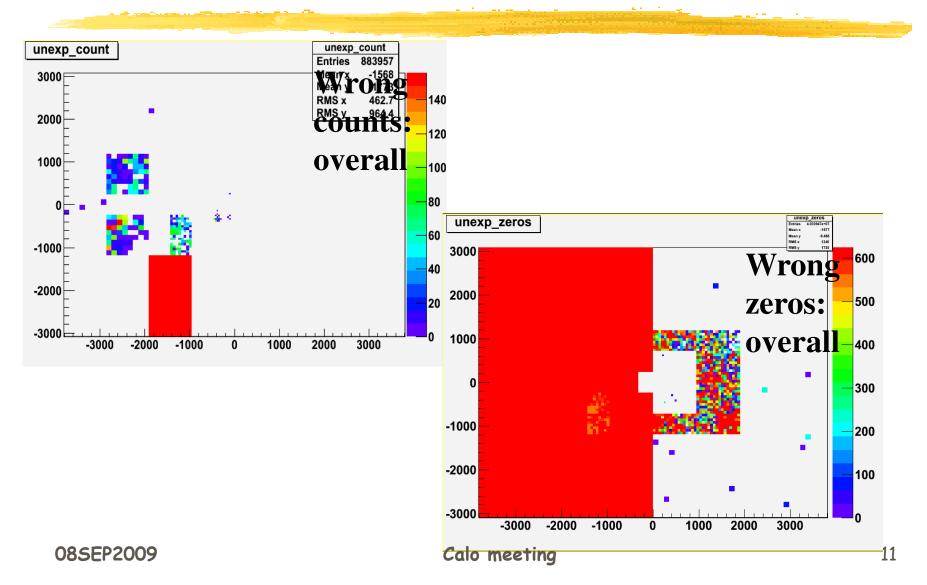
## LHCb LED Run 50932

- N. events: 10K (5K with even bx ID)
- No data for odd subchannels

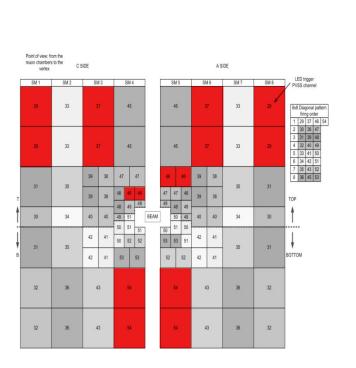
C side almost dead exp\_count

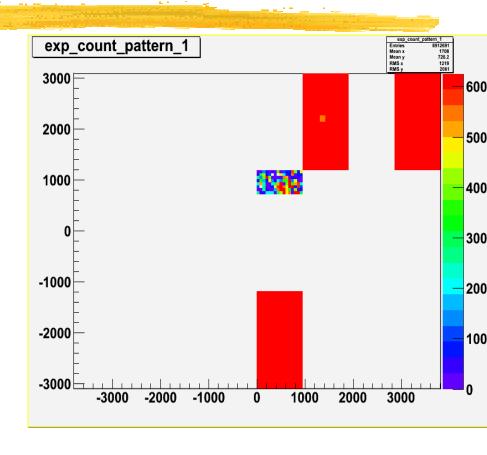










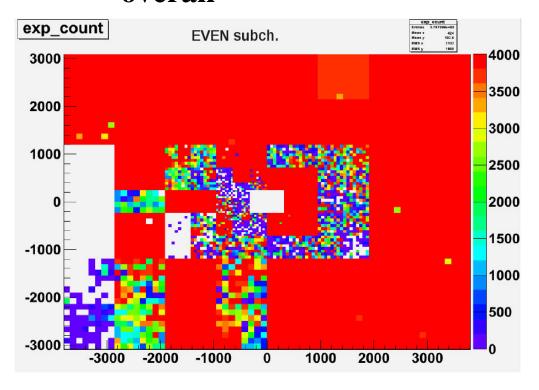


Example of a correct count cumulation for a single trigger pattern. (trigg. pattern #1)

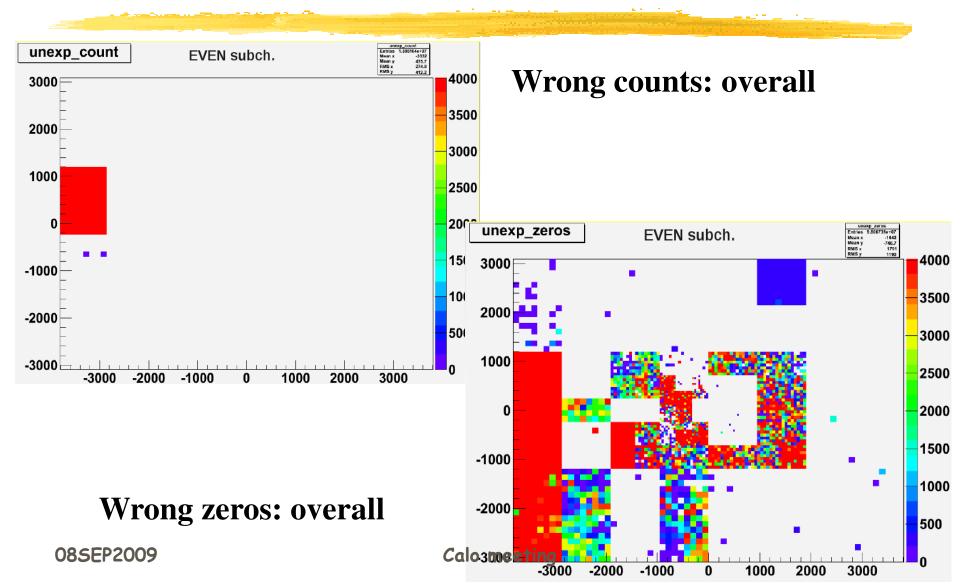


- Run # 52866
- N. events: 32K (~100% with even BXID)
- 1 event with odd BXID
- C side ~OK, but still worse than
   A side

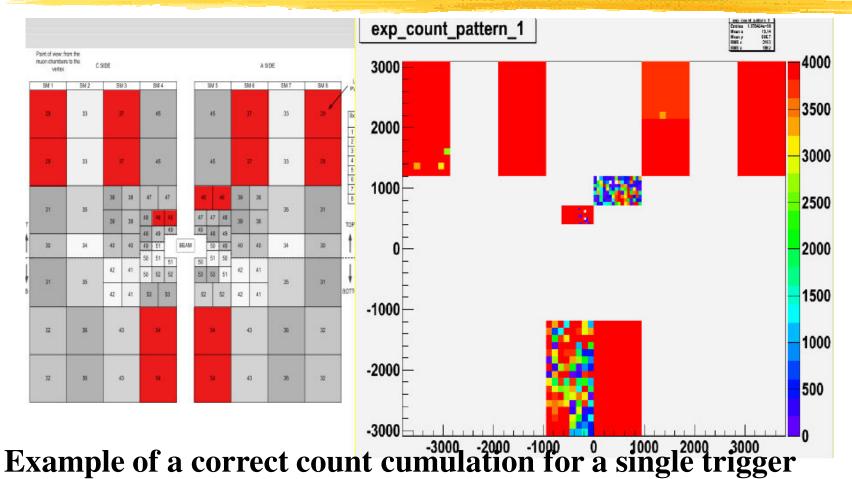
# Right counts: overall









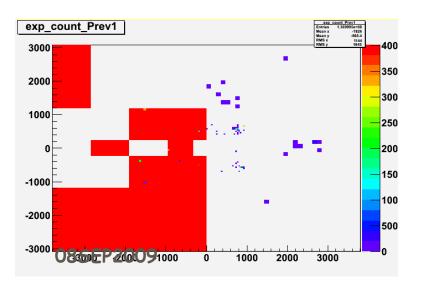


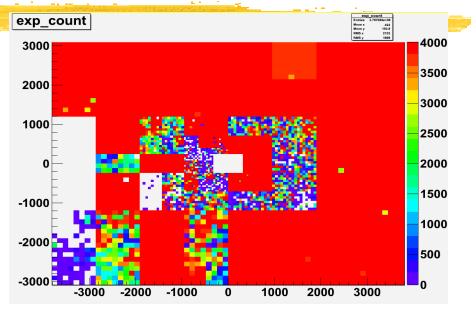
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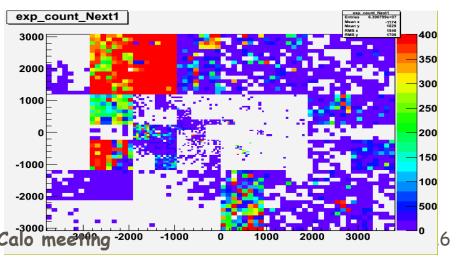


Total cumulate of correct counts at T0, prev1 and next1

#### **EVEN subch. - T0**

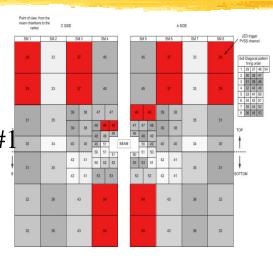


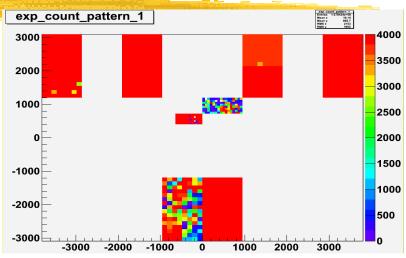




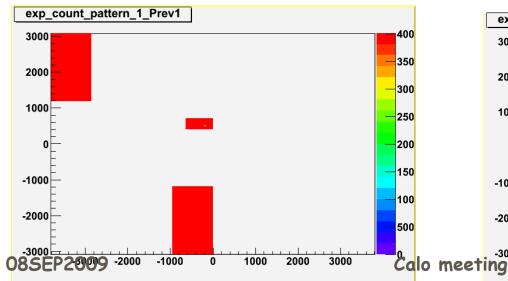


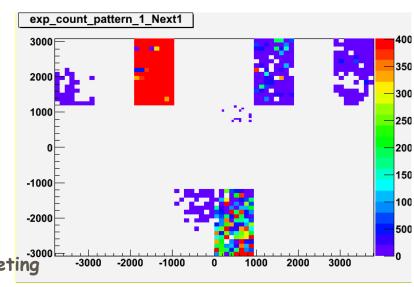
Total cumulate of correct counts at T0, prev1 and next1 for single trigger pattern #1





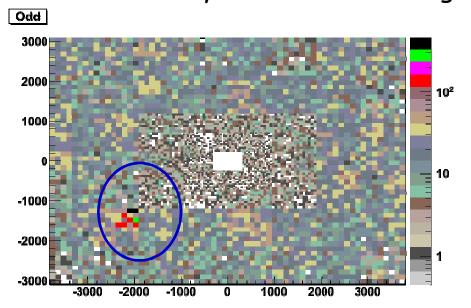
#### **EVEN subch. - T0**

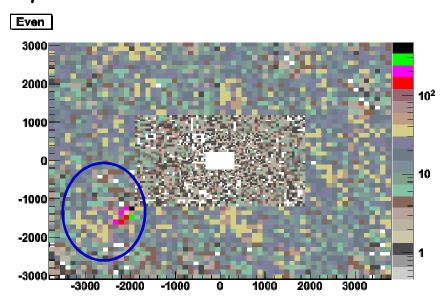






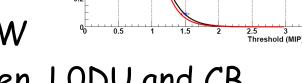
- Run triggering on SPDmulti>0 (thanks to Patrick R.)
- 109k evts / 400 Hz = 272 s =  $1,09 \cdot 10^{10}$  BXs sampled
- "Hot" VFE ~ 4 noise count /  $10^8$  BX  $\Rightarrow$  no problem
  - Will try to understand origin anyhow







- Perform a cosmic campaign
  - Check last changes in the HV
  - Efficiency study: 1.5-3M event
- Continue with LED monitoring SW



Theoretical efficiency as a function of threshold

- Synchronise dead BXIDs between LODU and CB
- Apply the temperature calibrations.
- Continue with MIERDA line measurments.
- Plans for time-alignment and calibration with first data in tomorrow's session