CALO HV system and HV Status bits board for ODIN

Outline

- Firmware upgrade of the HV_LED_DAC boards.

- HV Status Bits board. Status of the board integration into the LHCb TFC system.

Firmware upgrade of the HV_LED_DAC boards

Last weeks a firmware upgrade of the ACTEL FPGAs of the HV control boards have been done.

Reason of the Control Logic mezzanines FPGA firmware upgrade

The reason was to make the HV board initialization sequence in powering time more intelligent and safety for CW bases and the HV control boards.

New firmware allows

In powering-on time all DAC integrated circuits set to zero, the over-current protection relays set to ON and after a second the auto-protection hardware monitoring is automatically started. The time gap of order one sec is needed to exclude transitional current changes.

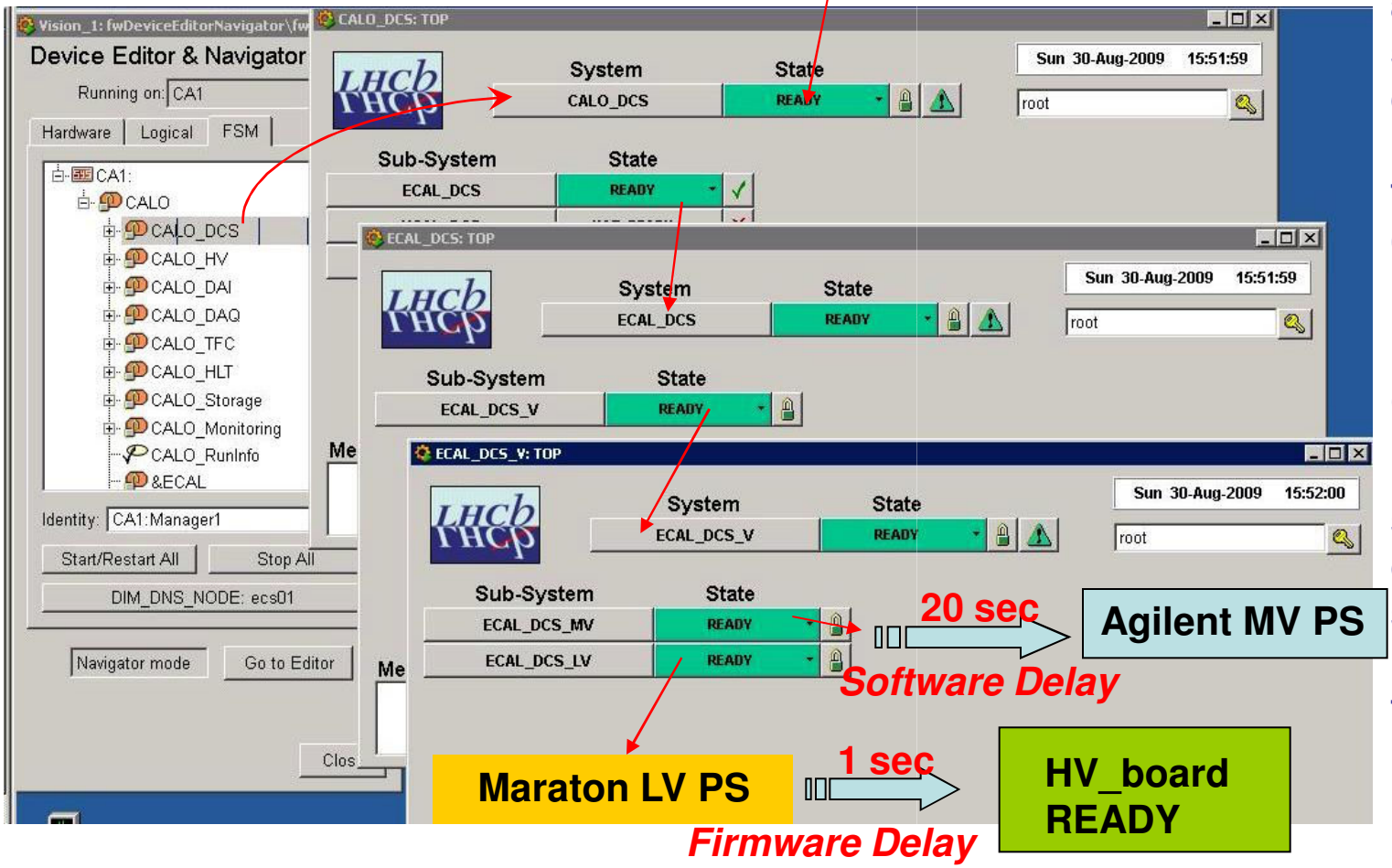
Summary

New firmware Version 7.0 has been developed (it's shown on HV-control panel now).

43 HV_LED_DAC control boards were upgraded and tested in last two weeks.

The Maraton LV and Agilent MV power supplies, dedicated to DCS partition, could be switch on now simultaneously from the CALO FSM top level tree.

Firmware upgrade of the HV_LED_DAC boards



Time sequence of the LV and MV supplies switching on, when the command "Switch_ON" is issued from the top of the FSM DCS partition (project CA1):

- Command is propagated to each CALO sub-detectors.
- LV and MV power supplies are switching on sequentially. LV is switching first with updated sequence and then in about 20 sec the MV is switched on too.

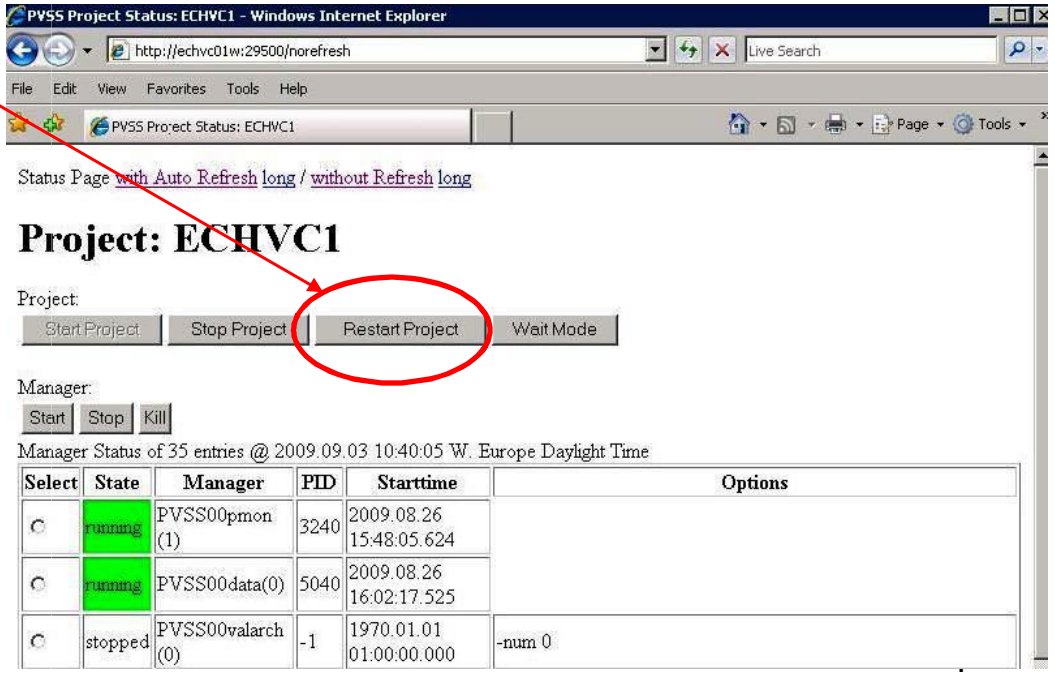
Screen-short of the CALO DCS panels shows how a "Switch ON" command goes from top to bottom.

Firmware upgrade of the HV_LED_DAC boards

Last time the HV recovering after power cuts was rather painful !

New procedure of the CALO HV system recovery after power cut.

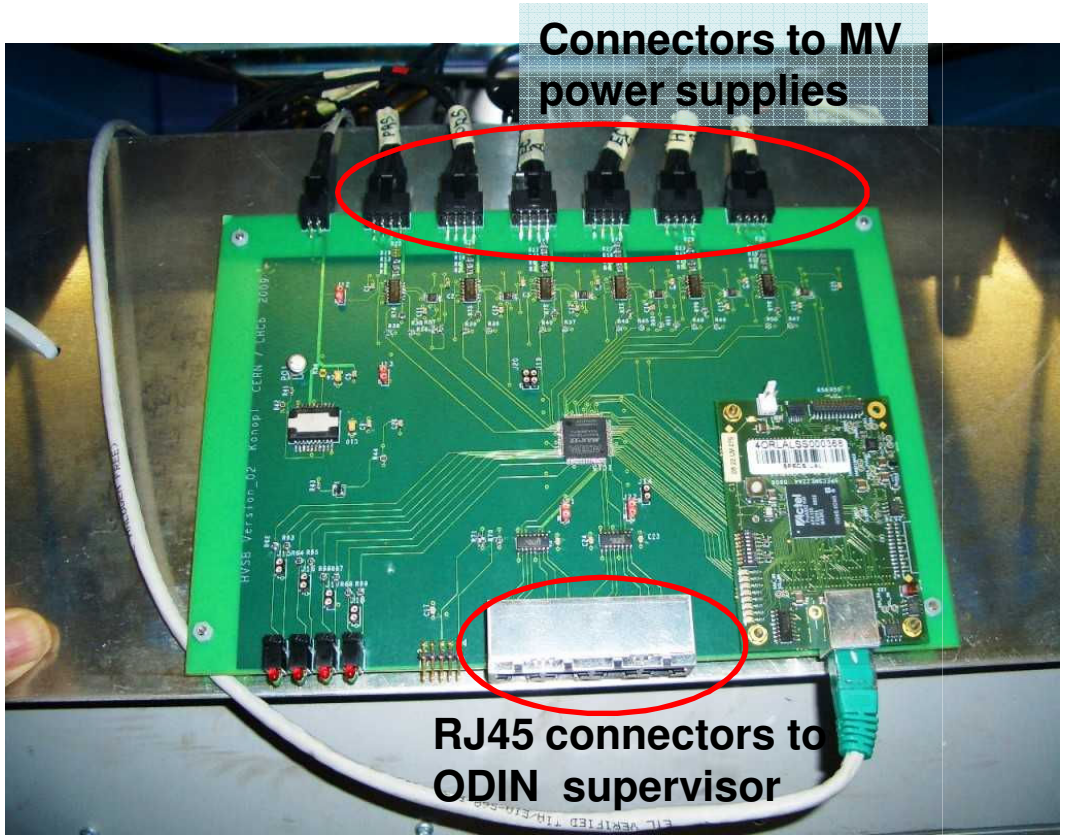
- Check FSM DCS tree is functional.
- Open the “CALO HV Status” panel.
- From FSM top level switch on all DCS power supplies for sub-detectors. (previous slide)
- Restart all CALO HV projects (PRSHVC1, PRSHVA1, ECHVC1, ECHVA1, HCHVC1,HCHVA1). There are two ways to do this. One is from Service+ of the dedicated online PCs and other one from shortcuts of the DetHVC1_Console
- Switch on the HV with needed recipe.



Screen-short of the ECAL side C HV project console

CALO HV Status bits for ODIN (hardware)

The CALO sub-detector HV Status Bit board has been developed, produced and tested. The solution is based on the MV power supply current measurement and sending the logical decision to ODIN supervisor for producing the data quality bits.



Final photo of the HVSB board.

HVSB board functionality:

- Fast measurement MV power supply currents.
- Produce the LVDS signals to the ODIN supervisor in case when the power current is out of range. Two decision bits are dedicated to each sub-detector (one bit per sub-detector side).
- Board is equipped with DACs, comparators and logic CPLD.
- The Specs mezzanine is used for DC levels measurement by DCU-ADC and communication with ECS.

CALO HV Status bits for ODIN (hardware)

Final installation

Additional LV +5 V Agilent power supply for HVSB board powering

Photo of the Agilent power supplies and HV Status Bit board installation into the rack.

CALO HV Status bits for ODIN (firmware)

Firmware

- The MAX-II ALTERA logic CPLD EPM240 has been chosen for implementation of logic function for producing a decision to ODIN supervisor.
- Logic implemented inside CPLD allows to mask any input channels, make needed coincidence and produce a decision output signal for each sub-detector.
- CPLD communicates with SPECS mezzanine through the PBUS.

List of the SPECS commands:

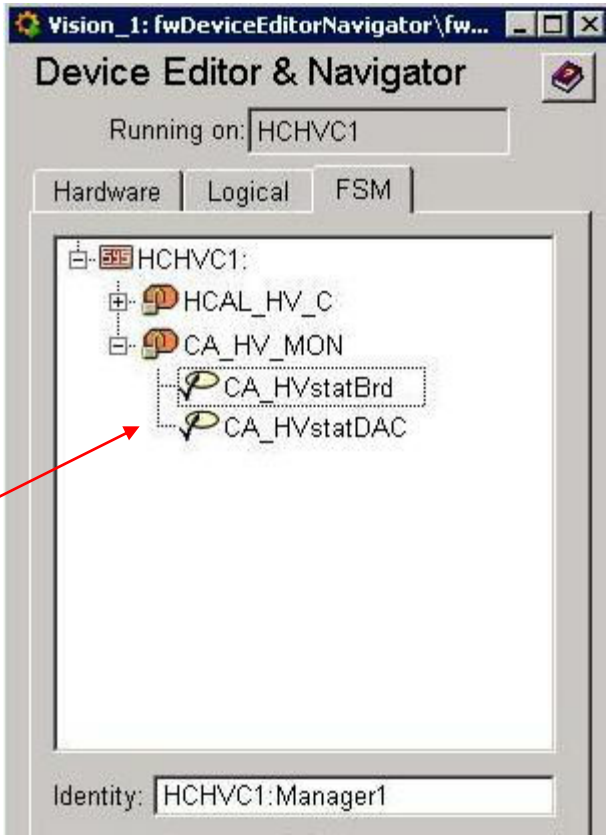
- PBUS write/read of the four 16 bit channel mask registers;
- PBUS write/read operation of the CSR (Status/Control Register);
- DCU read commands for six analog outputs of the current shunt circuits;
- I2C write/read operation for 12 DAC threshold settings integrated circuits.

CALO HV Status bits for ODIN (software)

Integration to ECS I.

HVSB board must be configured in initialization time and monitoring in run time. To allow to do this, the board was integrated into the CALO HV project. The following PC and PVSS project are used for HVSB board integration into ECS:

- HCDAQHVC01W PC has spares Specs ports and one of them is used now for interconnection with HVSB board.
- HCAL HV project HCHVC1 has been modified and additional device units CA_HVstatBrd and CA_HVstatDAC were build for HVSB board and added to this project.
- HVSB board configuration is performed simultaneously with HV settings load.



Updated DEN panel of the HCHVC1 project

CALO HV Status bits for ODIN (software)

Integration to ECS II.

HVSB board is powering from the Agilent +5V power supply. For control and monitoring this power supply it was integrated to CADCSMV project. The control unit CA_STATUS_LV and DIM server “agilent_serverPS5” were added into the project.

Agilent power supply was registered into Online DB with following parameters:

IP: 10.130.36.156 /psagil04.lbdaq.cern.ch/

MAC address: 00 – 03 – D3 – 0C – BA – 97

Updated DEN panel of the CADCSMV project

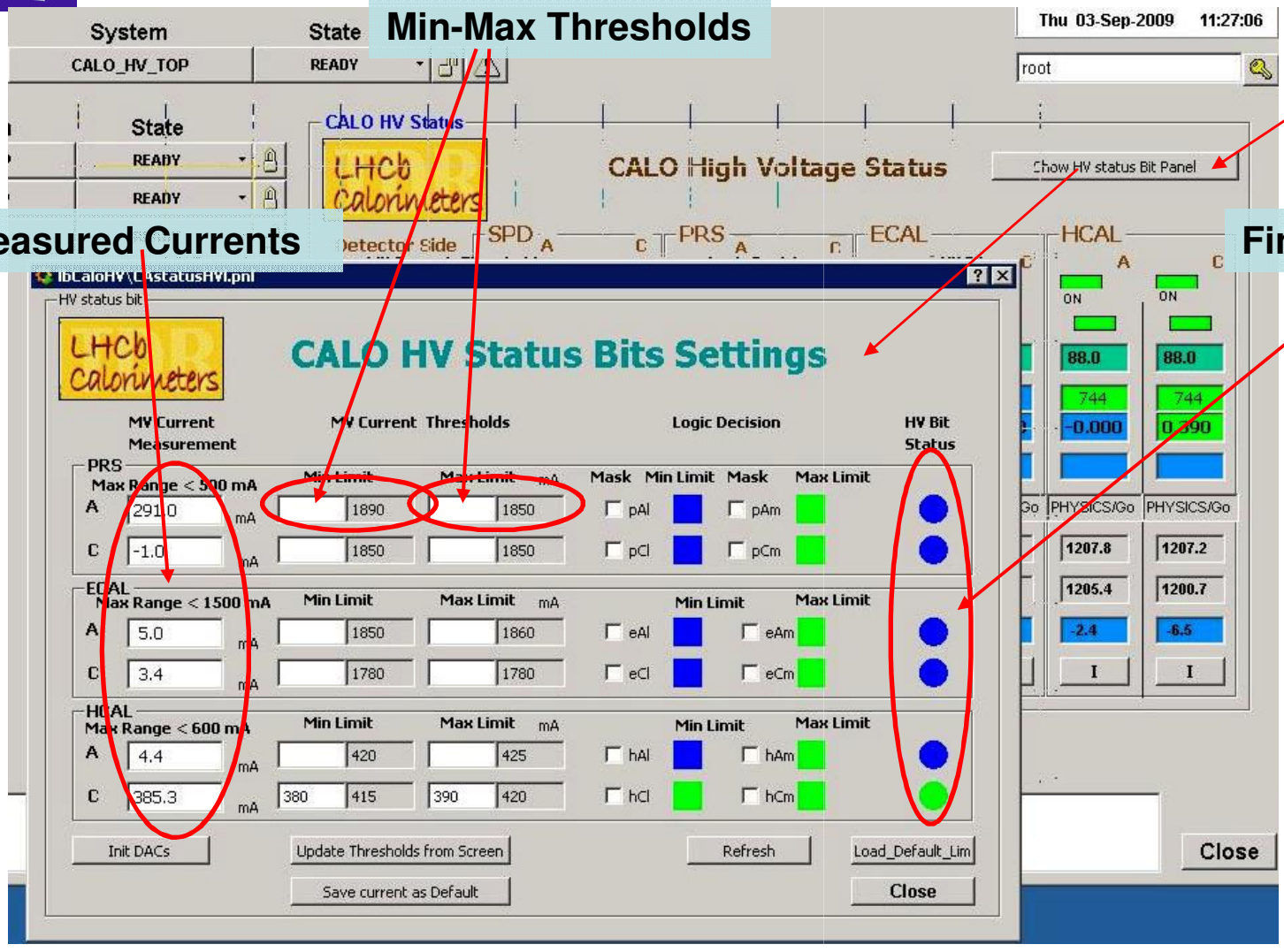
CALO HV Status bits for ODIN

Click on the button for open Panel.

Min-Max Thresholds

Measured Currents

Final HV Status



The Status is green when the power supply current is into a range between Min and Max threshold

Screen short of the panel for CALO HV status Bits board monitoring and control

CALO HV Status bits for ODIN

Conclusion

- Firmware upgrade of the CALO HV boards have been done. Now the procedure of the HV system recovering after power cut is much simple.

- The electronic board HVSB for monitoring the middle voltage currents and generating two status bits per each sub-detector for ODIN supervisor has been developed.
  - Two PCBs have been produced and one assembled, tested ant installed in D3 .
  - First version of a firmware for the control logic ALTERA MAX-II CPLD was developed and loaded.
  - LV power supply with additional cabling have been installed into the rack of the barrack D3 and integrated to ECS.
  - The designed HVSB board has been integrated to existing PVSS project and dedicated panel for the board settings developed too.

Planning

- Make a system test of the HVSB board with ODIN supervisor.