Status of CTF3 acquisition

Crate problems:

- Last month we noticed SPECS network problems on Mercury crate:
  3 last boards KO/4.

Tests showed a daisy chain transmission problem (swapping boards and timing measurements).

We still have to investigate why problems occur on a crate which used to work:

→ EMC problems: we recovered the 2nd board just connecting grounds.

→ occurred when current increased: radiations? Though rad-hard design.

→ Next shutdown several actions: cable length adaptation for timings, grounding…

→ LAL team developers of SPECS are interested to investigate the problems. They should come when accelerator will be open.

Currently, in Mercury 2 boards OK, 2 KO. Also 1 KO in Uranus.

Status of CTF3 acquisition

Crate problems:

- Finally, a solution could be to increase the number of network links and reduce the number of boards chained to 2: next shutdown, several network cables will be installed.

Mercury crate problem showed that a transmission breakdown can occur even it used to work for a long time.

At the end it should represent an additional cost of 1 gateway + 3 SPECS master boards + cabling: cost of peace?

Also a solution to run different timings on TBTS crates because of PCI conflicts (FESA crashes).

Status of TBL installation

1st part installation: end April.

1 crate “Titan”: 2 DFE boards + timings distribution + cabling AFE-DFE.

2nd part installation: W39 - W42.

3 crates ,12-13 DFE boards + timings distributions + cabling AFE-DFE.

All boards ready, waiting for CLEX opening to produce AFE-DFE cables (lengths).

Installation and tests foreseen the two last weeks.

Other.

- collaboration with Franck G. for a calibration mux. soft (Jean Jacquemier).
- modifications on 5 TBTS analog modules foreseen next shutdown to have both analog and digital readout.
- Acquisition documentation available on: http://hal.in2p3.fr/in2p3-00412457/fr/

R&D activities: prototypes

first tested prototypes:

- ADC evaluation board with both samplings (100Msps & 500Msps).

Tests and debug this summer: 100Msps 16bits solution works well. (ENOB≈12,5).

500Msps ADC does not work very well and ENOB=10bits (prototype).

- Tests on PCI optical transmission boards have shown the feasibility of synchronous data and machine clock transmission on a standard fiber and its repetition. Elimination of timing cables and timings boards possible.

- Design and tests of a local 10A/50Ω calibration current pulse generator proto.

3% Current regulated and good square shape. Rise time≈some ns.

Current should be locally regulated by the FPGA.

R&D activities: next steps

Architecture simplification:

At the beginning we foresaw a 6 ADC boards (4channels each) crate dedicated to the CLIC module:

> ***Crate:*** 6 ADC boards + 1distribution/repetition board + 1 local service board (power supplies and calibrations).
>
> + 1 PCI board for network (gateway).

After discussions with CLIC collaboration, the needs for one module and typical use in CTF3 allow to limit the acquisition to 4 BPMs by crate.

We think we can integrate these 16 channels on one single board: no more local network switch.

→ very important cost reduction: no local switch, only one PCB and FPGA, simpler network…

Currently, we study the performances of such an acquisition chain: estimation of possible dynamics, elimination of analog preamplification, local FPGA processing, network compatibility with future synchronous ethernet White Rabbit…

R&D activities: next steps

Next actions:

Technical discussions and specifications definition are foreseen with CLIC after the shutdown. As the future pick-ups are not well defined, the idea is to make a proposal with a “state of the art” technology for a low cost 100Msps solution.

We will propose to produce a prototype of the full chain: mid 2010.

→ small crate with 1 ADC board (4*4 channels) + 1 local service board.
→ PCI express optical network board (network distribution).

Could be tested in CTF3.
Collaboration should be formalized.