# WIT2010 Workshop on Intelligent Trackers

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Lawrence Berkeley National Lab

# Book of Abstracts

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# DC-DC Conversion Powering Schemes for the CMS Tracker at Super-LHC

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With conventional powering the increasing power requirements of the CMS tracker at Super-LHC cannot be met using the existing power supplies and/or cable plant. Therefore a novel powering scheme based on parallel powering with DC-DC conversion is foreseen for the CMS pixel detector at SLHC phase-1, and for the CMS outer tracker at SLHC phase-2.

We will present electrical studies (efficiency, EMC) and system test measurements with strip modules, using DC-DC buck converters with either custom radiation-hard converter ASICs or with commercial ASICs. Low-mass air-core inductors have been developed, and various filters methods have been compared. The presentation will include studies of the noise coupling mechanism and the detector susceptibility. Finally the implementation of DC-DC converters into the future pixel detector and outer tracker will be discussed.

**Development of specific components, for example low mass interposers / 3**

# A Silicon and Carbon Foam Low Mass Interposer

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We present prototype results for a new wafer integration component called a low mass interposer (LMI). The LMI prototype is an assembly of silicon and carbon foam resulting in a composite 4 inch wafer of 4 mm thickness and average density 10% that of silicon. Rows of vertical copper contacts traverse the bulk on 4mm pitch. Each row consists of identical contacts on 10 micron pitch. This results in an average contact density of 25 /mm^2 for this particular prototype. The contact and row pitches as well as the final thickness are arbitrary choices made for demonstration purposes. These parameters can be varied by factors of 2 or more within the construction process under development. The LMI is intended for copper-copper bonding to IC wafers in a 3D integration process. This prototype does not match any specific wafer design and was produced to develop a fabrication procedure and quantify the results. 3D integration tests using these LMI prototypes would have to be done elsewhere.

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# Design Evolution from 2-D to 3-D MAPS

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Swift, high resolution, thin CMOS Monolithic Active Pixel Sensors (MAPS) being developed by the IPHC and IRFU collaboration, have demonstrated their strong potential for tracking devices, particularly for flavour tagging.

The 2-D MAPS development has reached necessary prototyping maturity for real scale applications, through the recent realisation of a full scale swift and accurate sensor (MIMOSA26) optimised for the EUDET beam telescope. The 2-D MAPS are foreseen to equip several vertex detectors, such as for the STAR Heavy Flavor Tracker (HFT) upgrade.

The emerging 3D integration technology is expected to be particularly beneficial for MAPS. They can combine different fabrication processes and resorb most limitations specific to 2-D MAPS. Three prototypes have been designed by the IPHC and IRFU collaboration to explore its capacities.

The proposed talk will present the 2-D MAPS development and its extension to the 3D-MAPS.

**Coupled layer and monolithic architectures II / 6**

## Architecture of a module with transverse momentum discrimination for the CMS Tracker Upgrade

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CMS is currently studying solutions to build a new tracker capable of providing prompt information on high transverse momentum to the central level one trigger. This information is essential for the reduction of trigger rates at the projected SLHC beam luminosity.

The architecture described here aims at detecting high transverse momentum particles directly in the front-end modules. It assumes a system built with a few layers with this pattern recognition capability covering an area of between 10 to 20 m2. It is based on double-sided modules of 5x5 cm2 with sensing elements of about 100 by 2000 microns. Some 36 front-end chips of 16 by 8 mm2 would be mounted on two sides of the module with a floorplan resembling pixel front-end read-outs but with a considerably higher functionality built-into their logic.

The data adjustment and pattern recognition logic to be implemented in the front-end chips are being designed and presently described in Verilog. Entire front-end modules are also modeled using this language. The logic necessary to reduce large hit clusters, align the tracks in the Z-direction as to provide momentum matching in the phi direction and for momentum discrimination will be described.

A software environment capable of reading physics Monte-Carlo events, of simulating for these input conditions the behavior of the proposed matching algorithm described at the hardware gate level and to compare them with standard data analysis software will also be described.

A realistic power consumption estimate based on the number of active logic gates, the chosen VLSI technology and of the logic switching generated at the design luminosity will also be given.

**High speed communication / 7**

## New Optical Technology for Low Mass Intelligent Trigger and Readout

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We describe a number of new electro-optical technologies which would enable data transmission with very low mass and power. Extremely small optical modulators which can be integrated into CMOS chips would allow the mass and power of lasers to be displaced outside the tracking volume. These modulators could be used to pass data between tracking layers of order cm apart rather than mm, enabling very fine resolution on an angle trigger with silicon pixels. This might implemented

be as follows: External lasers would provide light which would be transmitted into the tracker by fiber or perhaps beams in air. The data from one layer would be imposed by the modulator, which might be incorporated into a multiplexer or processor chip. The data would be passed to the adjacent layer by beams in air, perhaps directly or with extremely small fixed mirrors. Photodiodes of the same SiGe technology as the modulators in processors on the second layer would receive the data. The modulators themselves use extremely low power, of order 50 fJoule/bit in one case. Versions which might be suitable for HEP are being developed by MIT and IBM. They could also be used to pass data out of a tracker at over 1 to 5 Gbit/sec with very low mass and power. In general these could be useful for data transmission on staves,

between staves,and out of staves. There is an ATLAS study of the radiation hardness of SiGe materials in CMOS electronics which is relevant to these modulators, and indicates that the materials would be suitable for use in an LHC upgrade. We refer to a group at MIT which has expertise at all levels of these optical issues from materials to devices to system aspects.

Another technology which looks promising is the use of light beams with no fibers. The technology will be different on different distance scales. Over distances of microns, communication between chips might be done directly with no external lensing. Over distances of cm, the use of MEMS mirrors for steering and switching has been demonstrated by Lucent. Over longer distances, the use of the MEMS mirrors with feedback loops which may or may not involve extra optical paths is being investigated

at Argonne. Low mass MEMS mirrors are also being developed at Argonne. Over the longer distances, some very low mass rad-hard lenses would be used. In all these cases, the mass of optical connectors is eliminated, and there is no fiber to be radiation damaged.

**Development of specific components, for example low mass interposers / 9**

## Development of Interconnect Technologies for HEP Applications

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HEP detectors are continually advancing towards higher segmentation of elements and higher complexity in assembly architectures. The task of interconnecting detector elements with readout electronics and with readout buses for such detectors poses new challenges and opportunities. We will address progress on several fronts: gold stud bonding, anisotropic conducting films, conductive epoxy stencils and flexible cable attachments. Some speculative concepts such as use of PDMS for single-die photolithography and as low-mass interposers will also be presented. Our work is aimed at generic R&D but focused towards detectors for the ILC and SuperLHC.

**Coupled layer and monolithic architectures I / 10**

## System Concepts for Doublet Tracking Layers

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Aspects of the overall design and components for coupled doublet layers will be considered. These include interconnect, electronic architecture, and services.

**High speed communication / 11**

## Wireless data transfer at 60 GHz

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The data transfer rate from highly granular tracking detectors are today limited by the available bandwidth in the readout links. This prevents the detectors from being used for fast triggering. To get the tracker to contribute to a fast trigger decision the data rate from the tracker has to be increased or the quantity of data to decrease. A higher data transfer rate can be achieved by increasing the the number of data links, the data transfer speed in the data link or both. The data quantity can be decreased by introducing in-detector intelligence.

In addition to the limited data transfer capacity, the semiconductor tracker geometry is not not optimal for triggering purposes. The trackers are built of independent layers that are not grouped in topological structures. The logical grouping is following the most convenient path of service routing rather than phi-eta that is preferred by the trigger.

Wireless data transfer may be a suitable method of solving many of the limitations for using the tracker for fast triggers. The WLAN market will in the future shift to the 60 GHz band to reach higher data transfer rates allowing for wireless transfer of HD video signals. The high speed links are low mass and low power for short distance data transfer. Further more the antennas can easily be integrated as surface integrated wave guides on present hybrid designs.

In this contribution we will present how 60 GHz wireless data transfer can be used in next generation trackers.

**High speed communication / 12**

## FF-LYNX: protocol and interfaces for the control and readout of future silicon detectors

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Future High Energy Physics experiments will have similar requirements with respect to latency, bandwidth, robustness against transmission errors and component failures, radiation hardness and power dissipation of hardware components. The FF-LYNX project started from the assumption that a general purpose flexible protocol implemented in IP cores available to future ASIC designers can fit these requirements. It can also address new requirements related to the low and fixed latency transmission of data to be used in embedded or remote trigger processors, providing a "standard" solution with obvious advantages in terms of development and production costs and homogeneity among the different experiments. The project is a collaboration among INFN-Pisa, University of Pisa, Department of Information Technology, and UCSB, Department of Physics. The project targets are:

-) development of an Integrated Simulation Environment (ISE) for the validation and characterization of protocols and interfaces;

-) definition of a protocol for the data acquisition and the distribution of the TTC signals;

-) implementation of the protocol in radiation tolerant and low power interfaces designed and developed in standard CMOS technologies (130nm, 90nm) and available to the designers of the integrated circuits for the future experiments.

We started from a detailed analysis of the requirements in the scenario of the LHC upgrades in collaboration with several groups involved in the design of future pixel and strip detectors and Front-End electronics. High level (System-C) models of the links have been developed to validate and characterize different protocols and interface implementations. Error injection in physical links and interfaces due to noise or radiation has been simulated and figures of merit (e.g.: Trigger Loss Rate, Frame Loss Rate) have been evaluated in different operating conditions. These models are the first building blocks of the ISE: sensors, Front-End ASICs, electrical and optical links DAQ and control systems and, possibly, embedded or remote trigger processors will be modelled and simulated together. The ISE will provide a powerful tool to evaluate the impact of any choice in terms of protocols, algorithms, architecture or technology on the overall detector performance.

The first version of the FF-LYNX protocol was released in July 2009 and will be described in detail. Key features are the integrated distribution of TTC signals and DAQ, the robustness of triggers and frame headers against transmission errors and the general structure of data frames, transparent with respect to different data types. Interfaces can be easily coupled to the core of the host circuits. They are compatible with different architectures of the control and readout systems and with different link technologies and speeds. Two channels multiplexed in the time domain are used for triggers and frame headers (THS channel) and data frames (FRM channel) supporting different data types. Different speed options (4xF, 8xF, 16xF; F = frequency of the reference clock) are foreseen. VHDL models of transmitter and receiver interfaces implementing the FF-LYNX protocol have been developed, simulated and synthesized in one high performance FPGA (Altera Stratix III). The design of a test circuit with interface prototypes in a commercial 130nm CMOS technology will start in March 2010 and a submission is scheduled for spring 2010.

A second version of the protocol supporting the transmission of data frames with low and fixed latency has been defined, it is currently under validation in the ISE and it should be released in January 2010. Simulation results will be presented on latency and efficiency in the "trigger" data transmission in different scenarios w.r.t. occupancy and link speed and possible architectures to readout "trigger" and "raw" Silicon data in future Trackers will be proposed.

**Coupled layer and monolithic architectures I / 13**

# 2-D PT module concept for the sLHC CMS tracker

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The CMS tracker at sLHC is required to provide prompt PT information to the trigger to maintain the 100kHz LHC level 1 rate. Simulations show that a promising technique to achieve this is by correlating hits in two closely spaced strixel layers (~ 1mm spacing, ~ 100 um x 2.5 mm strixels), the so-called stacked tracking approach. While direct vertical correlations between strixels is a possible method for constructing a module (the 3-D approach), simulated occupancies indicate that this can also be achieved by transferring cluster information to the edges of modules (the 2-D approach), where cluster information from both layers can be brought together to find correlations. We believe this will lead to a module design that could be simpler and cheaper to prototype and construct. We present the current status of the proposed 2-D PT module design, in terms of the logic architectures necessary to implement the required functionality, and associated power consumption estimates.

**Electronic circuits (3D and conventional) / 14**

# Towards a high performance vertex detector based on 3D integra-

## tion of Deep N-Well MAPS

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The development of deep N-well (DNW) CMOS active pixel sensors was driven by the ambitious goal of designing a monolithic device with similar functionalities as in hybrid pixel readout chips, such as pixel-level sparsification and time stamping. The implementation of the DNW MAPS concept in a 3D vertical integration process naturally leads the designer towards putting more intelligence in the chip and in the pixels themselves, achieving novel device structures based on the interconnection of two or more layers fabricated in the same technology. These devices are read out with a data-push scheme that makes it possible to use pixel data for the generation of a flexible level 1 track trigger, based on associative memories, with short latency and high efficiency. This paper gives an update of the present status of DNW MAPS design in both 2D and 3D versions, and presents a discussion of the architectures that are being devised for the Layer 0 of the SuperB Silicon Vertex Tracker.

**Coupled layer and monolithic architectures II / 15**

## A high efficiency readout architecture for a large matrix of pixels.

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Based on the requirements of new generation vertex detectors, we present an innovative readout architecture for a large matrix of pixels (A>1.2 cm^2) capable to sustain high data rates (~100 MHz/cm^2) with high efficiencies (> 97%).
The readout is based on the parallel sparsification of one entire matrix column per clock cycle. The scan logic activates in sequence only the columns that present hits. Time labeling is performed by the central logic that divides the incoming hits into precise time windows defined by a dedicated clock. The column scan algorithm preserves the time sorting of the hits during their extraction from the matrix, allowing a simple integration in a triggered system, though considering the data-driven nature of the chip. In this architecture, which is strongly horizontally parallelized, we introduced an additional parallelization subdividing the matrix into 4 vertical sub-matrices, each one provided with its own readout. A unique output stage implements a data compression algorithm based on the time&space sorting of the hits and it has been optimized for clustered events. The architecture has been described in synthesizable (Synopsys) and highly parameterized VHDL code. The validation process passed through several simulations. The efficiency results obtained by these simulations are presented.

**Applications of intelligent detectors I / 16**

## Concepts and validations of a pT based tracker trigger using single and double sensors strip modules using CMS data

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One of the proposed solutions for a pT based trigger at SLHC for CMS is based on the concept known as the "cluster width" approach, in which clusters produced by low pT tracks are rejected based on the width of the cluster shape, made either on a single strip sensor or a doublet of strip sensors by a suitable electronics logic at the level of the front-end. This information can then be used in many ways to provide first level trigger primitives.

These kind of modules are inexpensive, and coupled high-speed opto-electronic components this concept provides the simplest solution to the first level trigger for SLHC trackers. We will present the simulation studies aimed to optimize the concept, as well as the basic building blocks of the module and their connectivity. Finally we will provide the experimental validation of it by using data collected by the CMS Tracker during the Cosmic runs in 2008 and 2009 as well as the first collision data from the LHC.

**Coupled layer and monolithic architectures I / 17**

# Design and development of a micro-strip stacked module prototype to measure flying particles direction

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Experience at high luminosity hadron collider experiments shows that tracking information enhances the trigger rejection capabilities while retaining an high efficiency for interesting physics events.

The design of a tracking based trigger for SLHC is an extremely challenging task, and requires the measurement of the charged particle momentum at first level trigger. Simulation studies show that the measurement of the charged track momentum can be achieved by correlating hits on two closely spaced silicon strip sensors.

This work has been focussed on the design and development of micro-strip stacked module prototype and will discuss the technical challenges in the construction of modules made of two silicon micro-strip sensors stacked on top of the other and wire bonded to the same readout chip. Several possible sensor spacing and wire bond techniques will be presented.

The prototypes have been built with the silicon sensors and electronics used to equip the present CMS Tracker. Coincidences of signals collected from strips of top and bottom sensors are evaluated off detector.

We will present the tests performed on the prototype modules in terms of the noise performance of the proposed stack geometry and the full electric characterization and stability in time of the devices. Some preliminary results in terms of signal over noise and coincidence signal generation using cosmic rays will also be shown.

**Development of specific components, for example low mass interposers / 18**

# Development of Silicon Interposers

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We report on fabrication of prototype silicon interposers for coupling pixel detectors in high energy physics experiments. The interposers feature a high density of conductive through-vias with additional mass reduction achieved by etching large voids in the silicon where possible. We report results of electrical and mechanical evaluations of the devices.

**Coupled layer and monolithic architectures II / 19**

# VECTORS AND SUBMICRON PRECISION: REDUNDANCY AND 3D STACKING IN SILICON PIXEL DETECTORS

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It is traditional wisdom that a minimal number of silicon tracking planes must be used in the inner detectors, in order to avoid multiple scattering, large numbers of photon conversions and other disturbances upstream of the calorimeter. In this work it is shown that a silicon pixel detector with hundreds of successive, highly redundant measurement planes can provide extremely precise and detailed information. It is worth more study to determine trade-offs between gains in local precision and pattern recognition, and a degradation of the interaction products at the entrance of the calorimeter by the use of a 'redundant' device, with maybe some tens of layers. One obvious possibility is that such a redundant detector IS the entrance of the calorimeter. In the course of this work we observe also some interesting effects of secondary 'delta' electrons, which have a significant probablity to create corrupted position measurements along the trail. If these could be recognized and eliminated from the fitting procedure, an improved precision may result. At least one more point along the trails would be needed.

For the measurements two Medipix devices have been assembled closely together and results with this stack are described. With Medipix and Timepix detectors in the CERN H6 beam we illustrate a first voxelized detector system with full parallel readout, that can provide vector tracking with submicron precision, at very high densities of incident particles.

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Fig. 1 A frame (14x14 mm, 256x256 pixels) showing 3 beam muons and a vertical trail in the two back-to-back silicon pixel matrices. The horizontal GeV beam particles enter at the right, cross the central contact plane (a thin Cu foil) and exit from the left sensor. The top muon seems to generate an energetic secondary particle, probably a ˜MeV electron. By chance, a vertically incident cosmic ray muon has been recorded as well during the exposure time.

**Applications of intelligent detectors I / 20**

# Guessing the geometric features of a particle trajectory in a magnetic field by measuring one point and its tangent.

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The talk reviews the geometric basis of the "PT" and "CW" approaches for the selection of high transverse momentum particles coming from primary interactions at sLHC. Starting from the definition of a small segment measurement (stub) of a particle trajectory it gives basic general constraints which contour the architecture of both methods. The sensor position with respect to the production vertex as well as the sensor structure and design are key factors the behavior of which is described by a-dimensional parameters according simple scaling laws. Using these tools the selection efficiency of high transverse momentum is discussed in a thorough way, with emphasis to the effects due to the Lorentz drift, non primary background particles, sensor dimension and position. The discussed predictions, while waiting the LHC collisions validation, can be verified with the cosmic rays data in the CMS Tracker.

**System integration / 21**

# Light prototype support using microchannel technology as high efficiency system for silicon pixel detector cooling .

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The development of microscale mechanical system has been growing rapidly getting the opportunity to satisfy to the request of the semiconductor detectors to have ever more power located on the active region.
Miniaturization associated to microtechnologies allow the design of microsystem structures able to cool silicon pixel detector with specific power of the order of some W/cm2 with less than 0.3% of radiation length .
Using microchannel technology we present design and thermo hydraulic results for low material budget support and cooling obtained through forced liquid convection, developed for Layer-0 of SuperB silicon vertex tracker.
The support prototypes, realized in composite material (CFRP) and with different geometries , has been tested in the thermo-fluid dynamic test bench in the INFN Pisa laboratory.
The experimental results confirm the finite-element analysis studies conducted on computational model .
Moreover, looking forward to cooling systems fully integrated on silicon wafers, some mechanical tooling tests actually in progress and the design of a module prototype are shown .

**Applications of intelligent detectors I / 22**

# Triggering performance of stacked pixel layers for the SLHC CMS tracker

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We present simulation results for a concept detector designed to provide tracking information to the CMS Level-1 trigger in a new silicon tracker for SLHC. A layer comprising pairs of closely separated pixel sensors (˜1mm spacing, ˜100 um x >2.5 mm strixels) could be used to reduce the on-detector data rate by selection of hits from high transverse momentum tracks. The geometry has been modeled within GEANT for an accurate description of material effects. The performance of one of these triggering layers has been measured from simulations for a range of sensor configurations. We present that a single layer would be capable of reducing the detector data rate by a factor of ~20 while maintaining efficiencies in excess of 95% for tracks with pT>2GeV/c while information from two or more triggering layers could be used to further reduce the amount of tracking information provided to the Level-1 trigger.

**Applications of intelligent detectors I / 23**

## Intelligent Trackers as L1 Trigger providers for the SLHC

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At the SLHC, the present Trigger strategies based on energy deposits in the Calorimeters, and tracks in the outer Muon Detectors, will have to be augmented with information from the Inner Tracking Detectors, to confirm the presence of the corresponding high Pt tracks, and to establish their isolation.

We discuss possible layouts and architectures for the CMS Tracker upgrade at the SLHC, based on "Stacked Modules"and their ability to determine the Pt of charged tracks with a local measurement and to discriminate accordingly, and review the present status of simulation studies of their performance potential both in terms of track reconstruction as well as L1 Trigger providers for the SLHC.

**Electronic circuits (3D and conventional) / 24**

## Application of Vertically Integrated Electronics to Intelligent Trackers

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At Super-LHC luminosity it is expected that the standard suite of L1 triggers for CMS will saturate. Information from the tracker will be needed to reduce trigger rates to satisfy the L1 bandwidth. Tracking trigger modules which correlate information from closely-spaced sensor layers to form an on-detector momentum filter are being developed by several groups. We report on a trigger module design which utilizes three dimensional IC technology to incorporate chips which are connected both to the top and bottom sensor, providing the ability to filter information locally. A demonstration chip, the VICTR, has been submitted to the Chartered/Tezzaron two-tier 3D run coordinated by Fermilab. We report on the 3D design concept, the status of the VICTR chip and associated sensor integration utilizing oxide bonding.

**High speed communication / 25**

# Ultra low power consumption 10.7 Gb/s transmission over 2 km single mode fiber optics link

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In this work we demonstrate a digital error-free transmission (BER < 1e-12) at a bit rate of 10.7 Gb/s over a 2 km optical-link obtained with an ultra-low-voltage lithium niobate Mach-Zehnder modulator (LNM) driven by 0.6 Vpp and with 1 mW of optical input power at a wavelength of 1550 nm. Voltages in this range allow driving the modulator directly from the board and placing the optical active part of the link (e.g. signal lasers) outside the critical radiation area. This implies a strong reduction of components'number and power requirement in the "hot"zone. In such a scenario, lasers are some hundred meters away from the modulators and polarization issues along the laser-modulator connecting fibre link play a significant role, in particular if deployment of polarization maintaining fibres has to be avoided to reduce the system cost. We will present proposals and results aimed at employing single mode fibers (SMF) throughout the link (laser-modulator-detector) without increasing penalties due to polarization dependency. We also address the integration of the overall link presenting a low cost solution for laser-modulator subsystem.

**System integration / 26**

# The design of stable, low-mass support and cooling structures

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Designs of stable, low-mass support and cooling structures for intelligent trackers should take into account the additional power dissipation associated with local trigger generation, high speed communications, and power delivery, as well as the spatial distributions of heat sources. For many applications, a modular design can alleviate cooling and support issues and allow parallel fabrication at multiple locations. A proposed design for CMS phase 2 upgrade track trigger formation will be used to illustrate the extent to which design requirements are specific to intelligent tracking, ways in which those design requirements might be met, and implications for local tracker geometry, material selection, structural stability, and the material budget.

**Electronic circuits (3D and conventional) / 27**

# Fast Readout Logic Interfacing a 256-Pixel Matrix of a Dual-Layer 3D Device

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A fast readout architecture with sparsification capabilities for a 256-pixel 3D ASIC was recently proposed by the Italian VIPIX Collaboration and submitted to the CMOS Chartered 130 nm technology. In particular, the readout logic exploits one of the two layers of a 3D device. The readout logic allows sweeping the matrix within 1us and can face an input hit-rate of 100MHz/cm2. The architecture has been deeply investigated in terms of efficiency and sparsification capabilities and a parameterized Register-Transfer-Logic VHDL code has been designed. The paper presents the readout efficiency versus a variety of parameters as the clock rate, the pixel hit-rate and the time-stamp resolution. In addition, the study shows how the readout layer might be adapted to future larger matrices of pixels. A fast readout might also match a data-driven tracking system. The overall project leads to design a high-density thin vertex detector with an on-chip sparsified digital readout system, for particle tracking, aimed at matching the requirements of future high-energy physics experiments.

Applications of intelligent detectors II / 29

# I-ImaS: Intelligent Imaging Sensor - application to intelligent X-ray imaging

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Conventional x-radiography uniformly irradiates the relevant region of the patient. Across that region, however, there is likely to be significant variation in both the thickness and composition of the tissues present, which means that the x-ray exposure conditions selected, and consequently the image quality achieved, are a compromise. The I-ImaS concept eliminates this compromise by intelligently scanning the patient to identify the important diagnostic features, which are then used to adaptively control the x-ray exposure conditions at each point in the patient. In this way optimal image quality is achieved throughout the region of interest whilst maintaining or reducing the dose. An I-ImaS system has been built under an EU Framework 6 project and has undergone pre-clinical testing. The system is based upon two rows of sensors controlled via an FPGA based DAQ board. Each row consists of a 160 mm x 1mm linear array of ten scintillator coated 3T CMOS APS devices with 32 μm pixels and a readable array of 520 x 40 pixels. The first sensor row scans the patient using a fraction of the total radiation dose to produce a preview image, which is then interrogated to identify the optimal exposure conditions at each point in the image. A signal is then sent to control a beam filter mechanism to appropriately moderate x-ray beam intensity at the patient as the second row of sensors follows behind.
Tests performed on breast tissue sections found that the contrast-to-noise ratio in over 70% of the images was increased by an average of 15% at an average dose reduction of 9%.
The same technology is currently also being applied to baggage scanning for airport security.

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# Architecture of a Level 1 Track Trigger for the CMS Experiment

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The luminosity goal for the Super-LHC is 10ˆ35/cmˆ2/s. At this luminosity the number of proton-proton interactions in each beam crossing will be in the hundreds. This will stress many components of the CMS detector. One system that has to be upgraded is the trigger system. To keep the rate at which the level 1 trigger fires manageable, information from the tracker has to be integrated into the level 1 trigger. Current design proposals foresee tracking detectors that perform on-detector filtering to reject hits from low-momentum particles. In order to build a trigger system, the filtered hit data from different layers and sectors of the tracker will have to be transmitted off the detector and brought together in a logic processor that generates trigger tracks within the time window allowed by the level 1 trigger latency. I will describe a possible architecture for the off-detector logic that accomplishes this goal.

Applications of intelligent detectors II / 32

# Pixel Imaging Mass Spectrometry with fast pixel detectors

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We report on 'proof of concept' experiments in Pixel Imaging Mass Spectrometry (PImMS) using an ultra-fast frame-transfer CCD camera and also describe an intelligent CMOS sensor which is being developed for this application by the PImMS collaboration in the UK. PImMS is a combination of a traditional TOF mass spectrometry and of the ion imaging. Information provided by the ion imaging gives access to valuable structural information of the molecule under investigation, in addition to the normal mass spectrum. Recording of the 2D spatial information of the arriving ions allows to reconstruct the ion velocity distributions for separate ion masses and to correlate them to each other. The new PImMS sensor will be capable to time stamp up to four arriving ions per pixel during the 200 microsec acquisition cycle with 50 nsec resolution which should meet the demanding requirements for complete recording of mass spectra of complex organic molecules.

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# Data Compression and LVL1 track triggering by means of Digital Signal Processing in GridPix/Gossip FE pixel chips

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The GridPix detector is a gaseous Time Projection Chamber with an active pixel chip as readout plane. See ATLAS Note: ATL-UPGRADE-SLIDE-2009-141; ATL-COM UPGRADE-2009-005.- Geneva : CERN, 2009 for detailed information.

Thanks to its fine granularity, the individual electrons along a particle track, are registered in three dimensions. Each GridPix layer measures therefore a track segment. The Gossip detector is a GridPix with a drift gap of only 1 mm. Here, the gas layer replaces a Si sensor layer of Si pixel or strip detectors. One of the advantages of Gossip/GridPix with respect to Si pixel or strip detectors is the extreme low source capacitance at the (pixel) preamp input pads. This limits the requirements

concerning power, and physical space, needed for the preamp in the pixel. As a consequence, space is available for data processing.

With a drift gap of 20 mm, and placed in a specific angle of rotation, the projected tracks, appearing on the pixel plane, have a specific length for infinite high momentum tracks. Deviations from this length are a measure for the track momentum and for the charge sign of the particle's track. The projected track length is therefore a criterion for a LV1 trigger. In the pixel chip, an algorithm of neighbour-pixel-active could operate, in parallel to all pixels. The projected track could be fitted within ˜100 ns, and its length could be established well within the trigger latency (the electron drift time of 200 ns included). This principle could also be used to provide a 1 - 20 GeV cut on 'valid' track data, reducing the data rate.

The present Si-strip trackers could be replaced by Gossip strixel detectors with its lower costs as main advantage. With a strixel width of ˜ 50 um and a strixel length of ˜ 5 mm, the strixel surface is for the largest part available for digital signal processing. The raw data can be converted in 2D track position data, and could be communicated to 'common sector' detection layers at smaller and larger radii.

**Applications of intelligent detectors I / 34**

# A First Level Track Trigger for ATLAS at Super-LHC

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The proposed luminosity upgrade of the Large Hadron Collider, the Super-LHC, will tenfold the luminosity to $10^{35}cm^{-2}s^{-1}$ to increase the LHC discovery potential for new heavy particles and to allow for statistics limited precision measurements of possibly discovered particles. Due to the increased luminosity the ATLAS and CMS experiments have to deal with hundreds of events per collision challenging especially the tracking and the trigger capabilities.

To maintain the output rate of the first trigger level both collaborations consider to integrate a new track trigger operating already at the first trigger level. The track triggers will exploit information from the pixel and silicon strip detectors and provide track candidates. The tracks can then be combined with information from the calorimeters and the muon detectors to form a L1 decision.

The timing requirements of the first trigger levels put severe constraints on the frontend and trigger electronics. A well established reconstruction technique is the fast hardware lookup for identifying track patterns. We will discuss possible lookup implementations using Content Addressable Memories, which provide pattern recognition matches with large memory space at high frequency. We report estimates on the number of track patterns based on the upgraded ATLAS detector design, depending on the number of used layers and the minimum transverse momentum of tracks.

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# Track finding with radially pointing scintillating fibers

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A detector layout using O(cm) long, radially pointing, scintillating fibers at large radius, is investigated. Such a geometry allows discrimination between high and low pT particles based on their angle of incidence and because high pT particles deposit large ionization in one or two fibers, while low pT particles deposit small ionization in many fibers. A pixelated array of these fibers provides a phi-z projection of particle trajectories, from which the track parameters can be calculated. The simulated track parameter resolutions will be presented, and some of the unique detector and electronics issues associated with such a design will be discussed.

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# Present and future inter pixel communication architectures in Timepix/Medipix derived read out chips

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The Medipix3 read out chip (ROC) demonstrates the successful use of inter-pixel communication to reconstruct spectroscopic information from X-ray hits in a segmented sensor mitigating the effects of charge sharing. Building on this work and the success of the current Timepix chip, conceptual designs for the matrix architecture of the Timepix2 and VELOpix ROCs are presented. These chips will use distributed analogue and digital architectures to increase the functionality available to each pixel and to perform significant on-chip data compression. Timepix2 will combine a measurement of the charge deposited in each pixel with a sub-2ns timestamp resolution and pipeline-trigger readout requiring significant on-pixel digital circuitry. The VELOpix chip being proposed for the LHCb VELO upgrade will utilise local pixel hit clustering and on-chip data compression to allow triggerless event readout at a sustained bunch crossing rate of 40MHz.

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# Proceedings and Adjourn