

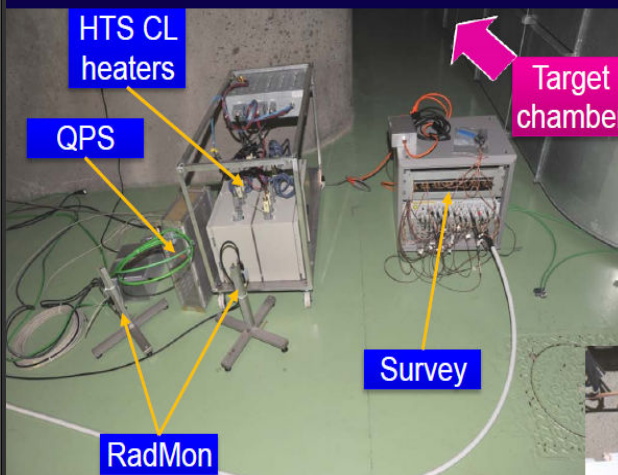
- **SITUATION DANS LE TUNNEL**
- **LES POINTS TESTÉS**
 - **Courants consommés.**
 - **Tensions d'alimentations.**
 - **Conditionneurs.**
 - **Acquisitions par le FIP (LHC)**
- **DESCRIPTION DES TESTS**
- **RÉSULTATS**
- **QUESTIONS ?**

Mesures
Analogiques

INTRODUCTION



2 Test areas – High & Low flux and dose rate with multiple calibrated locations



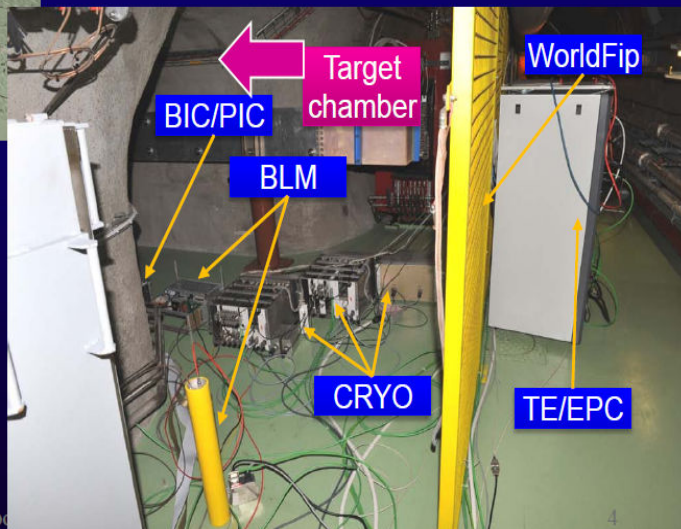
Hottest test area in TSG46:
~ 1.5 Gy(SiO₂)/week
~ 2.6 10¹⁰(1MeV n eq.)cm⁻²/week

New FLUKA simulations are now available thanks to K.Roed

TSG46 :
17 sept au 7 oct

TSG45 :
7 oct au XX nov

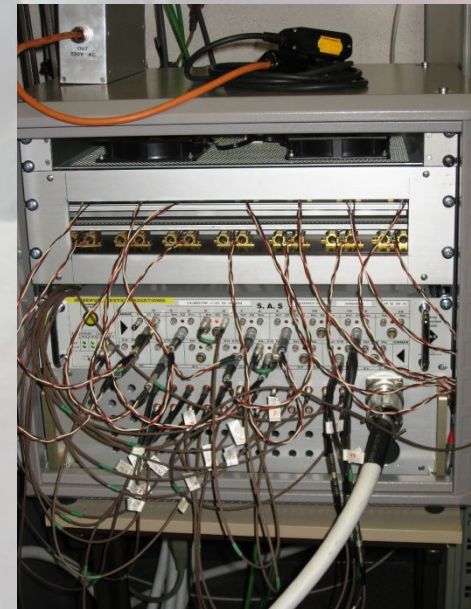
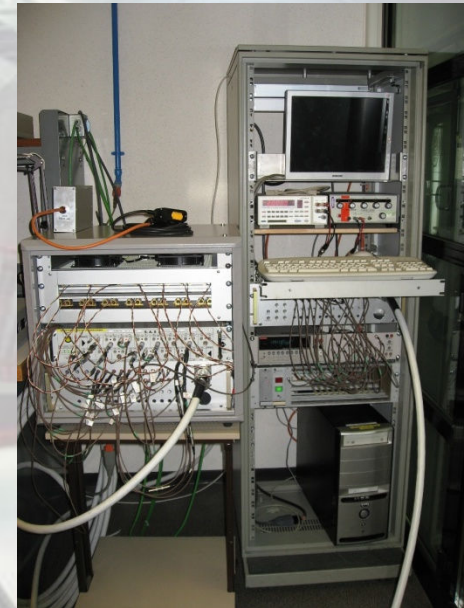
Hottest test area in TSG45 :
~ 12Gy(SiO₂)/week
~ 2.8 10¹¹(1MeV n eq.)cm⁻²/week
Most users in this area



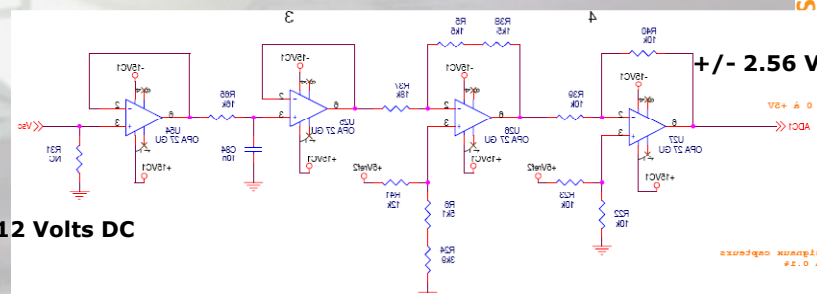
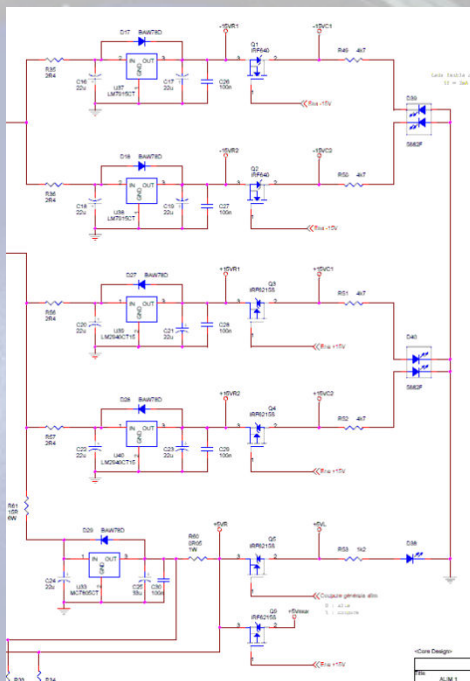
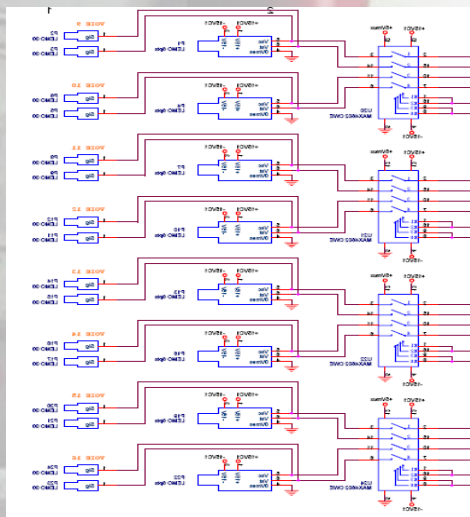
SITUATION



- **CONSOMATION DES ALIMENTATIONS**
- **COMPORTEMENT DES CONDITIONNEURS**
- **SWITCHES MOS + MAXIM**
- **CARTE ADUC834 + FIP**
 - **SYNCHRONISATION**
 - Programmes de logging et PC
 - **CYCLES DE 5 MINUTES**
 - 2 min de logging standard
 - 1 min de coupure alim.
 - 1 min pour 1^{er} conditionneur
 - 1 min pour 2^{ème} conditionneur
 - **RESETS POSSIBLE**
 - Général 230 V (relais).
 - Fip → remote reset via un message → 5V carte ADUC.
 - Watchdog Chip ADUC 834 → 5V carte ADUC.
 - I 500mA du SAS → 5V carte ADUC.



POINTS TESTÉS CHÂSSIS SAS



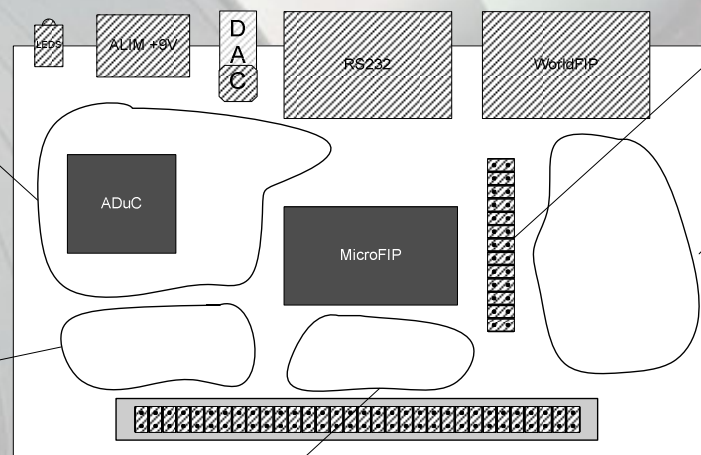
+/- 12 Volts DC

+/- 2.56 Volts DC

Régulation
Supervision

Reset FIP

Décodage
d'adresse



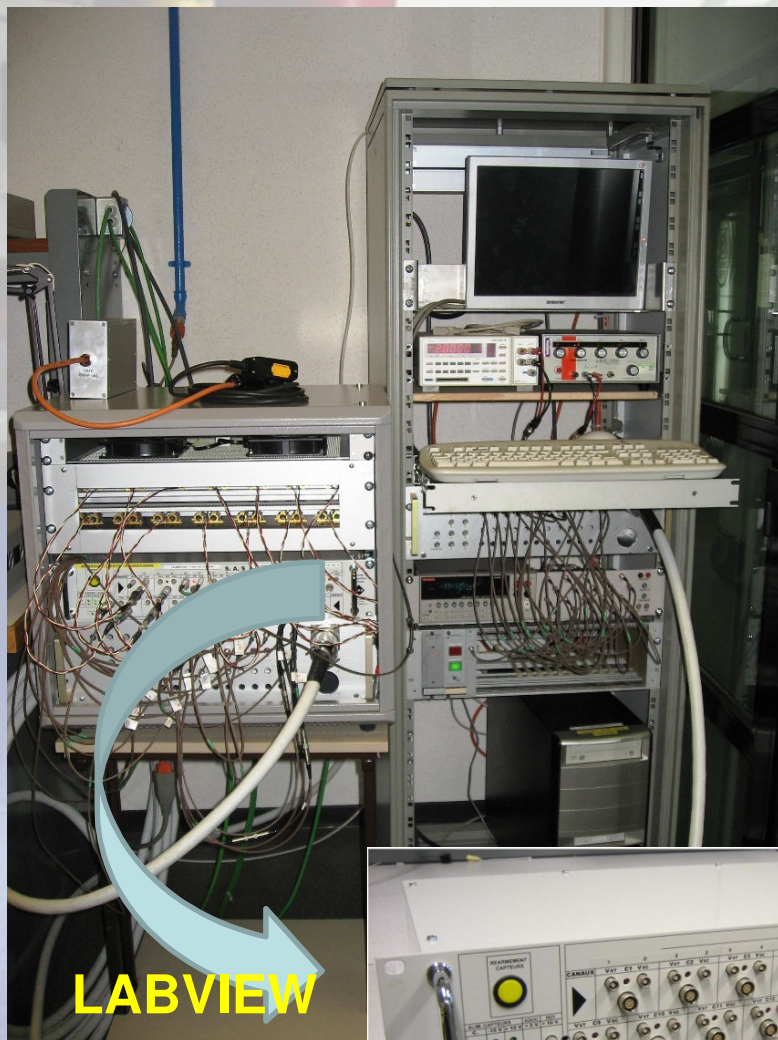
Config.
MicroFIP
+ PA/PB

Outils de
ligne FIP

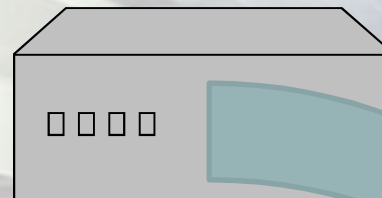


35 conv. of 20 bit in 1 sec.

COMMENT



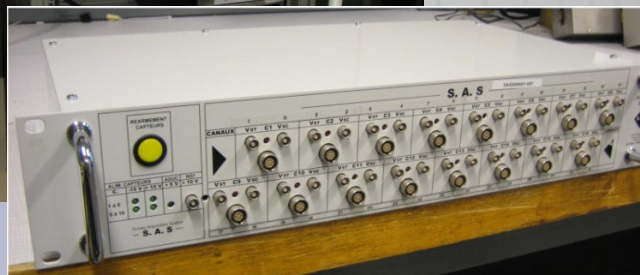
LABVIEW

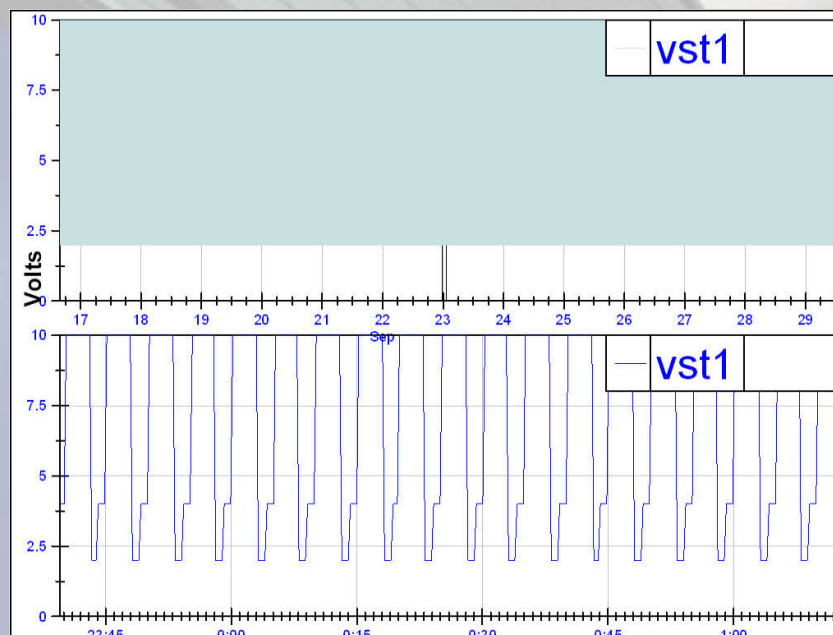
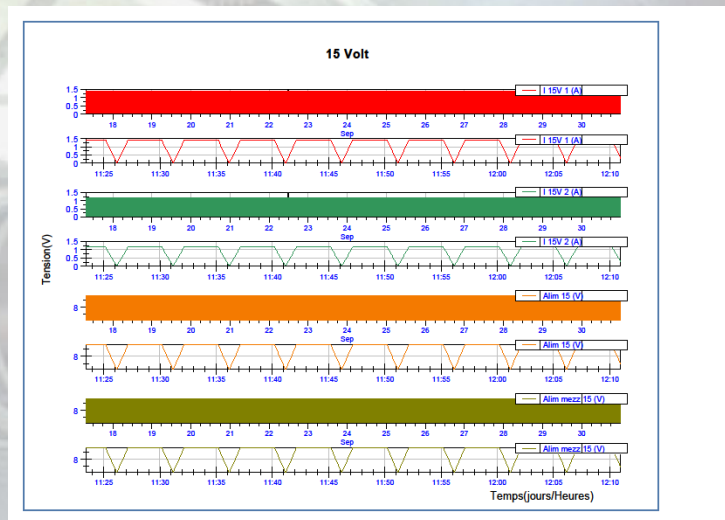
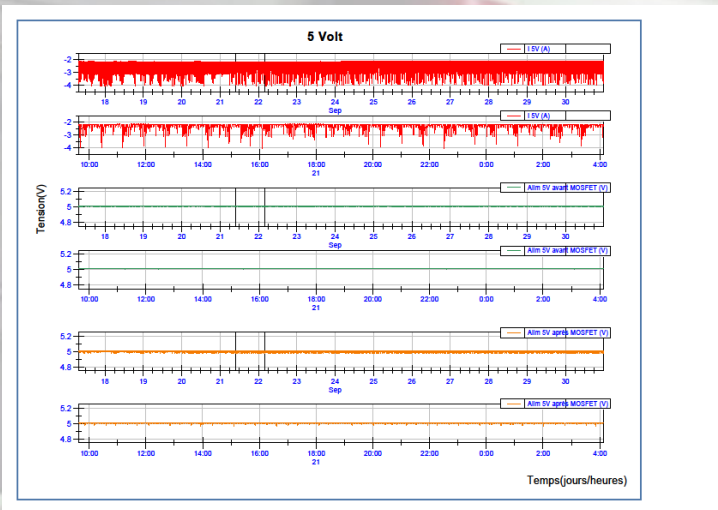


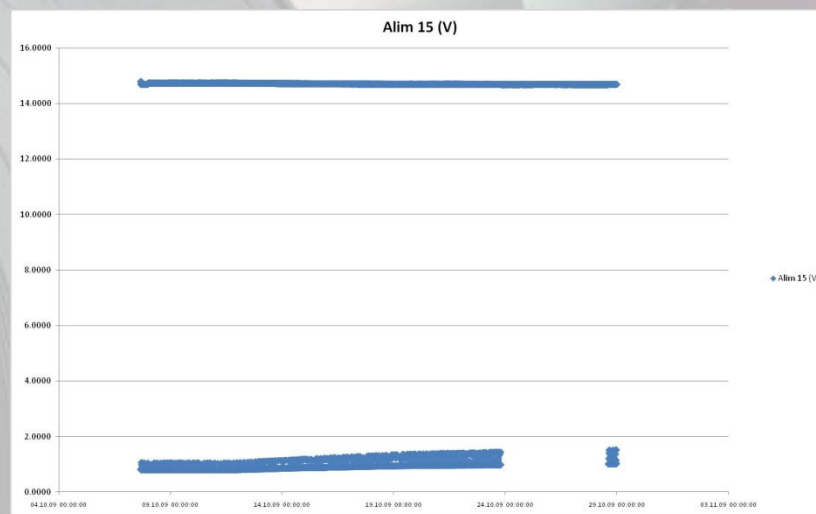
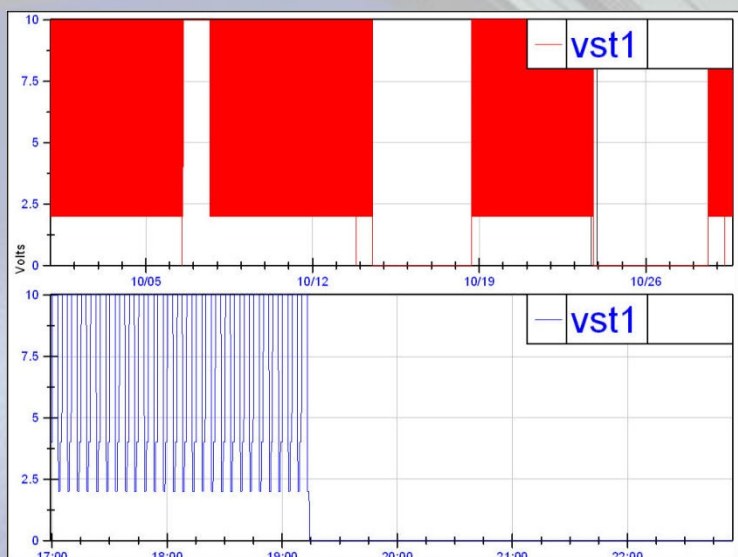
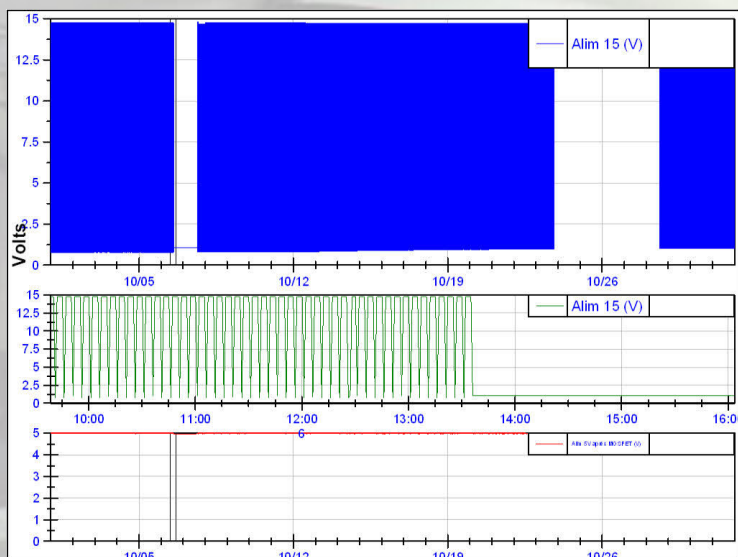
FIP LHC

J.Palluel
BE/CO

A.Marin
BE/ABP/SU

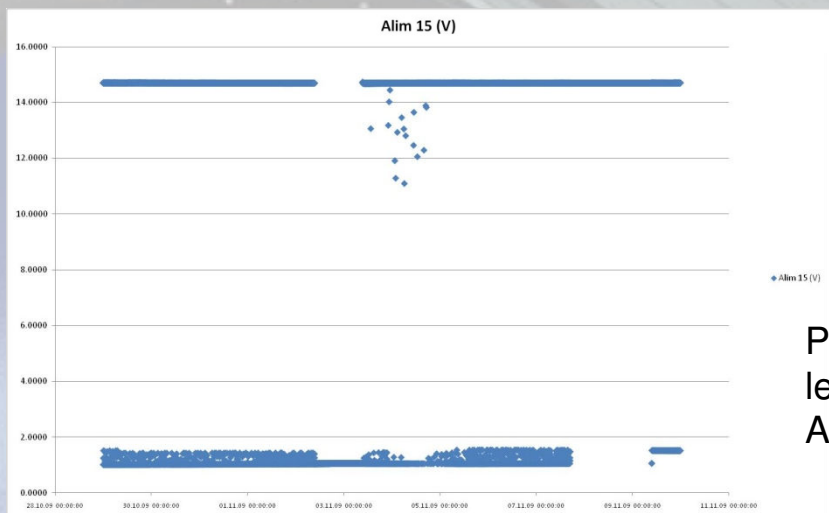
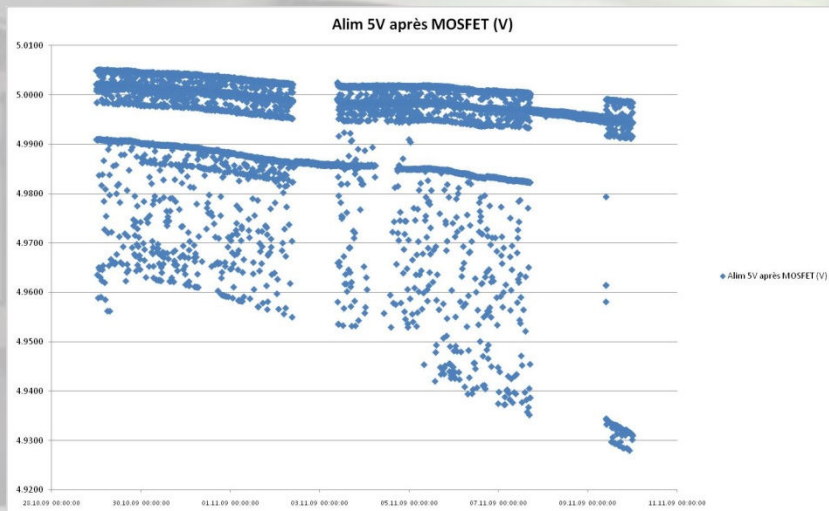






Changement de TJ45 à TJ46 le 7 octobre 2009.
 Pannes FIP le 14 et le 23 avec redémarrage le 19
 et le 28 avec un reset FIP à distance par BE/CO

OCTOBRE



Pannes FIP le 2, le 4, le 7 avec redémarrage le 3, le 5, le 9 avec un reset FIP à distance par BE/CO. Arrêt total le 9 novembre

NOVEMBRE

Successfully tested COTS in TCC2 from 1999 to 2003
COMPOSANTS DU SAS

COMPOSANTS CHÂSSIS SAS

- Amplifiers
 - **INA105, INA141, OPA27**, AD210BN
- Comparators
 - **LM311**
- Timer
 - NE555
- Voltage regulators
 - **MC7815, MC7915**
- Voltage references
 - **REF102**, LT1236A-10
- Digital isolators
 - ISO150

- Thyristors
 - SKT80/18E
- Isolated DC-DC converters
 - TH10522, TH10511, TMA0505S, TMA0515D
- Micro-converters
 - ADuC812, ADuC831, **ADuC834**

- Switches
 - **MAX4602**
 - **IRF640, IRF 6215s**
- logique
 - **Série 74HCTxxx**

- ADuC812 (4000 devices in QPS electronics)
 - 8 channel 12 Bit ADC + 8051 compatible core + 8k Flash EEPROM
 - ADuC831 (2700 devices in QPS electronics)
 - As ADuC831 but 62k Flash EEPROM
- **ADuC834 (7600 devices in QPS electronics)**
 - **24 Bit ADC + 8051 compatible core + 62k Flash EEPROM**
- **Functional test of the chip**
 - **Communication during the test via serial port**
- Memory access tests
 - ADuC812: external SRAM
 - **ADuC831 & ADuC834: internal & external SRAM, internal Flash EEPROM**
- Error correction algorithm
 - Bitwise triple voting for data stored in external SRAM validated