

Enhancement Presentation

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Enhancement Presentation

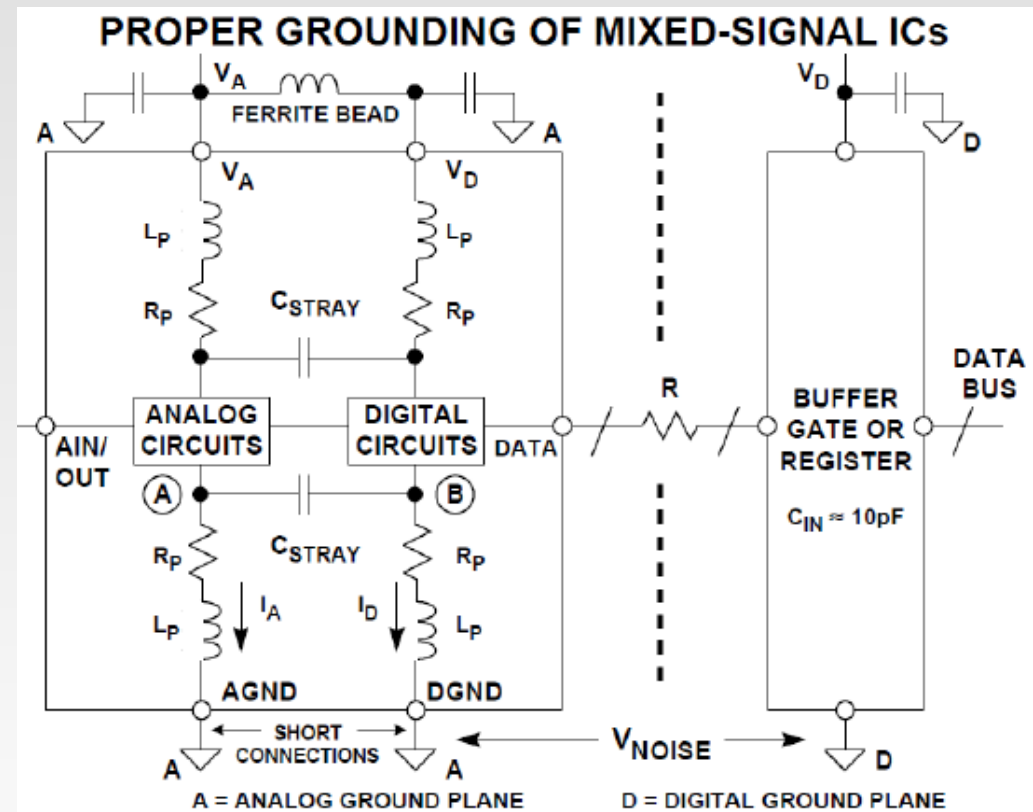
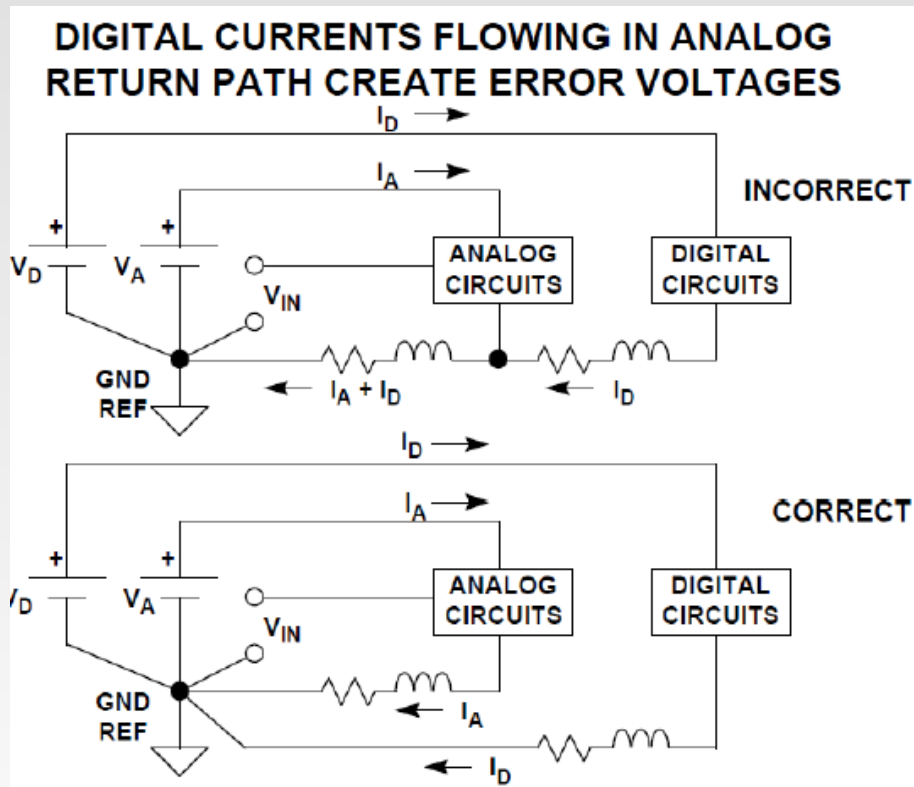
- Summary
 - The analogical mezzanine prototype
 - Ideas
 - Schematics
 - Physical dimensions
 - Connectors
 - Discrete OP Amp simulations
 - Previous problems
 - Calculations
 - Results

• The analogical mezzanine prototype

- Ideas to discuss
 - About noise and grounding
 - Different strategies with grounding
 - About connectivity
 - Flexibility to test any analog architecture
 - About delay evaluation
 - Flexibility to evaluate all possible delay scenarios

• The analogical mezzanine prototype

■ Noise and grounding



• The analogical mezzanine prototype

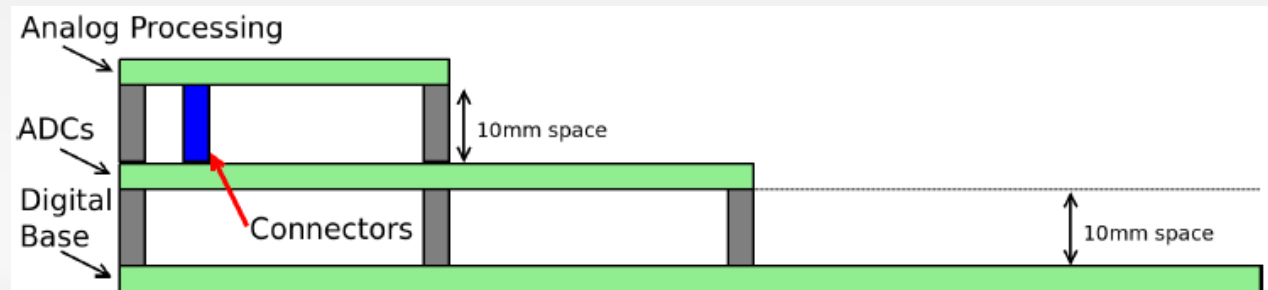
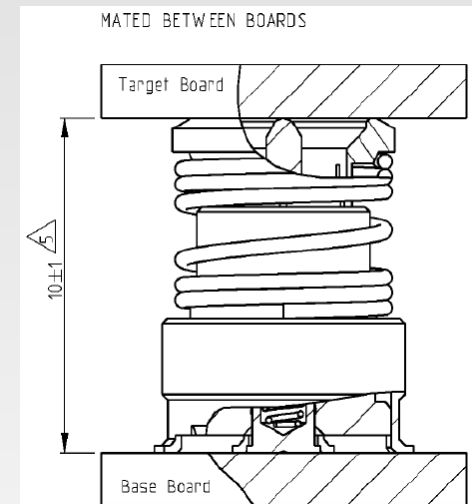
- Connectivity
 - Flexibility to test any analogical architecture

Tyco 619134-1

Char. Imp. 50 Ohms
Freq. Range Up to 6 GHz
Return Loss -20dB min.
Shield Effect. -60 dB min.
Resistance $< 70\text{ mOhm}$

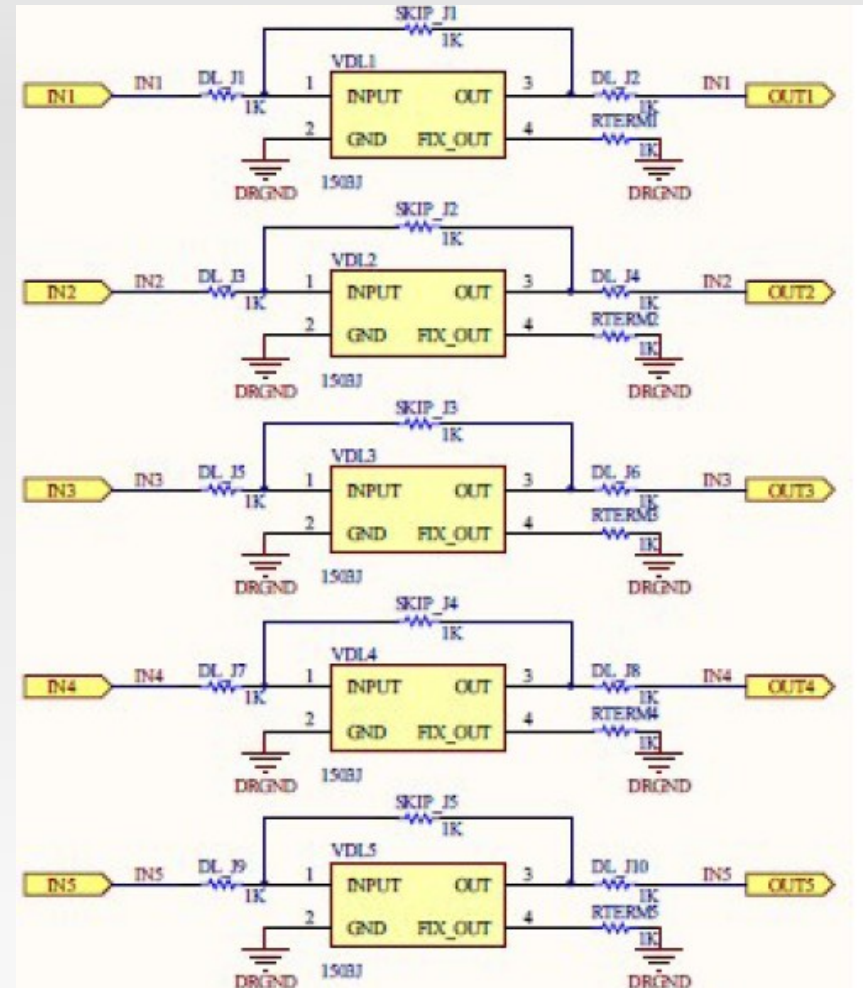
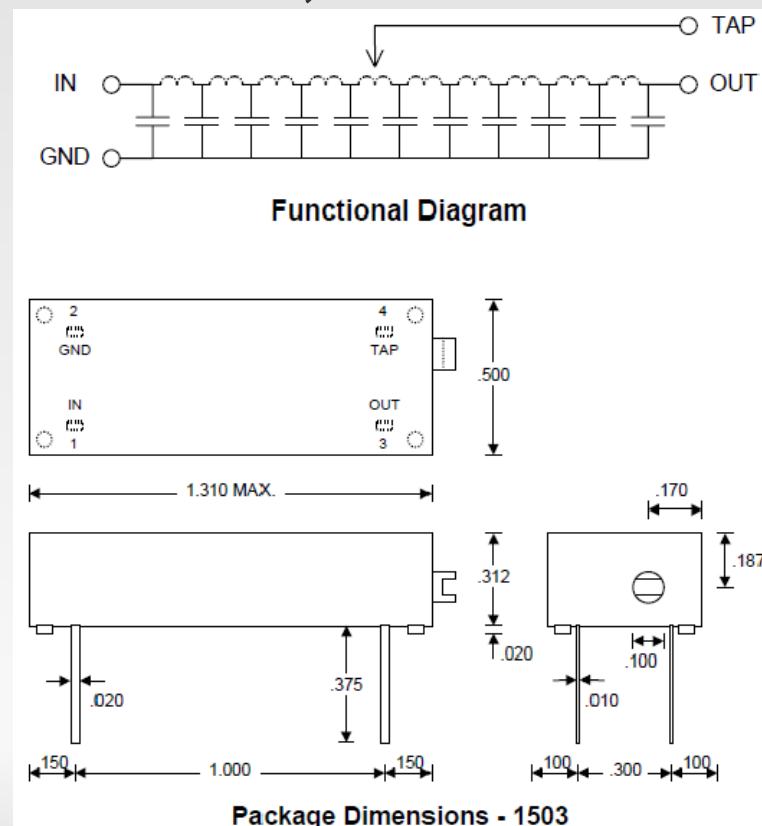
Ratings

- Voltage: 125 volts AC
- DC Current: 4.8 A max.



• The analogical mezzanine prototype

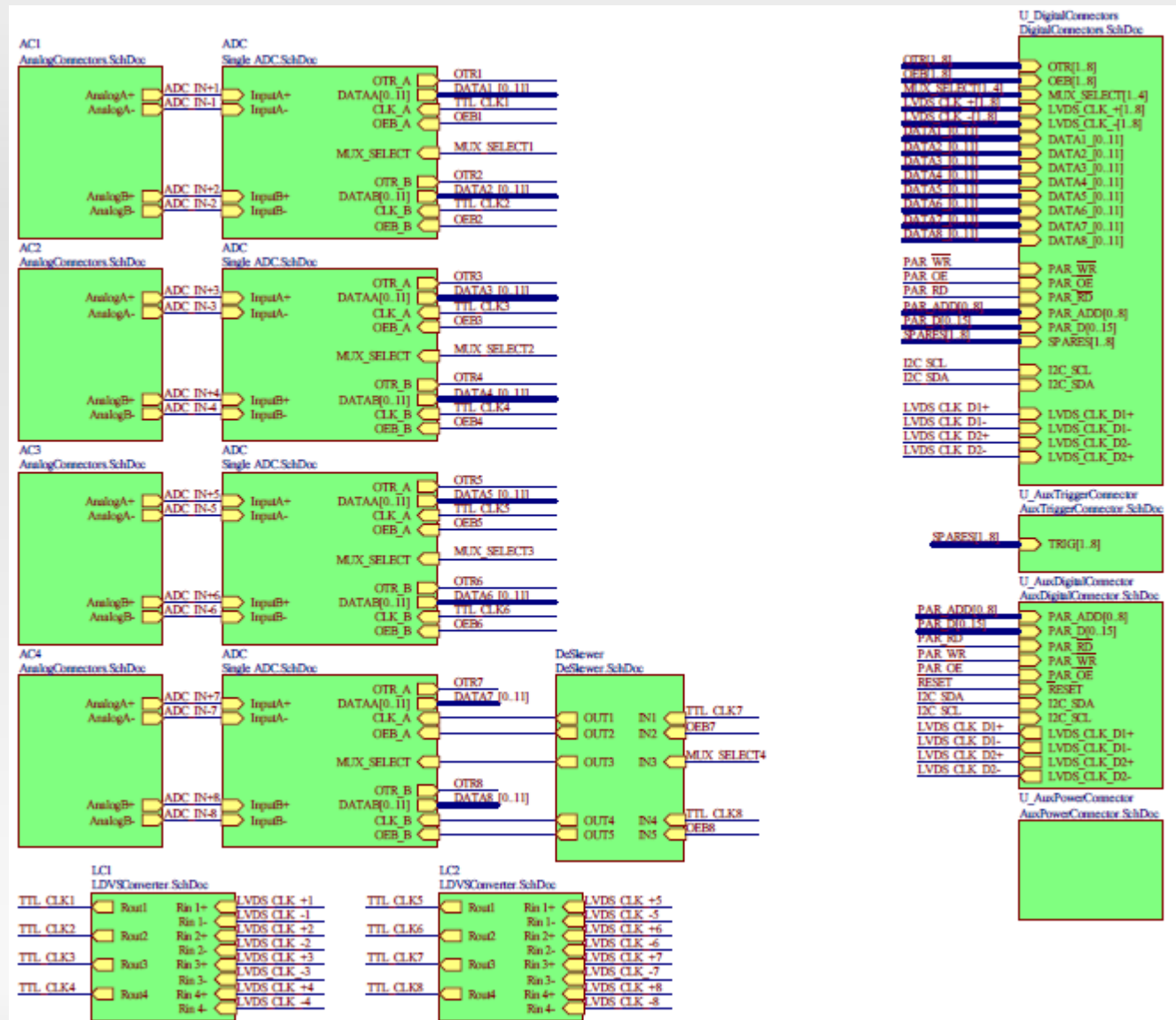
- Delay evaluation
- 2xClock, 2x Output Enable, Mux Select



The analogical mezzanine prototype

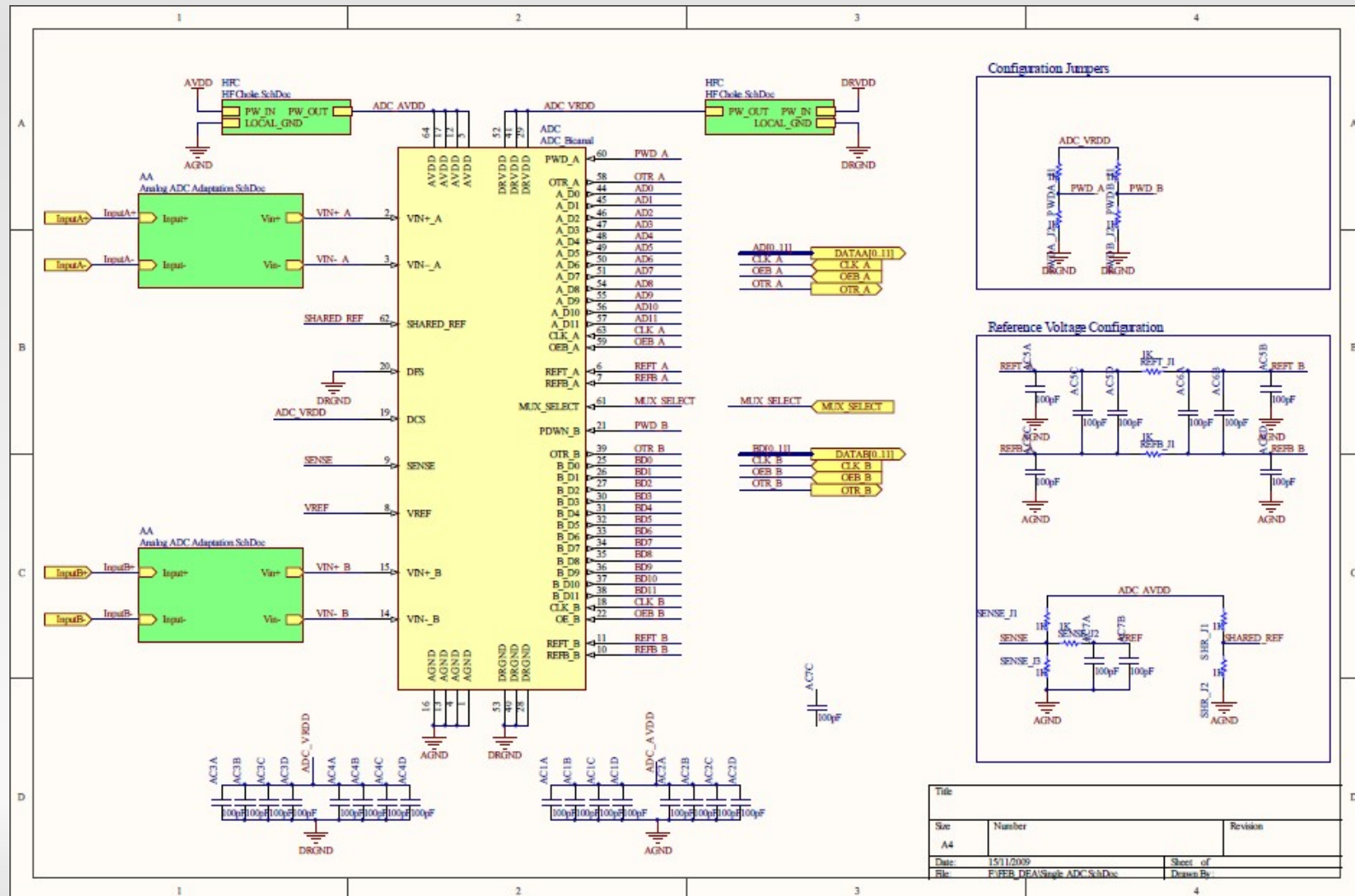
■ Schematics

- 4 Instances of 2 channels each
- 1 With Delay Control
- Clock Conversion to single ended
- Digital Connector
- Analogical Connector
- Auxiliary Connectors



The analogical mezzanine prototype

■ Schematics: ADC



■ Schematics: Connector



• The analogical mezzanine prototype

■ Schematics: Right Connector

1	71	DRGND	71	DRGND
2	72	LVDS_CLK_+6	72	LVDS_CLK_-1
3	73	LVDS_CLK_-6	73	LVDS_CLK_+1
4	74	DRGND	74	DRGND
5	75	LVDS_CLK_-7	75	LVDS_CLK_+2
6	76	LVDS_CLK_+7	76	LVDS_CLK_-2
7	77	DRGND	77	DRGND
8	78	LVDS_CLK_+8	78	LVDS_CLK_-3
9	79	LVDS_CLK_-8	79	LVDS_CLK_+3
10	80	DRGND	80	DRGND
11	81	LVDS_CLK_D1-11	81	LVDS_CLK_+4
12	82	LVDS_CLK_D1+12	82	LVDS_CLK_-4
13	83	DRGND	83	DRGND
14	84	LVDS_CLK_D2+14	84	LVDS_CLK_-5
15	85	LVDS_CLK_D2-15	85	LVDS_CLK_+5
16	86	DRGND	86	DRGND
17	87	MUX_SELECT3	87	MUX_SELECT1
18	88	OEB5	88	OEB1
19	89	DATA5_11	89	DATA1_11
20	90	DATA5_10	90	DATA1_10
21	91	DATA5_9	91	DATA1_9
22	92	DATA5_8	92	DATA1_8
23	93	DATA5_7	93	DATA1_7
24	94	DATA5_6	94	DATA1_6
25	95	DATA5_5	95	DATA1_5
26	96	DATA5_4	96	DATA1_4
27	97	DATA5_3	97	DATA1_3
28	98	DATA5_2	98	DATA1_2
29	99	DATA5_1	99	DATA1_1
30	100	DATA5_0	100	DATA1_0
31	101	DATA6_11	101	DATA2_11
32	102	DATA6_10	102	DATA2_10
33	103	DATA6_9	103	DATA2_9
34	104	DATA6_8	104	DATA2_8
35	105	DATA6_7	105	DATA2_7
36	106	DATA6_6	106	DATA2_6
37	107	DATA6_5	107	DATA2_5
38	108	DATA6_4	108	DATA2_4
39	109	DATA6_3	109	DATA2_3
40	110	DATA6_2	110	DATA2_2
41	111	DATA6_1	111	DATA2_1
42	112	DATA6_0	112	DATA2_0
43	113	OEB6	113	OEB2
44	114	MUX_SELECT4	114	MUX_SELECT2
45	115	OEB7	115	OEB3
46	116	DATA7_11	116	DATA3_11
47	117	DATA7_10	117	DATA3_10
48	118	DATA7_9	118	DATA3_9
49	119	DATA7_8	119	DATA3_8
50	120	DATA7_7	120	DATA3_7
51	121	DATA7_6	121	DATA3_6
52	122	DATA7_5	122	DATA3_5
53	123	DATA7_4	123	DATA3_4
54	124	DATA7_3	124	DATA3_3
55	125	DATA7_2	125	DATA3_2
56	126	DATA7_1	126	DATA3_1
57	127	DATA7_0	127	DATA3_0
58	128	DATA8_11	128	DATA4_11
59	129	DATA8_10	129	DATA4_10
60	130	DATA8_9	130	DATA4_9
61	131	DATA8_8	131	DATA4_8
62	132	DATA8_7	132	DATA4_7
63	133	DATA8_6	133	DATA4_6
64	134	DATA8_5	134	DATA4_5
65	135	DATA8_4	135	DATA4_4
66	136	DATA8_3	136	DATA4_3
67	137	DATA8_2	137	DATA4_2
68	138	DATA8_1	138	DATA4_1
69	139	DATA8_0	139	DATA4_0
70	140	OEB8	140	OEB4

• The analogical mezzanine prototype

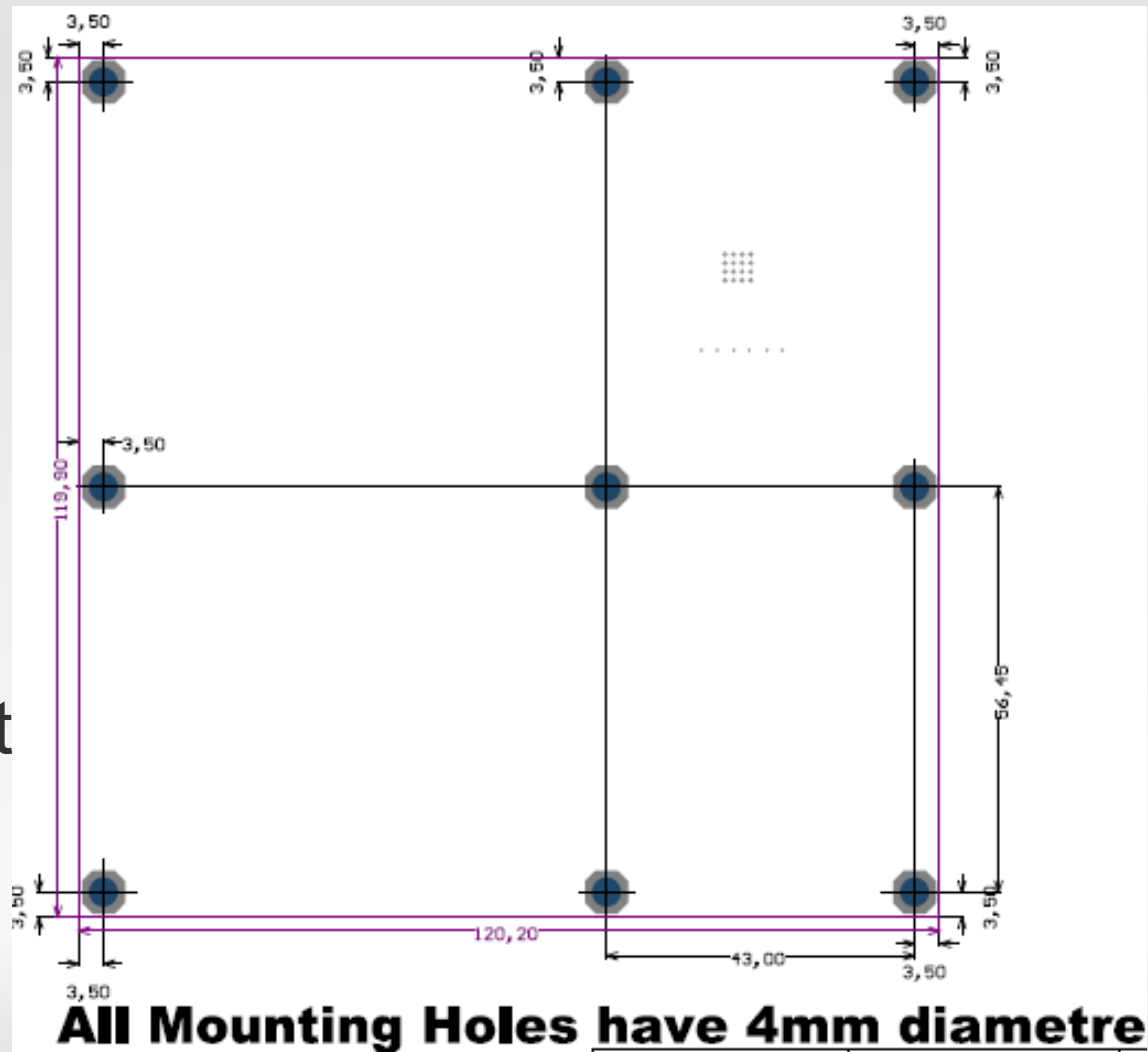
■ Schematics: Left Connector

RESET	1	71	71	DRGND
PAR_OE	2	72	72	DRGND
PAR_RD	3	73	73	DRGND
PAR_WR	4	74	74	DRGND
PAR_ADD0	5	75	75	AGND
PAR_ADD1	6	76	76	AGND
PAR_ADD2	7	77	77	AGND
PAR_ADD3	8	78	78	AGND
PAR_ADD4	9	79	79	AGND
PAR_ADD5	10	80	80	AGND
PAR_ADD6	11	81	81	AGND
PAR_ADD7	12	82	82	AGND
PAR_ADD8	13	83	83	AGND
PAR_D0	14	84	84	AGND
PAR_D1	15	85	85	AGND
PAR_D2	16	86	86	AGND
PAR_D3	17	87	87	AGND
PAR_D4	18	88	88	AGND
PAR_D5	19	89	89	AGND
PAR_D6	20	90	90	AGND
PAR_D7	21	91	91	AGND
PAR_D8	22	92	92	AGND
PAR_D9	23	93	93	AGND
PAR_D10	24	94	94	AGND
PAR_D11	25	95	95	AGND
PAR_D12	26	96	96	AGND
PAR_D13	27	97	97	AGND
PAR_D14	28	98	98	AGND
PAR_D15	29	99	99	AGND
DRGND	30	100	100	AGND
I2C_SDA	31	101	101	DRGND
I2C_SCL	32	102	102	DRGND
DRGND	33	103	103	DRGND
DRGND	34	104	104	DRGND
DRGND	35	105	105	DRGND
DRGND	36	106	106	DRGND
SPARE0	37	107	107	DRGND
SPARE1	38	108	108	DRGND
SPARE2	39	109	109	DRGND
SPARE3	40	110	110	DRGND
SPARE4	41	111	111	AVSS
SPARE5	42	112	112	AVSS
SPARE6	43	113	113	AVSS
SPARE7	44	114	114	AVSS
SPARE8	45	115	115	AVSS
DRVCC	46	116	116	AVSS
DRVCC	47	117	117	AVSS
DRVCC	48	118	118	AVSS
DRVCC	49	119	119	AVSS
DRVCC	50	120	120	AVSS
DRVCC	51	121	121	AVSS
DRVCC	52	122	122	AVSS
DRVCC	53	123	123	AVSS
DRVCC	54	124	124	AVDD
DRVCC	55	125	125	AVDD
RESERVED0	56	126	126	AVDD
RESERVED1	57	127	127	AVDD
RESERVED2	58	128	128	AVDD
RESERVED3	59	129	129	AVDD
RESERVED4	60	130	130	AVDD
RESERVED5	61	131	131	AVDD
RESERVED6	62	132	132	AVDD
RESERVED7	63	133	133	AVDD
DRGND	64	134	134	AVDD
DRGND	65	135	135	AVDD
DRGND	66	136	136	DRGND
DRGND	67	137	137	DRGND
DRGND	68	138	138	DRGND
DRGND	69	139	139	DRGND
DRGND	70	140	140	DRGND

• The analogical mezzanine prototype

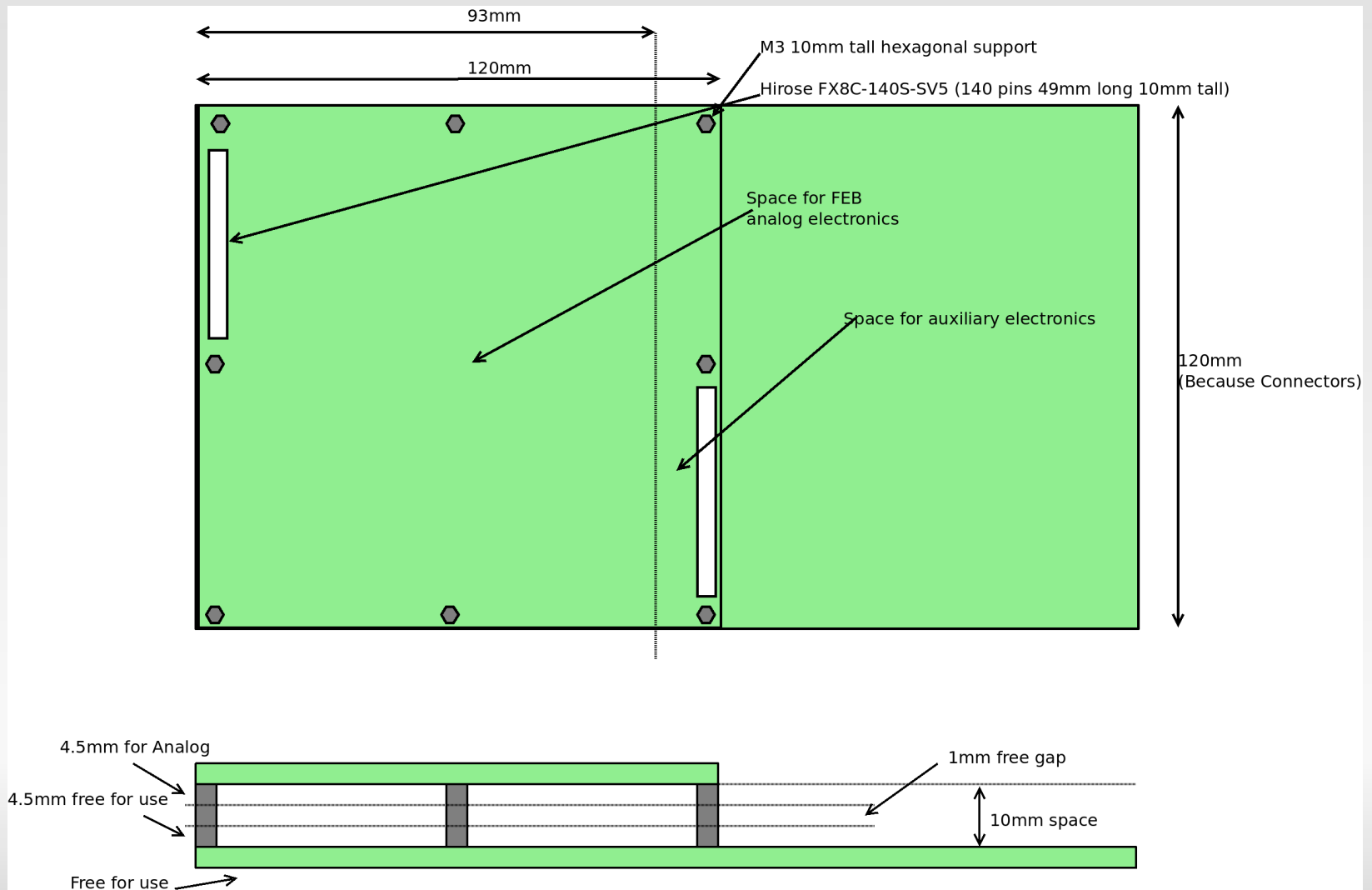
■ Physical Dimensions

- Mounting Holes for their use if needed.
- Digital connectors must be placed, not already agreed on exact position and direction.



• The analogical mezzanine prototype

■ Physical Dimensions



• The analogical mezzanine prototype

- Connectors
 - Hirose FX8C-140S-SV5
 - 10 mm tall
 - 49 mm long
 - 140 pins
- Male and female, not yet agreed on which to use on the digital motherboard and which on the analogical mezzanine.

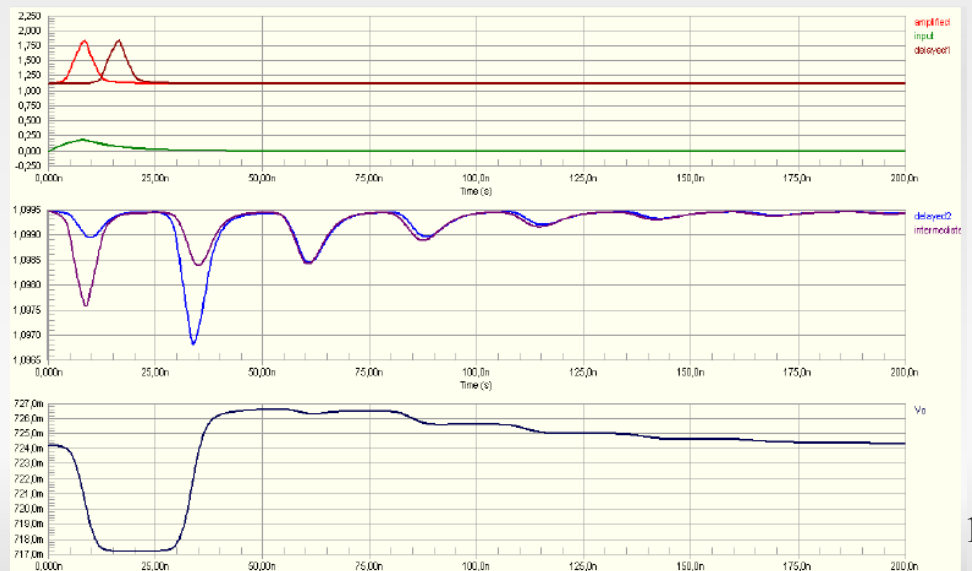
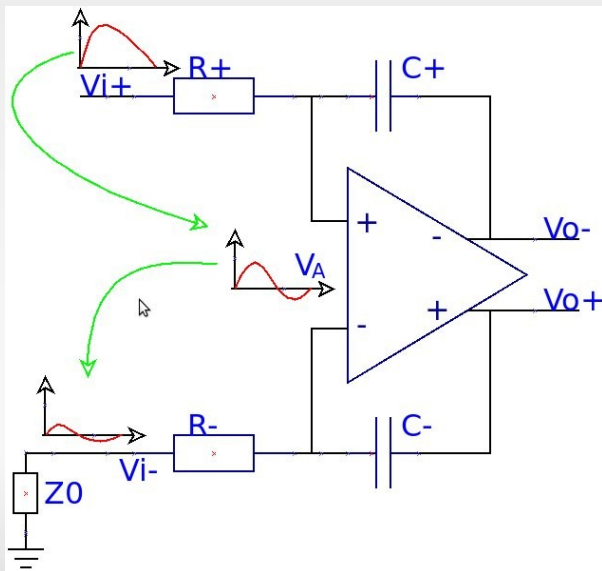
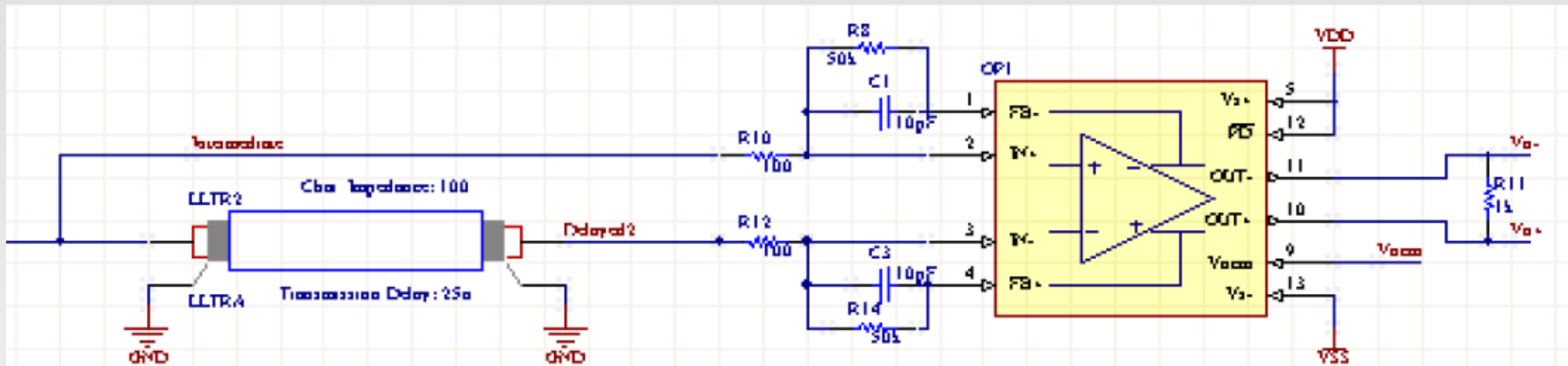


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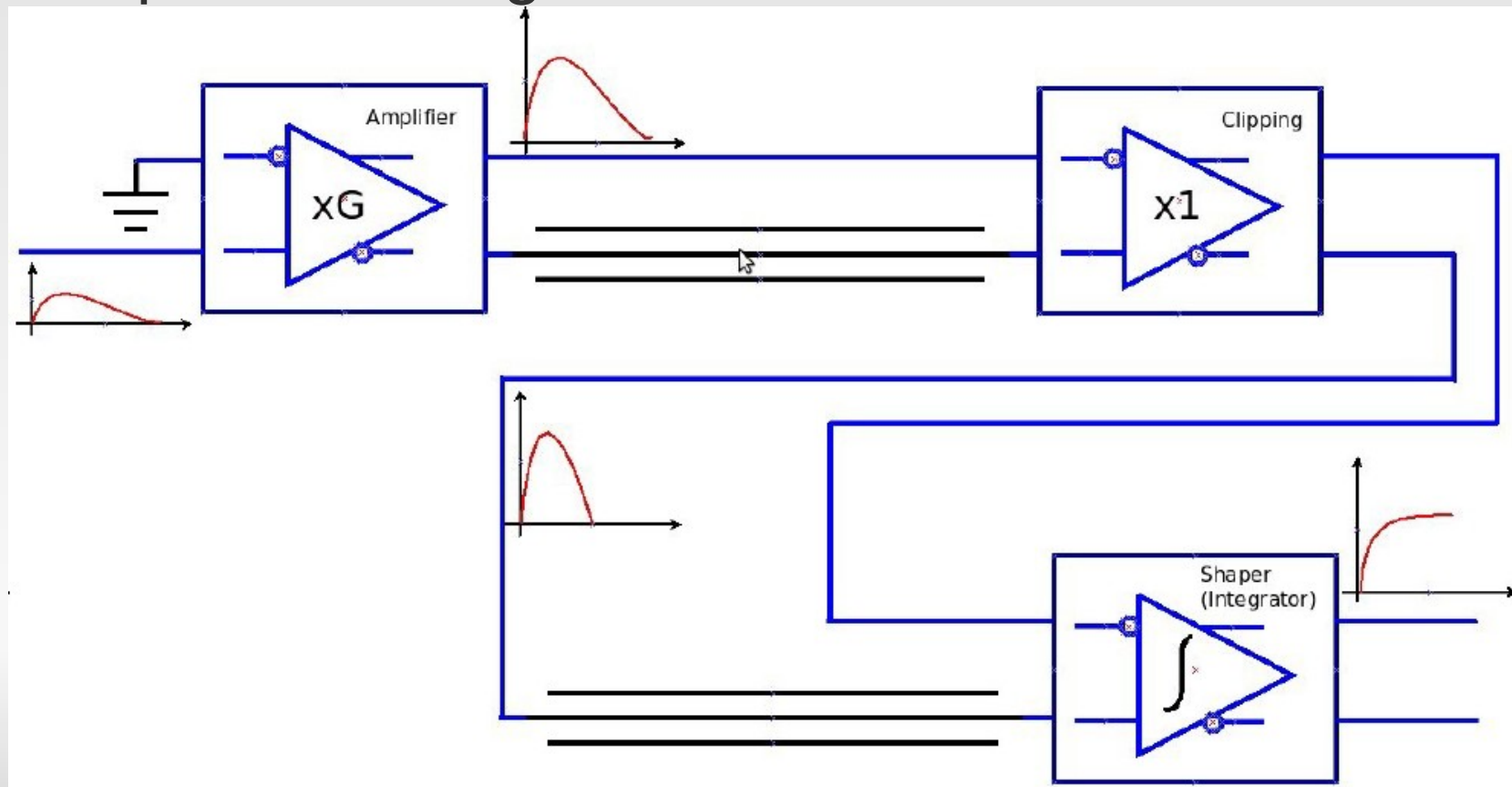
• The analogical mezzanine prototype

■ Discrete Op Amp: Previous Problems



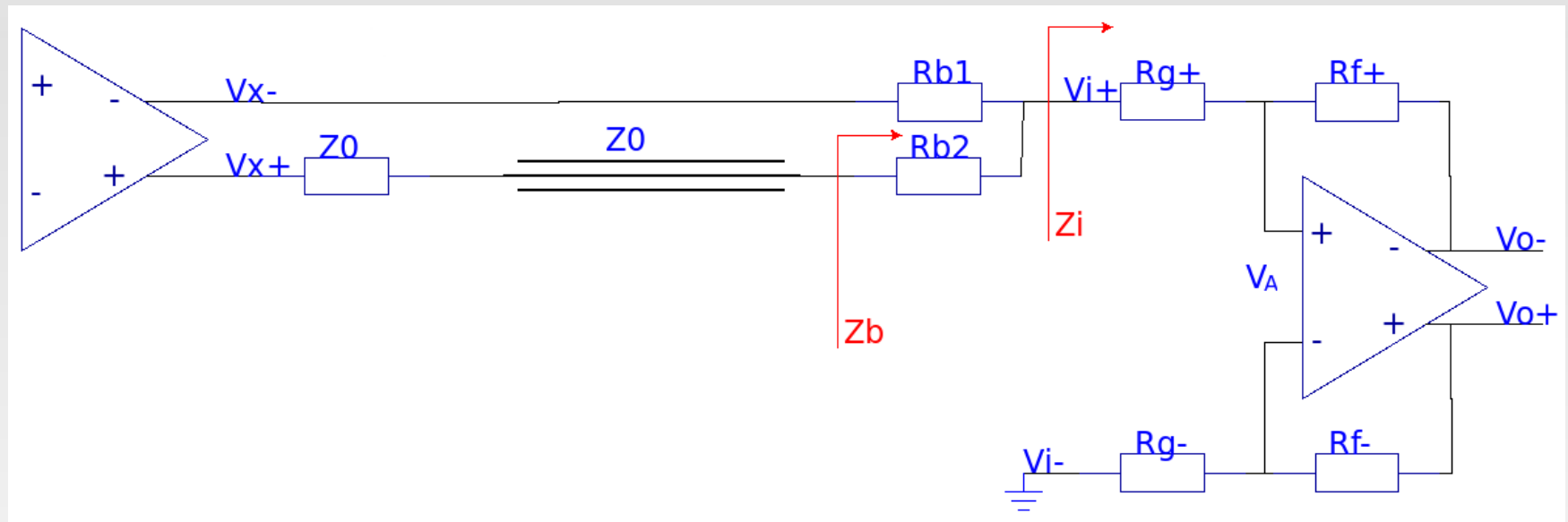
• The analogical mezzanine prototype

- Discrete Op Amp: Previous Problems
 - The previous OP Amp must also be differential in order to cut the feedback. The same happens to the previous stage.



• The analogical mezzanine prototype

■ Discrete Op Amp: Calculations



■ $Z_b = Z_0$; Same contribution of both outputs;

$$V_i = V_1 * \frac{\text{Par}[(R_2 + Z_0), Z_i]}{\text{Par}[(R_2 + Z_0), Z_i] + R_1} + V_2 * \frac{\text{Par}[R_1, Z_i]}{2 * Z_0};$$

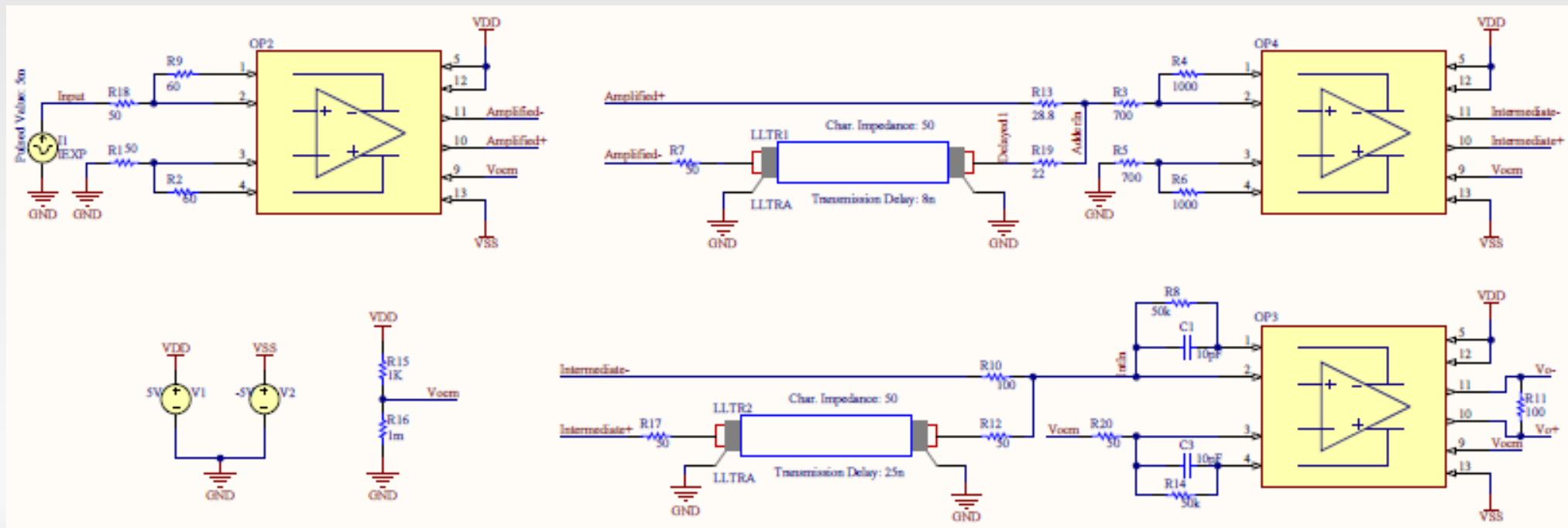
$$R_2 \rightarrow Z_0 - \frac{R_1 Z_i}{R_1 + Z_i}$$

$$\frac{\frac{\text{Par}[R_1, Z_i]}{2 * Z_0}}{\frac{\text{Par}[(R_2 + Z_0), Z_i]}{\text{Par}[(R_2 + Z_0), Z_i] + R_1}} = G;$$

$$R_1 \rightarrow \frac{1}{2} \left(2 G Z_0 - Z_i - G Z_i + \sqrt{8 G Z_0 Z_i + (Z_i + G (-2 Z_0 + Z_i))^2} \right)$$

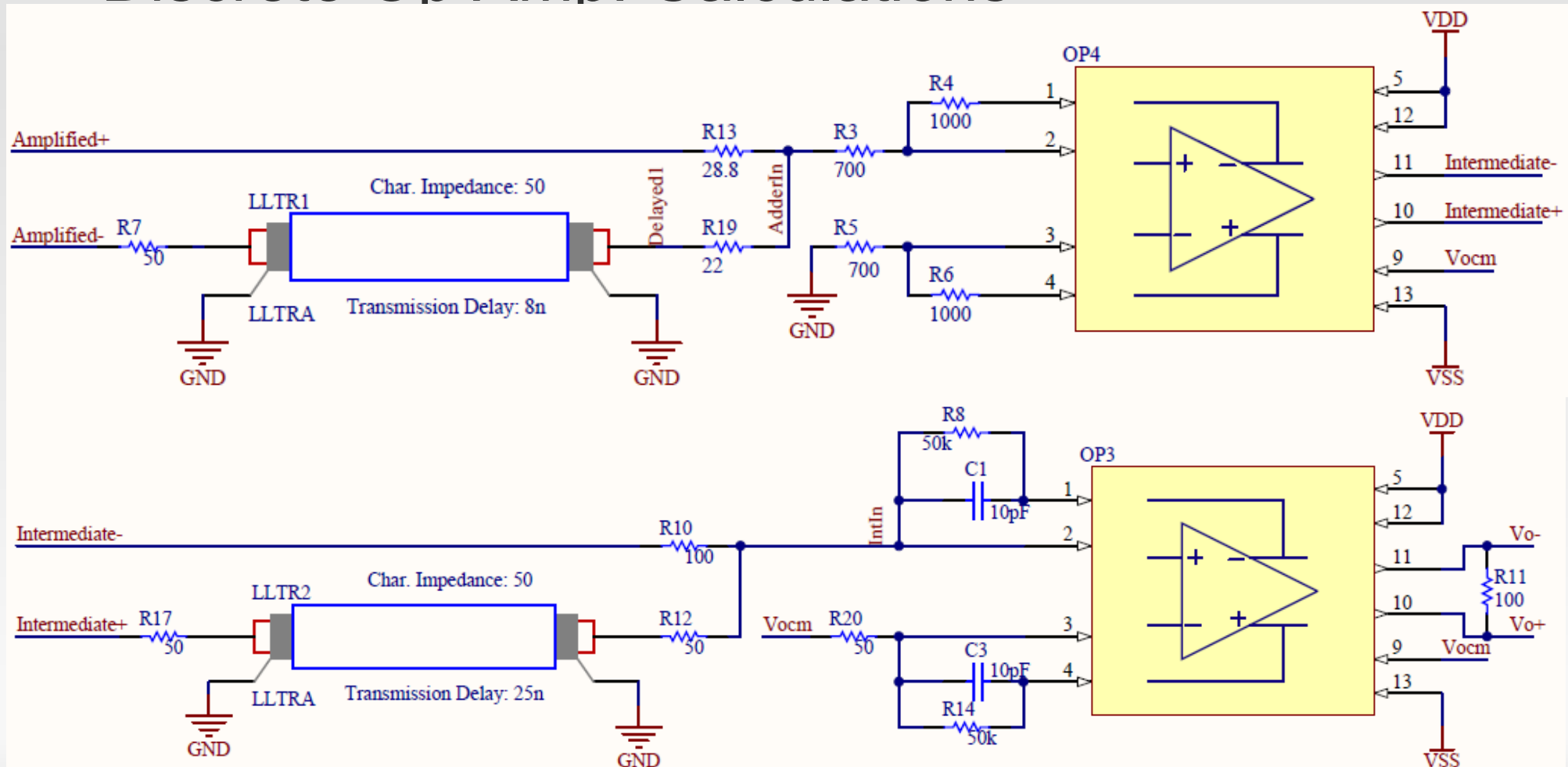
• The analogical mezzanine prototype

- Discrete Op Amp: Calculations
 - Also calculations for the integrator:
 - Same ideas. Adaptation & Same Contribution.



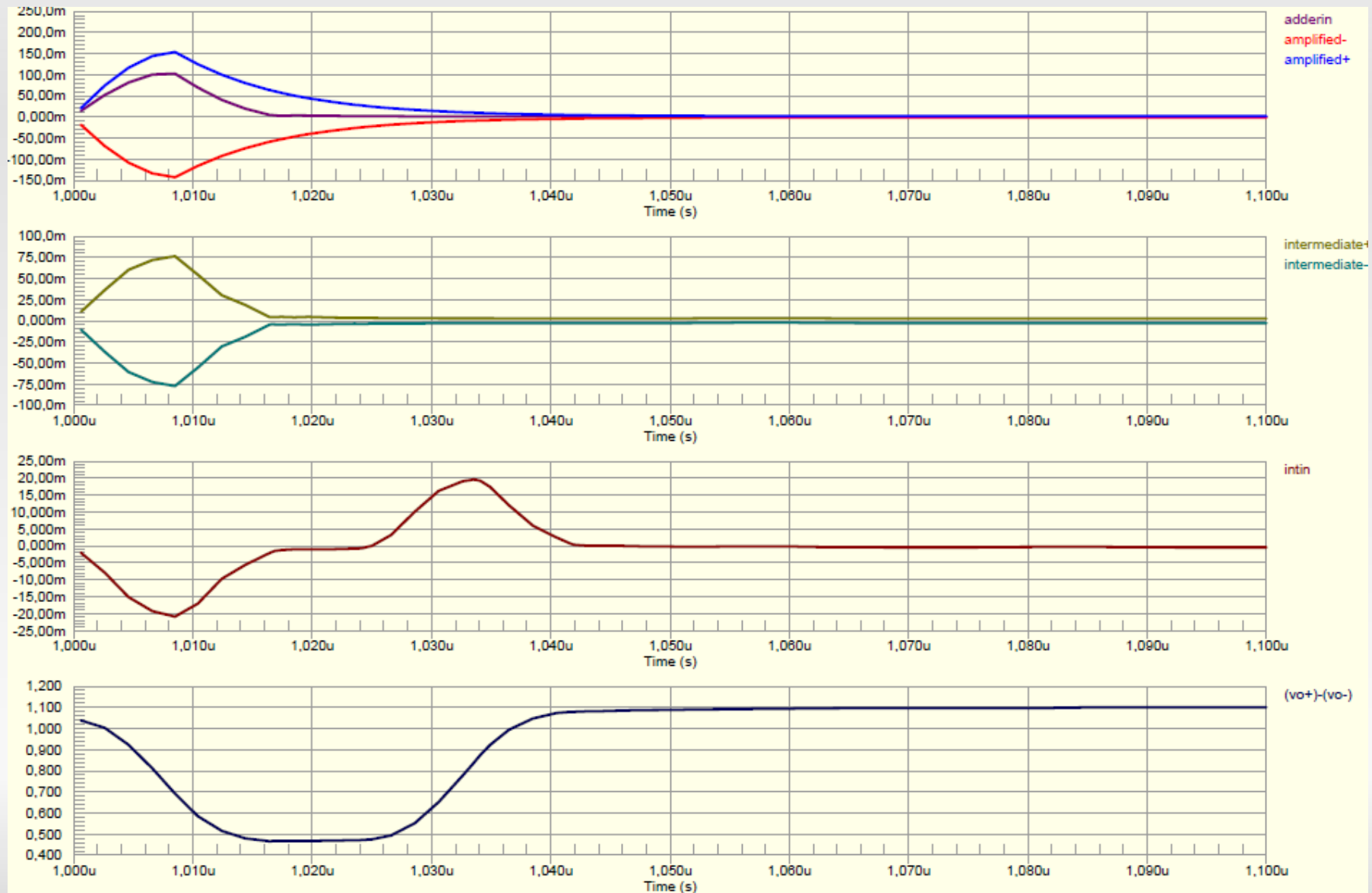
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■ Discrete Op Amp: Calculations



Simulation Results

■ Discrete Op Amp: Results



Conclusion

- A differential output was needed because of the interface with the ADC
- NOT a differential scheme, only uses differential OP Amps
- Studying the possibility of decreasing power
- Relatively low resistances → low noise, possible to decrease them even more, under study
- Needs noise and linearity studies