Low noise preamplifier

Upgrade of the front end electronics of the LHCb calorimeter

Calorimeter upgrade meeting – LAL /Orsay – December 17th 2009

Outlook

I. Introduction
II. LAPAS chip for ATLAR LAr calorimeter
III. Voltage output vs current output
IV. Current output / mixed feedback
V. Current output / current feedback
VI. Discussion

I. Introduction: requirements

- Requirements as agreed during last year (PM gain 1/5):

	Value	Comments
Energy range	0-10 GeV/c (ECAL) Transverse energy	1-3 Kphe / GeV Total energy
Calibration	4 fC /2.5 MeV / ADC cnt	4 fC input of FE card: assuming 25 Ω clipping at PMT base 12 fC / ADC count if no clipping
Dynamic range	4096-256=3840 cnts :12 bit	Enough? New physic req.? Pedestal variation? Should be enough
Noise	<≈1 ADC cnt or ENC < 5 -6 fC	< 0.7 nV/√Hz
Termination	50 ± 5 Ω	Passive vs. active
AC coupling	Needed	Low freq. (pick-up) noise
Baseline shift Prevention	Dynamic pedestal subtraction (also needed for LF pick-up)	How to compute baseline? Number of samples needed?
Max. peak current	4-5 mA over 25 Ω 1.5 mA at FE input if clipping	50 pC in charge
Spill-over correction	Clipping	Residue level: 2 % ± 1 % ?
Spill-over noise	<< ADC cnt	Relevant after clipping?
Linearity	< 1%	
Crosstalk	< 0.5 %	
Timing	Individual (per channel)	PMT dependent

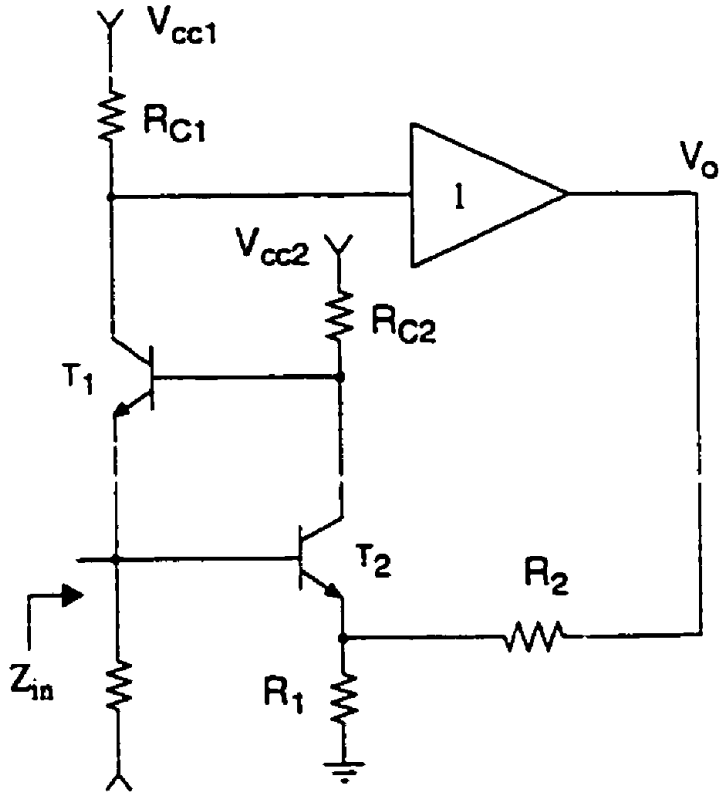
See talk about noise in June's meeting:

http://indico.cern.ch/materialDisplay.py?contribId=1&sessionId=0&materialId=slides&confId=59892

I. Introduction: active line termination

- Electronically cooled termination required:
  - 50 Ohm noise is too high
  - e. g. ATLAS LAr (discrete component)
- Common gate with double voltage feedback
  - Inner loop to reduce input impedance preserving linearity and with low noise
  - Outer loop to control the input impedance accurately

$$Z_i \approx \frac{1/g_{m1}}{G} + R_{C1}\frac{R_1}{R_1+R_2}$$



- Transimpedance gain is given by R_{C1}
- Noise is < 0.5 nV/sqrt(Hz)
  - Small value for R1 and R2
  - Large gm1 and gm2
- Need ASIC for LHCb
  - 32 ch / board: room and complexity

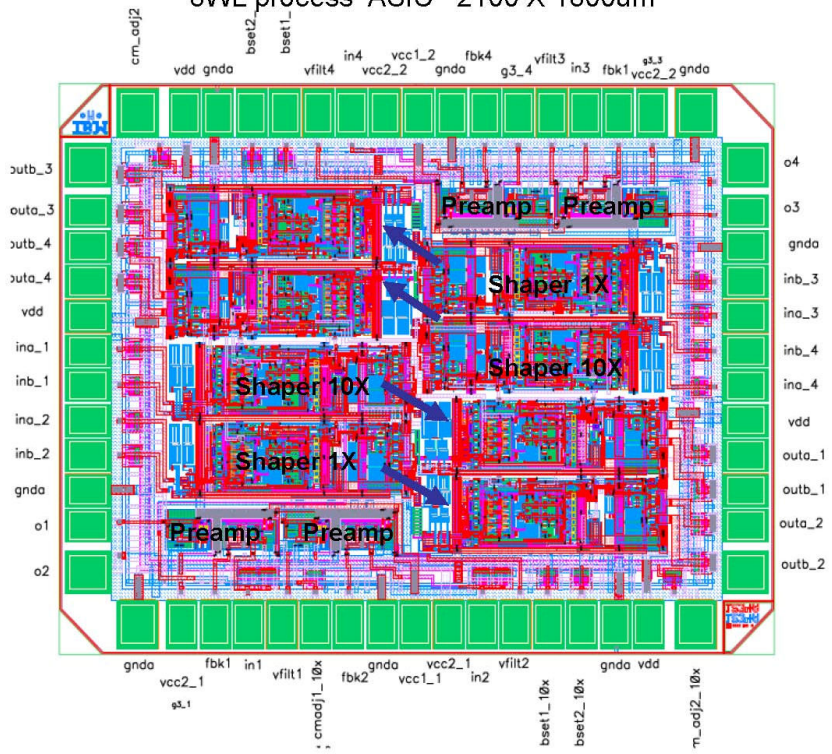
II. LAPAS chip for ATLAS LAr upgrade

- TWEPP 09

LAPAS: A SiGe Front End Prototype for the Upgraded ATLAS LAr Calorimeter

Mitch Newcomer
On Behalf of the ATLAS LAr Calorimeter Group*

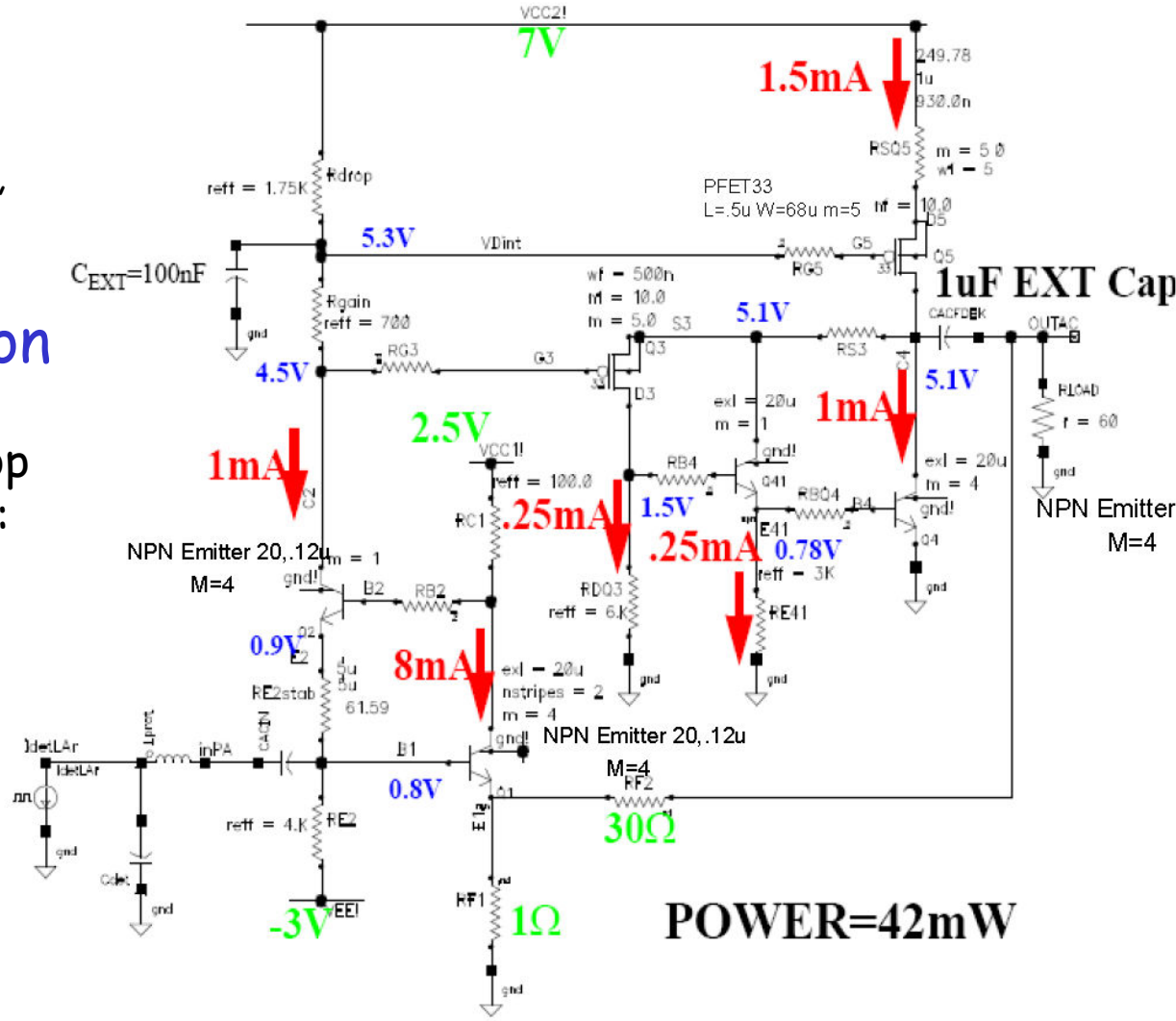
LAPAS: Liquid Argon PreAmplifier Shaper
8WL process ASIC 2100 X 1800um



Special Acknowledgment of the significant contributions of Emerson Vernon, Sergio Rescia (BNL) and Nandor Dressnandt (Penn) to this work.

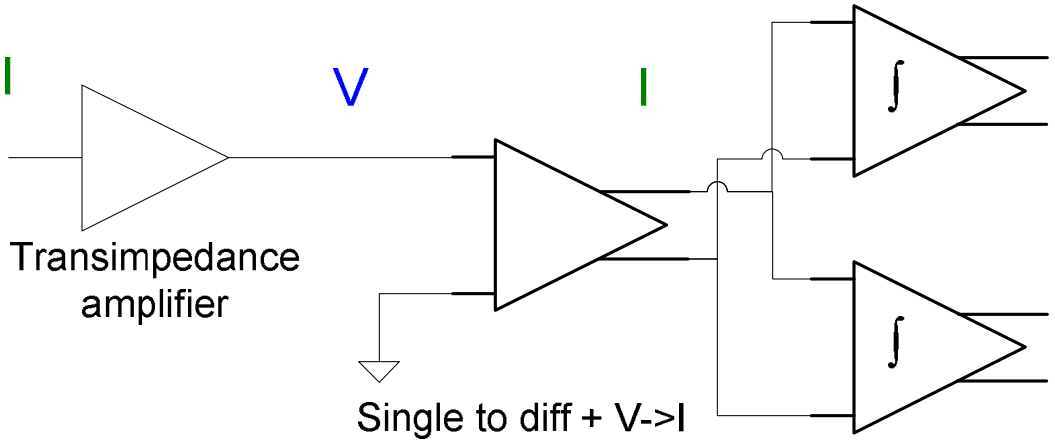
II. LAPAS chip for ATLAS LAr upgrade

- Technology:
  - IBM 8WL SiGe BiCMOS
  - 130 nm CMOS (CERN's techno)
  - More radhard than needed:
    - FEE Rad Tolerance TID~ 300Krad,
    - Neutron Fluence ~10^{13} n/cm^2
- Circuit is "direct" translation
  - Need external 1 uF AC coupling capacitor for outer feedback loop
  - Three pads per channel required:
    - Input
    - Two for AC coupling capacitor
  - Voltage output

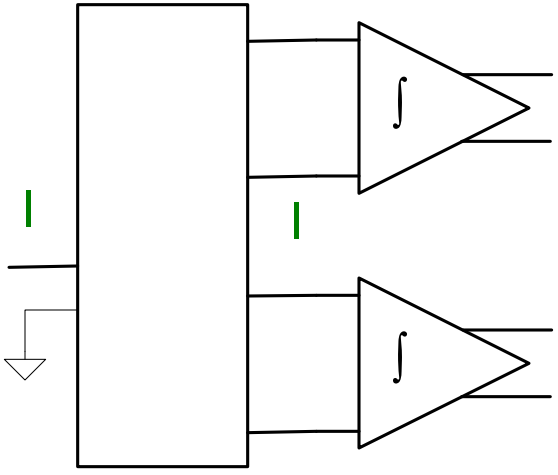


III. Voltage output versus current output

- Voltage output:
  - Pros:
    - Tested
  - Cons:
    - I (PMT) -> V and V -> I (integrate)
    - Larger supply voltage required
    - External components
    - 2 additional pads per channel



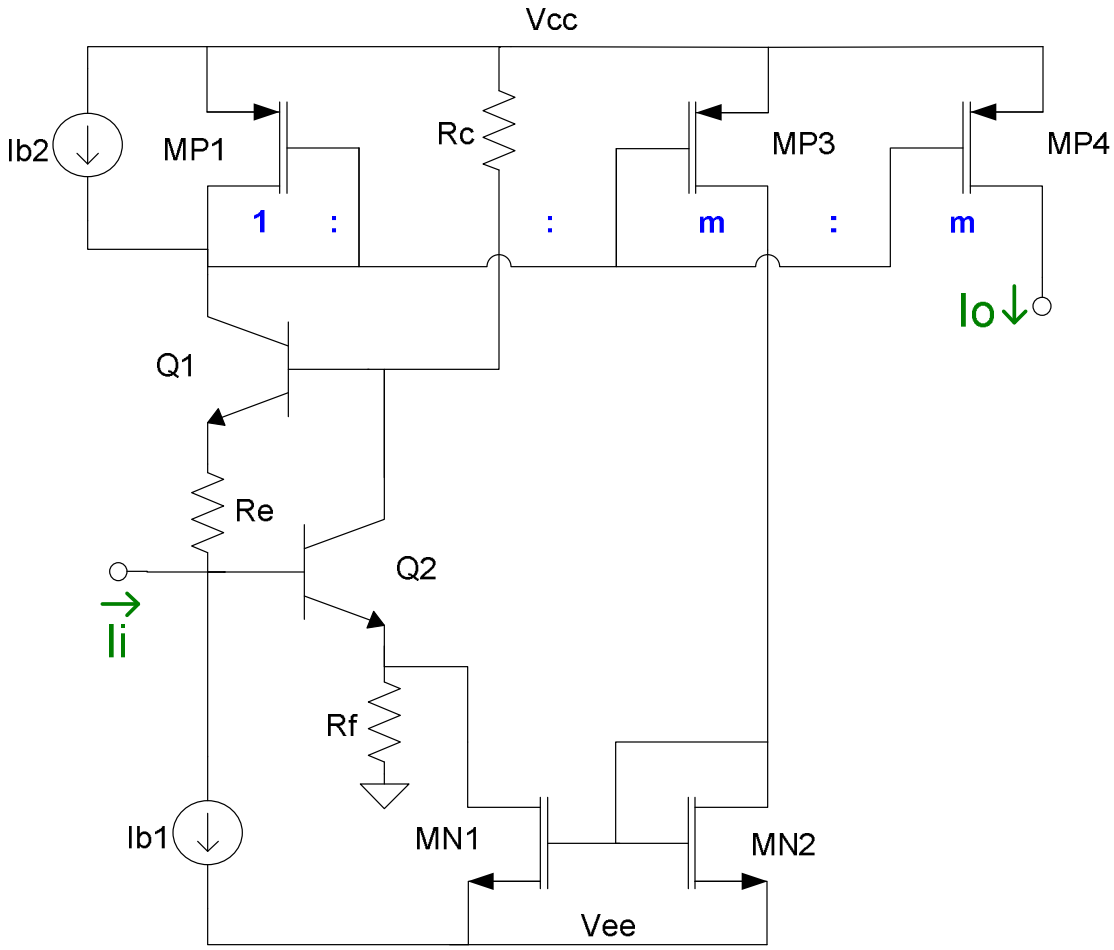
- Current output ("à la PS")
  - Pros:
    - "Natural" current processing
    - Lower supply voltage
    - All low impedance nodes:
      - Pickup rejection
    - No external components
    - No extra pad
  - Cons:
    - Trade-off in current mirrors: linearity vs bandwidth



IV. Current output / mixed feedback

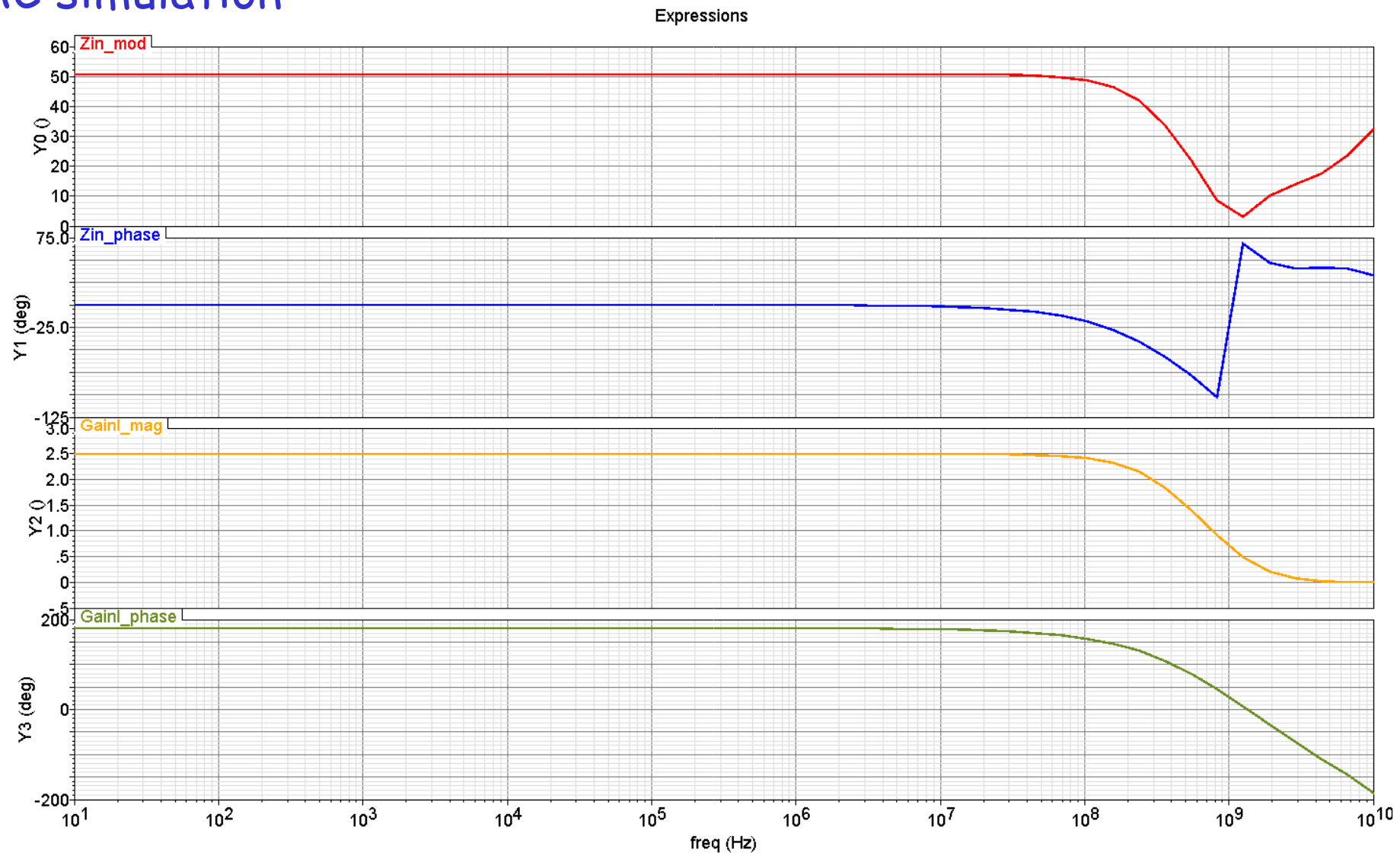
- Mixed mode feedback:
  - Inner loop: lower input impedance
    - Voltage feedback (gain): Q2 and Rc
  - Outer loop: control input impedance
    - Current feedback: mirrors and Rf
- Variation of LAr preamplifier
- Current gain: m
- Input impedance

$$Z_i \approx \frac{1/g_{m1} + \mathrm{Re}}{g_{m2}Rc} + mR_f$$



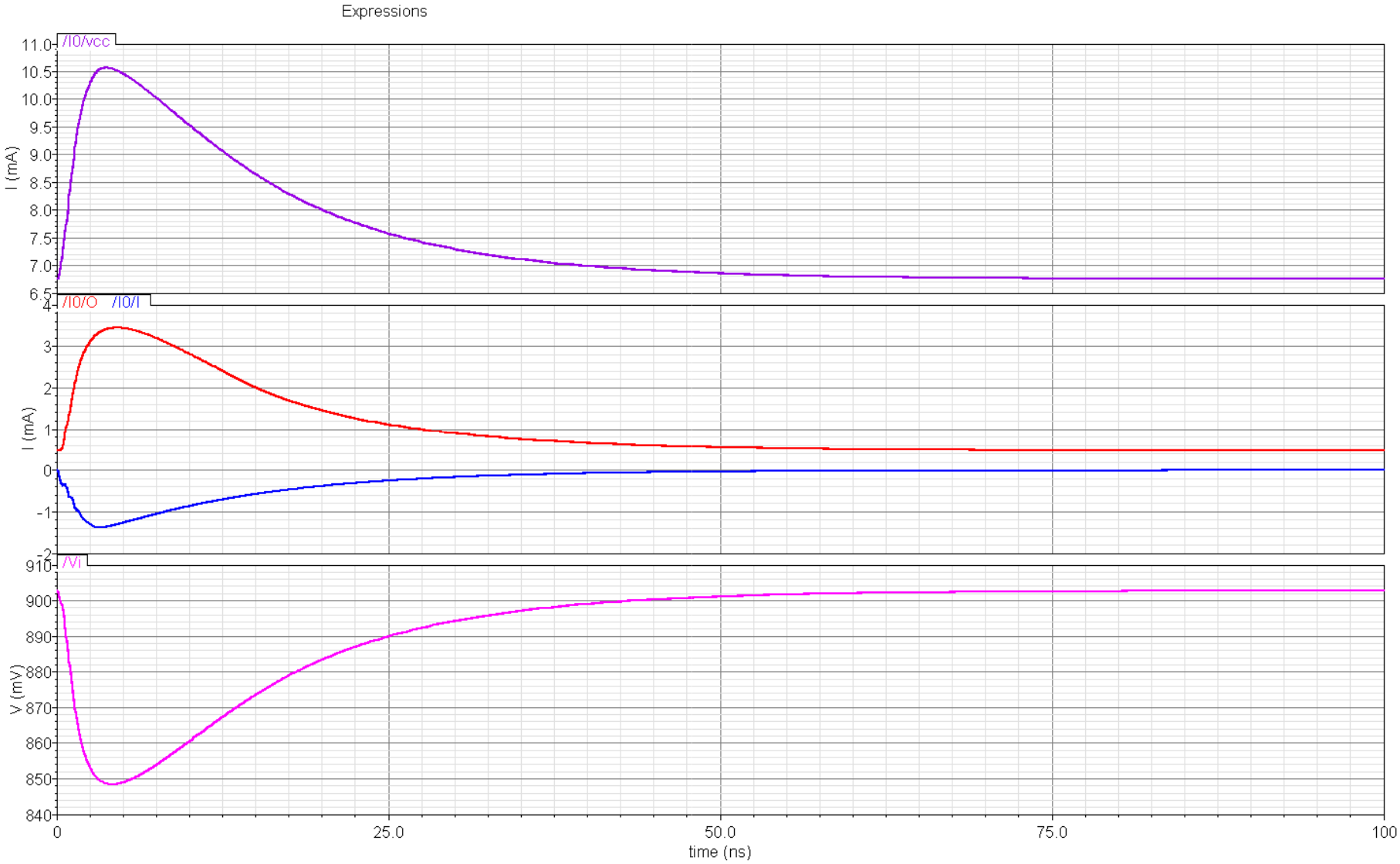
IV. Current output / mixed feedback

- *AC simulation*



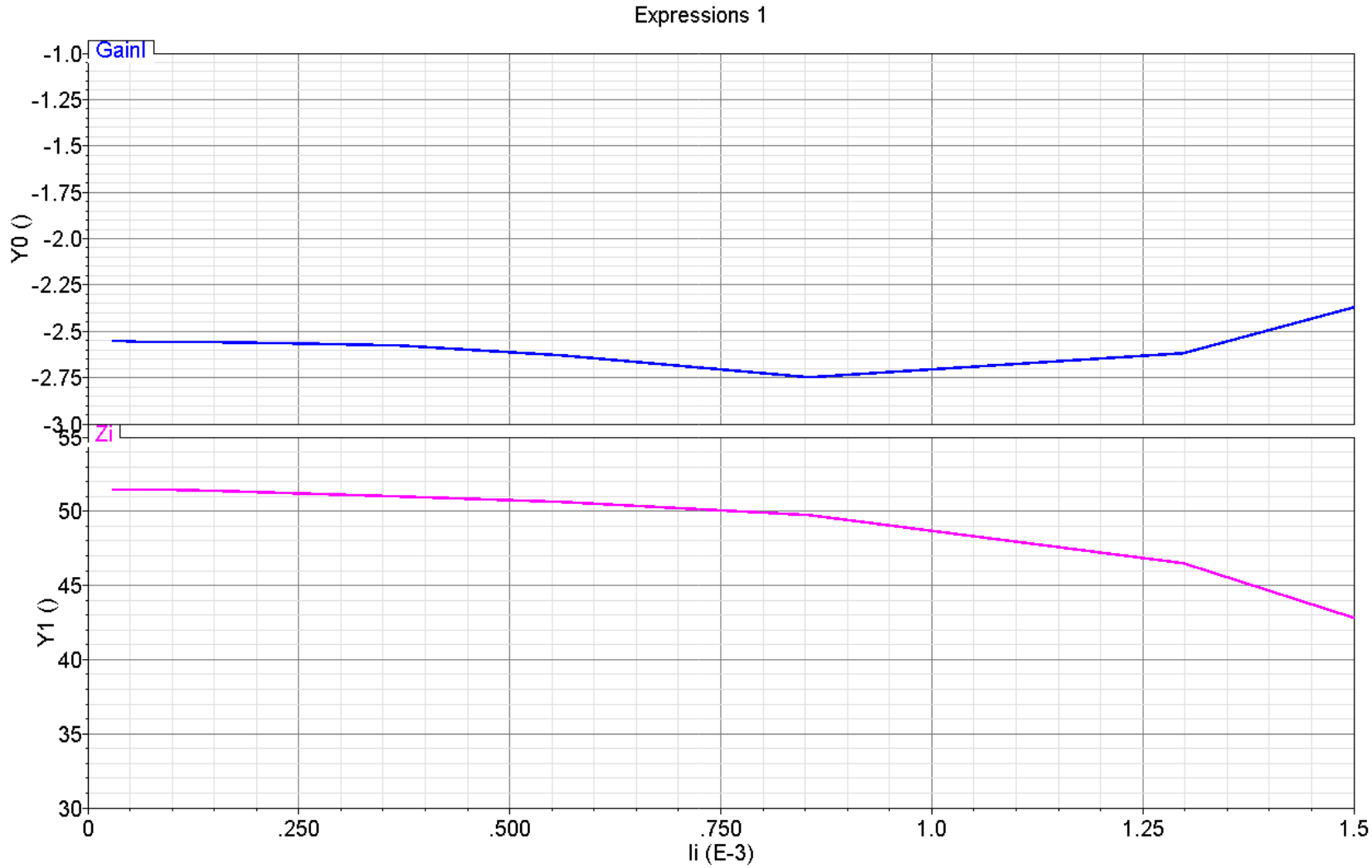
IV. Current output / mixed feedback

- Transient simulation



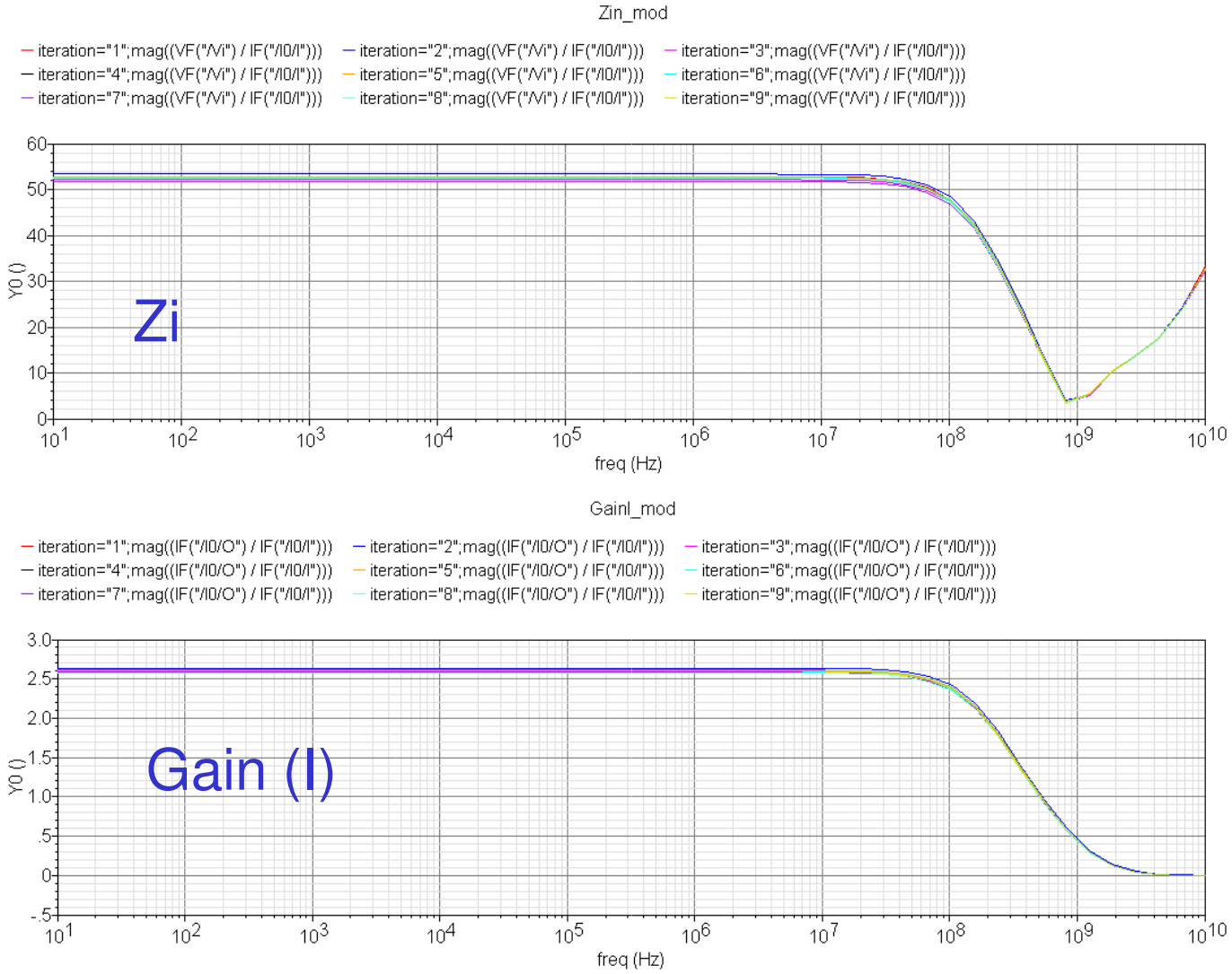
IV. Current output / mixed feedback

- Dynamic input impedance and linearity (mirrors to be optimized)



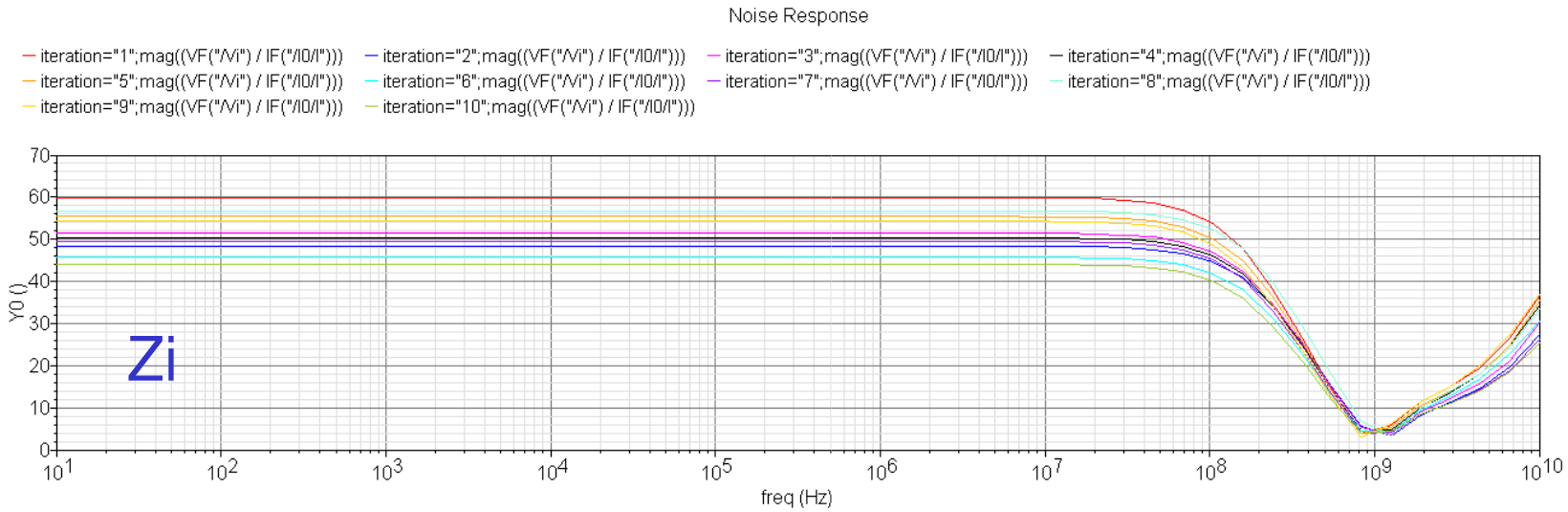
IV. Current output / mixed feedback

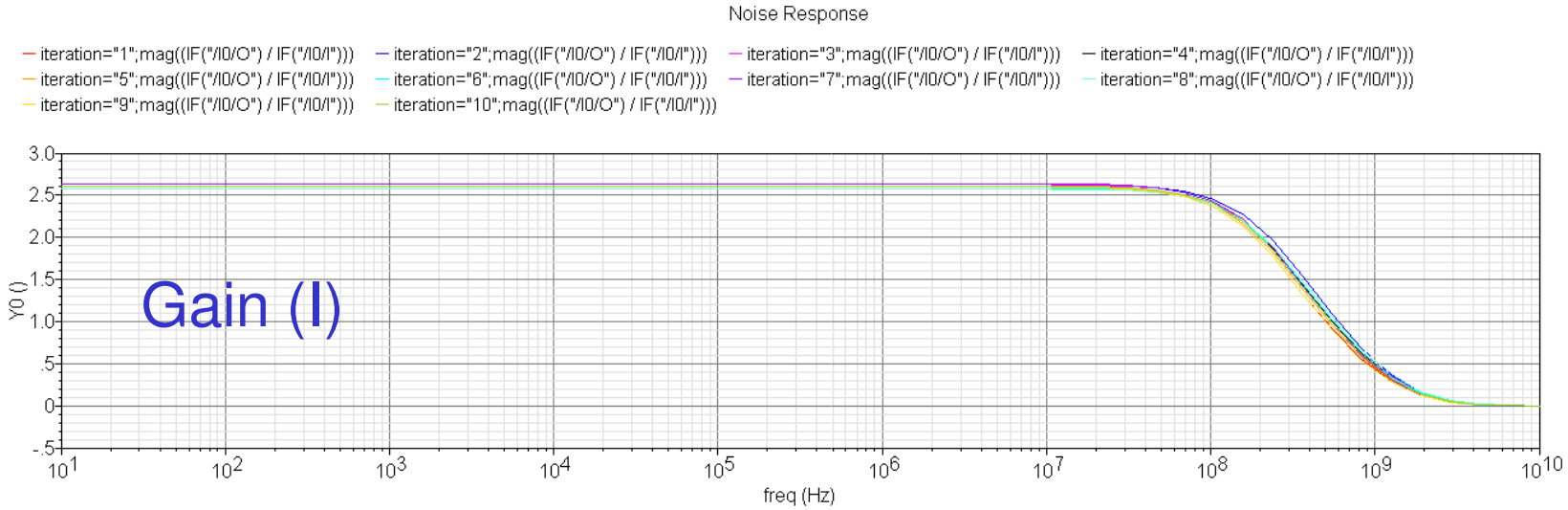
- Monte Carlo simulations: mismatch variation



IV. Current output / mixed feedback

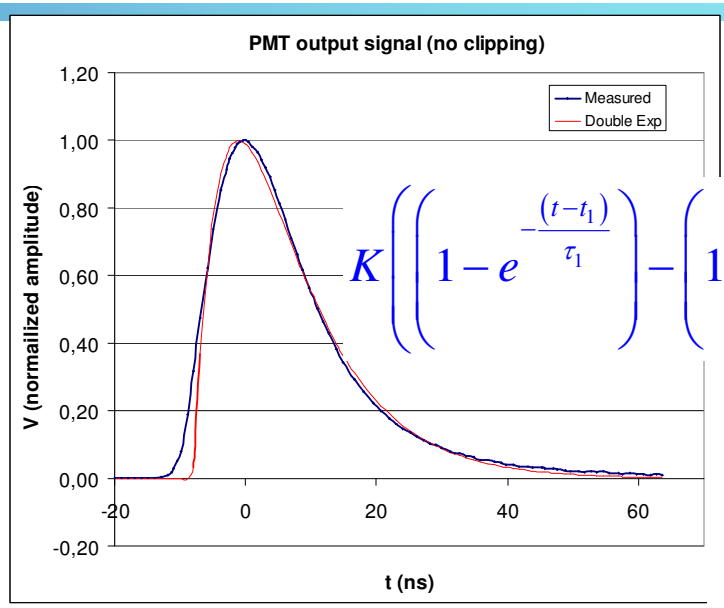
- Monte Carlo simulations: process variation





IV. Current output / mixed feedback

- Full channel simulation:
  - Delay line clipping
  - 12 m cable between PMT and FE
  - Preamplifier (transistor level)
  - Integrator (ideal)
  - Pedestal subtraction (ideal)
    - Skin effect taken into account in cable

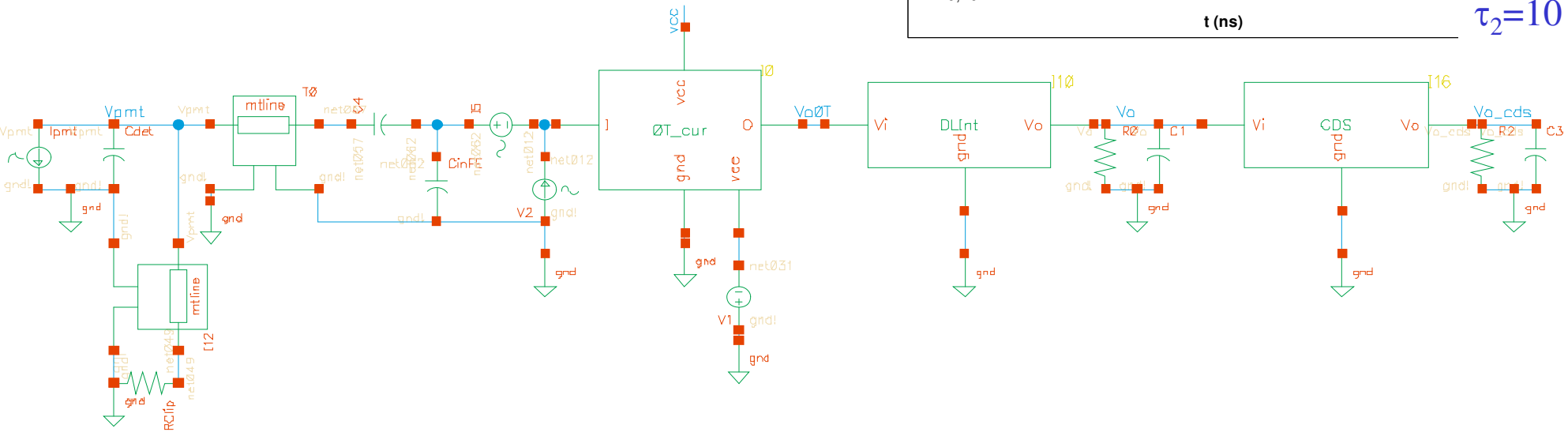


$$K\left(\left(1-e^{-\frac{(t-t_1)}{\tau_1}}\right)-\left(1-e^{-\frac{(t-t_2)}{\tau_2}}\right)\right)$$

$t_1=t_2$

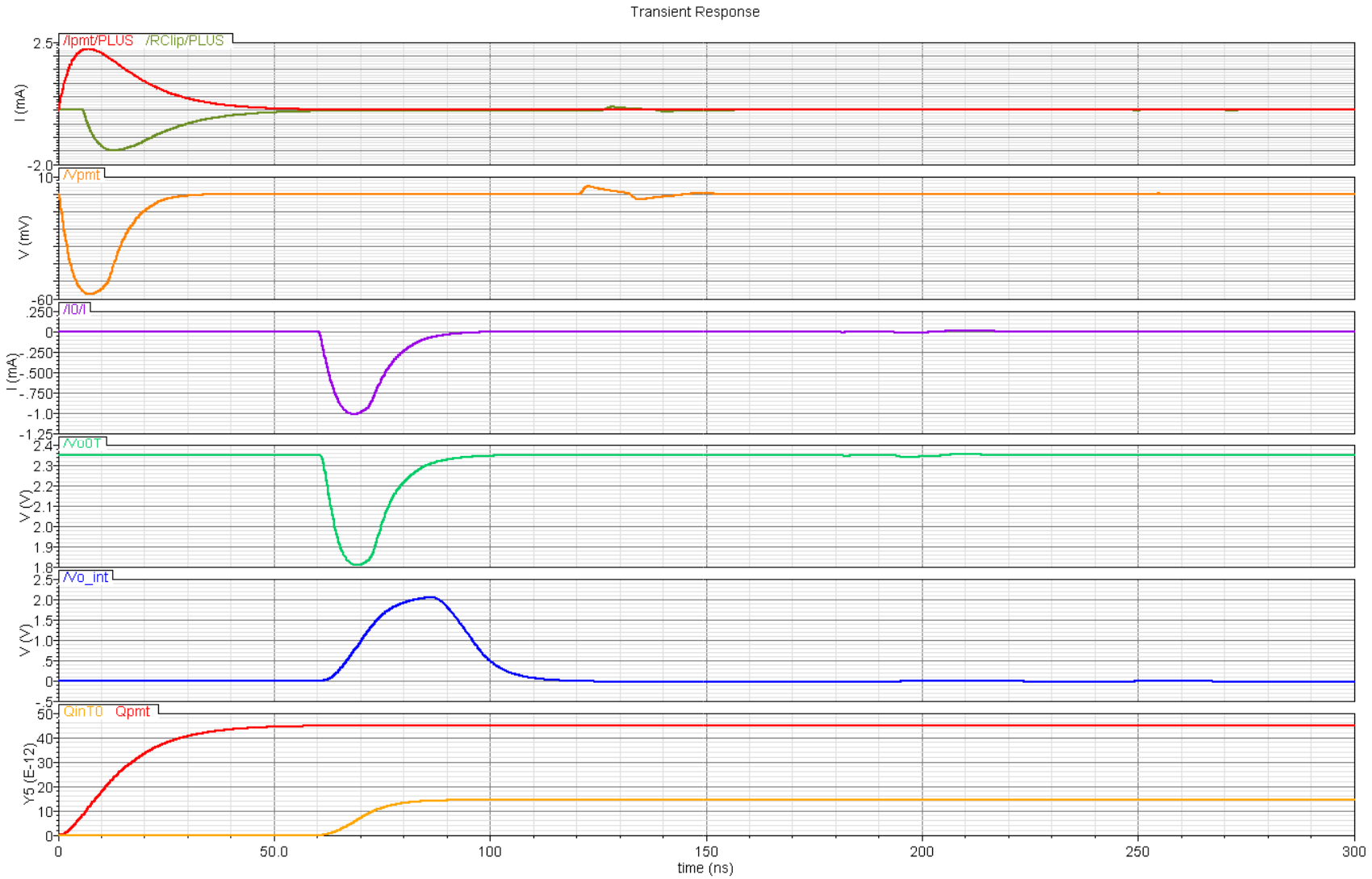
$\tau_1=5$ ns

$\tau_2=10$ ns



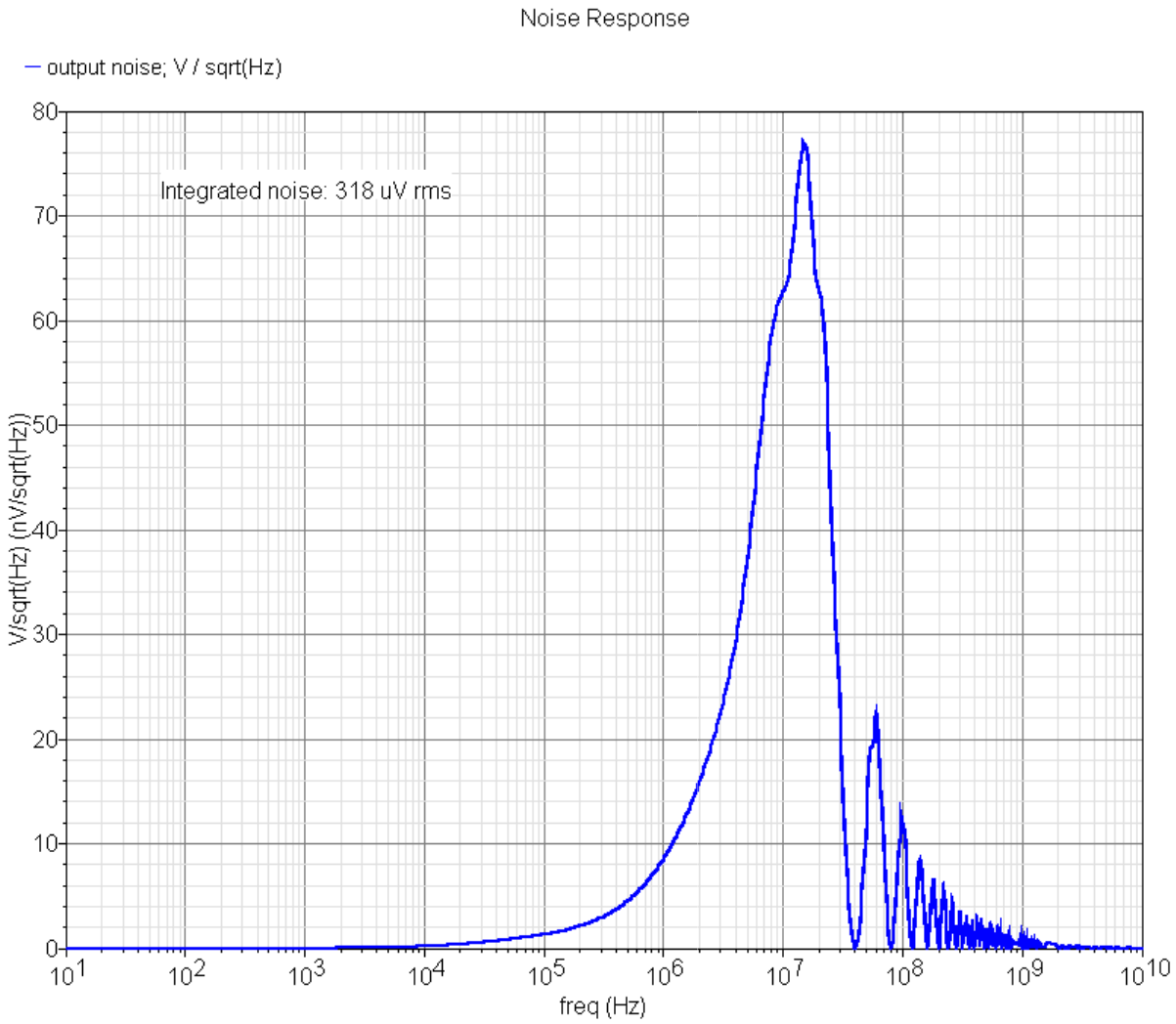
IV. Current output / mixed feedback

- Full channel simulation: transient response



IV. Current output / mixed feedback

- Full channel simulation: noise

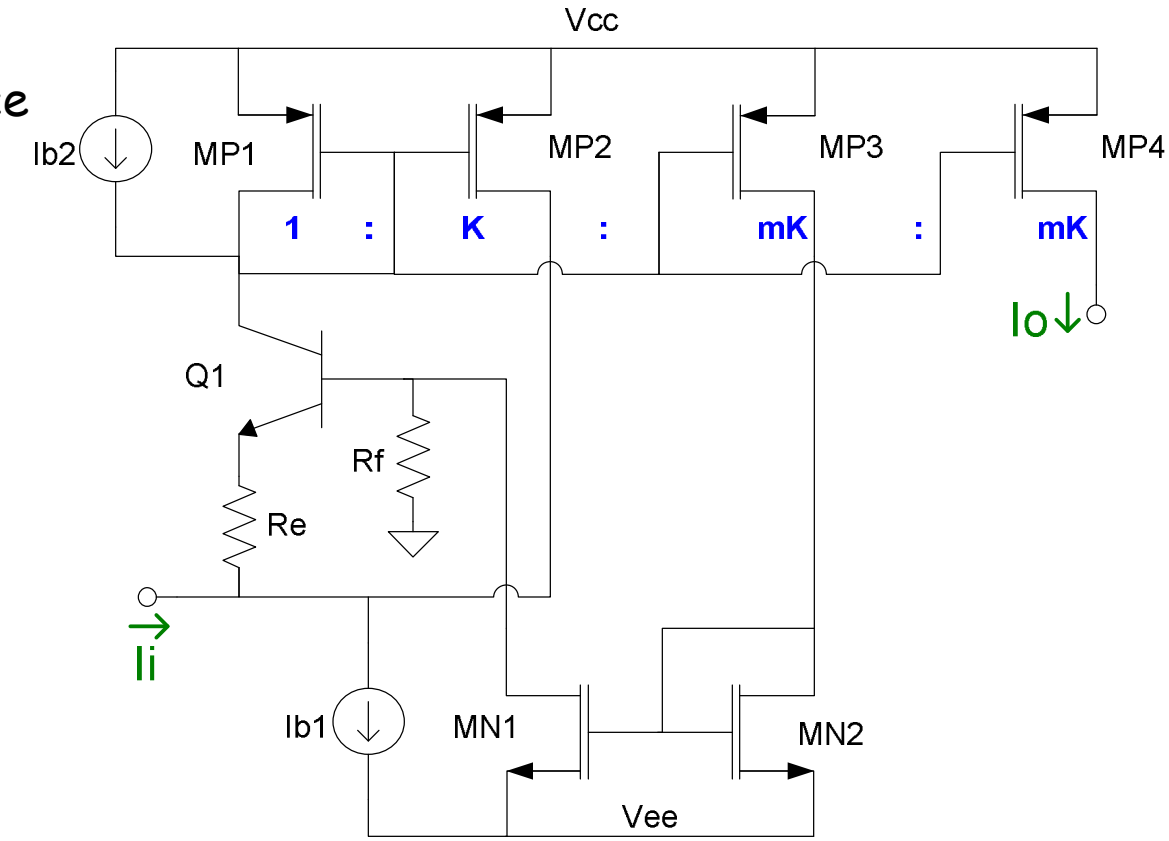


V. Current output / current feedback

- Current mode feedback:
  - Inner loop: lower input impedance
    - Current feedback (gain): mirror: K
  - Outer loop: control input impedance
    - Current feedback: mirror: m
- Current gain: m
- Input impedance

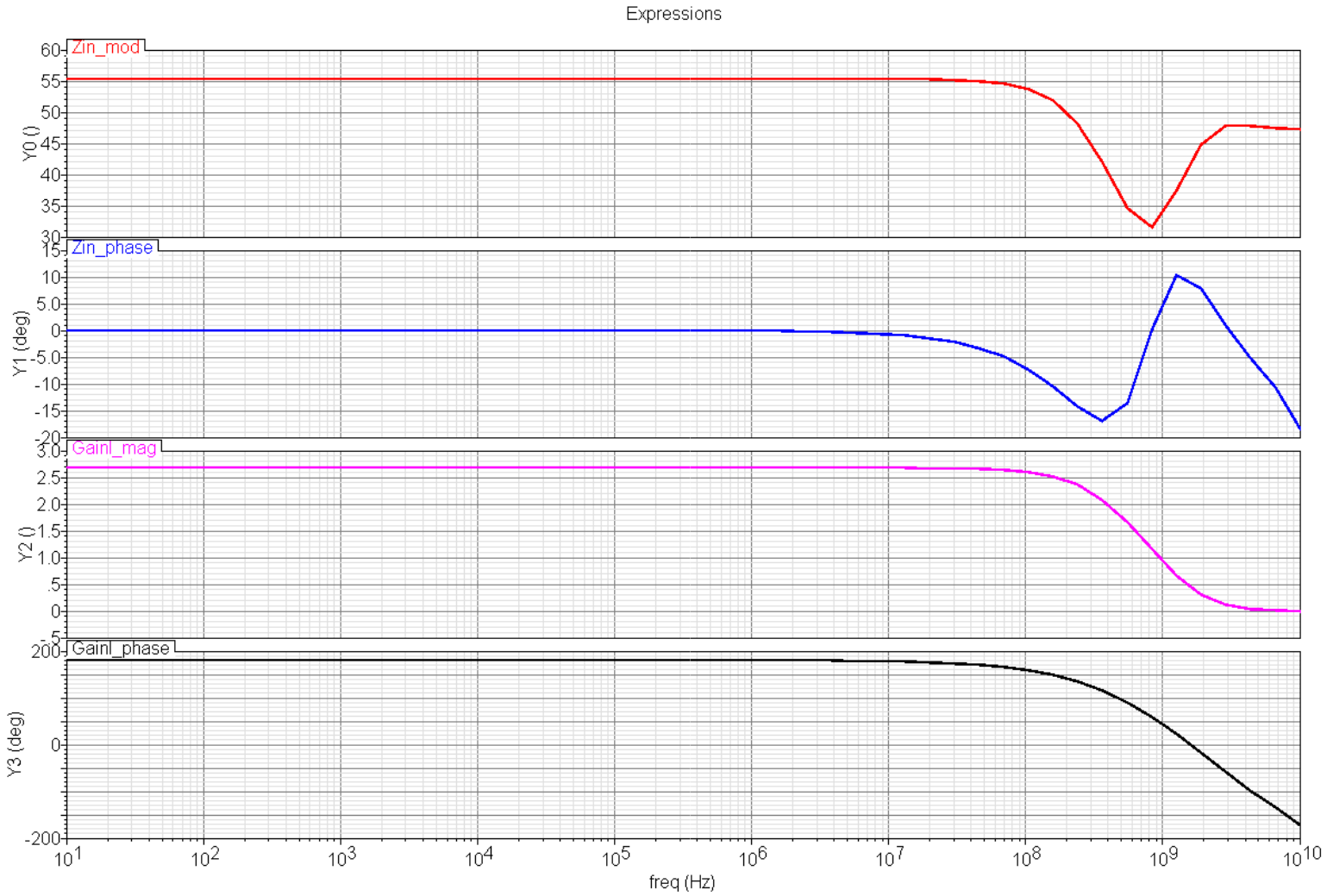
$$Z_i \approx \frac{1/g_{m1} + \mathrm{Re}}{1+K} + \frac{K}{1+K} mR_f$$

- Current mode feedback
  - Optical comunications
  - SiPM readout
- Better in terms of ESD:
  - No input pad connected to any transistor gate or base



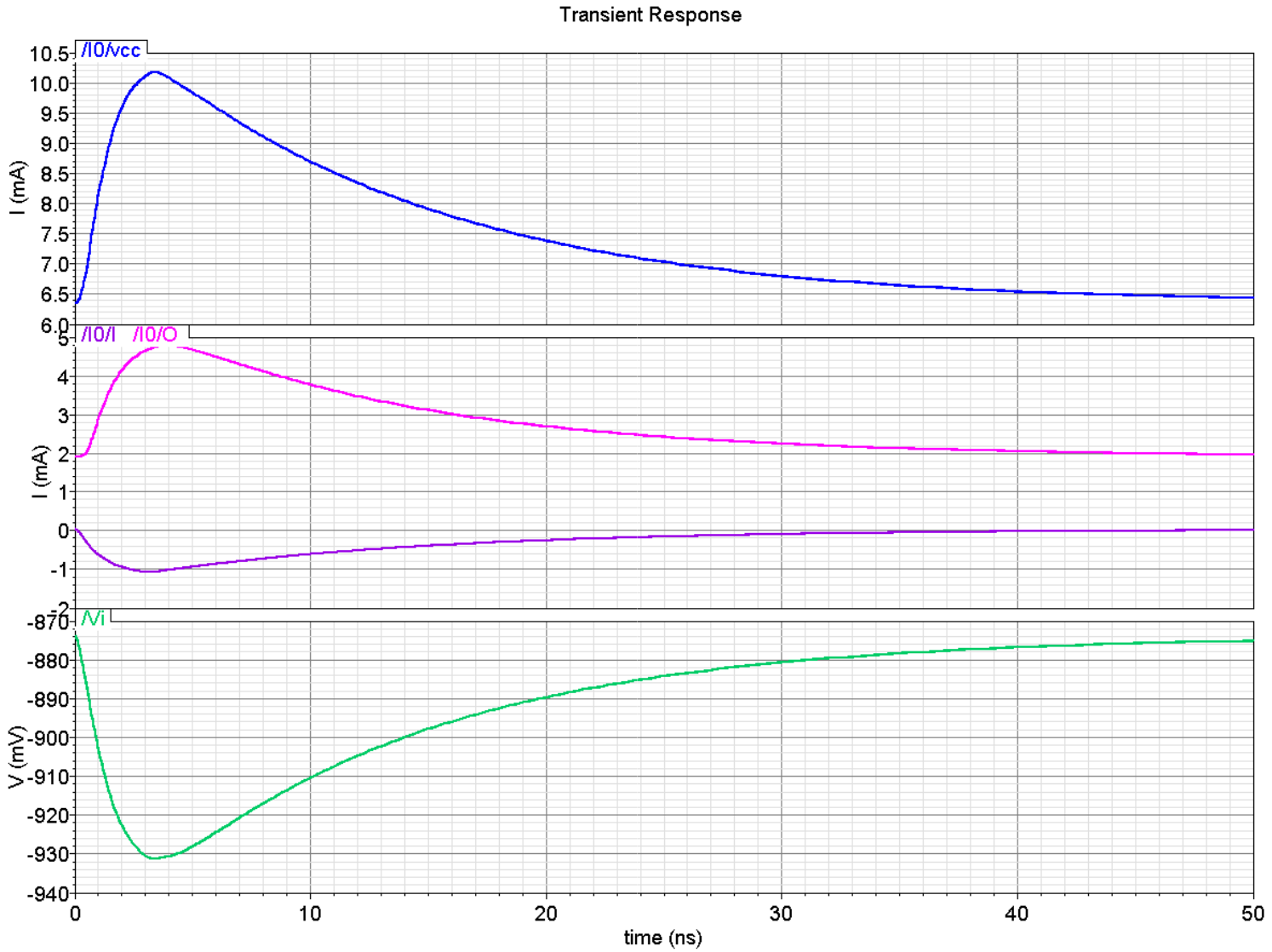
IV. Current output / current feedback

- *AC simulation*



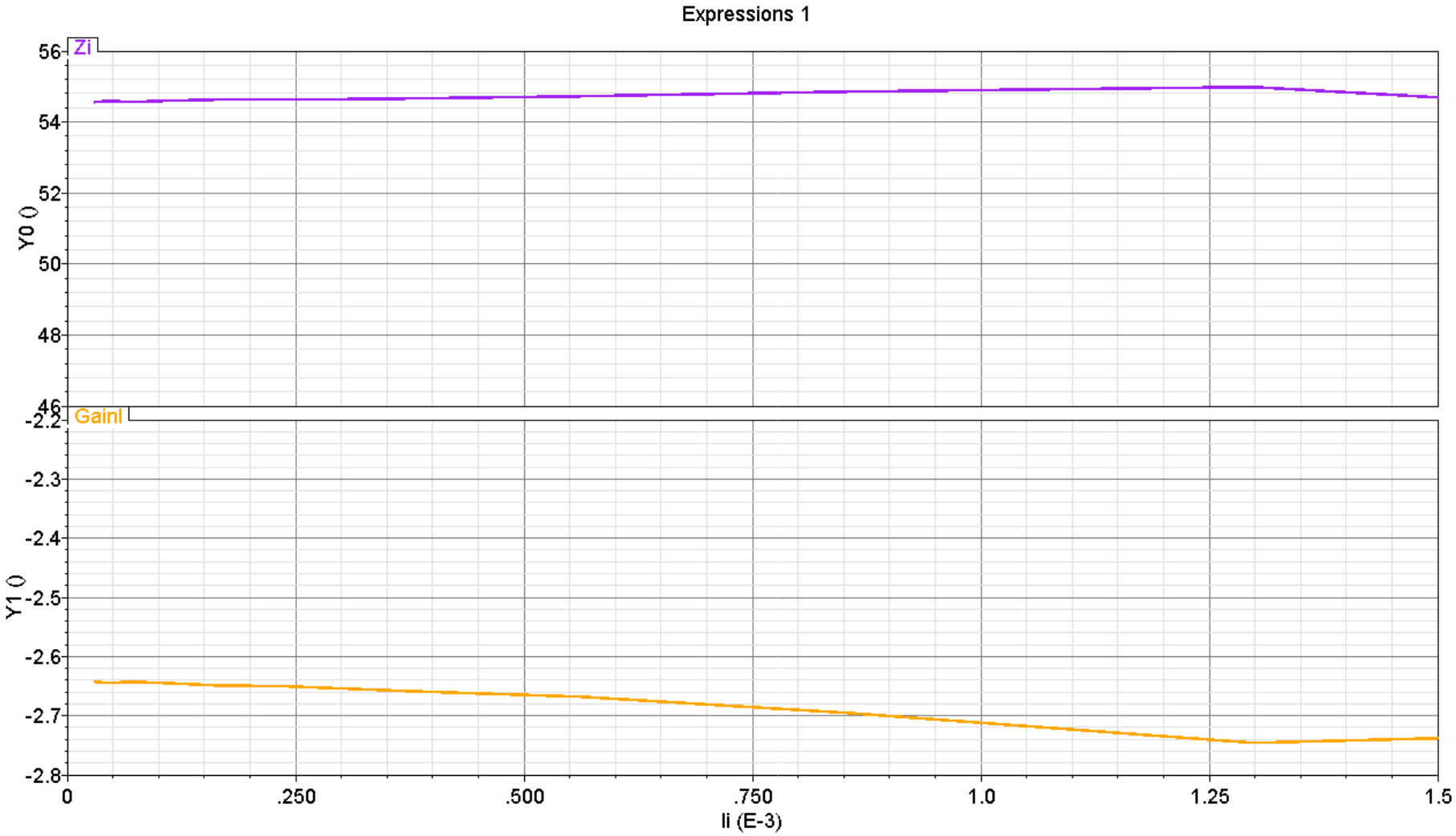
IV. Current output / current feedback

- Transient simulation



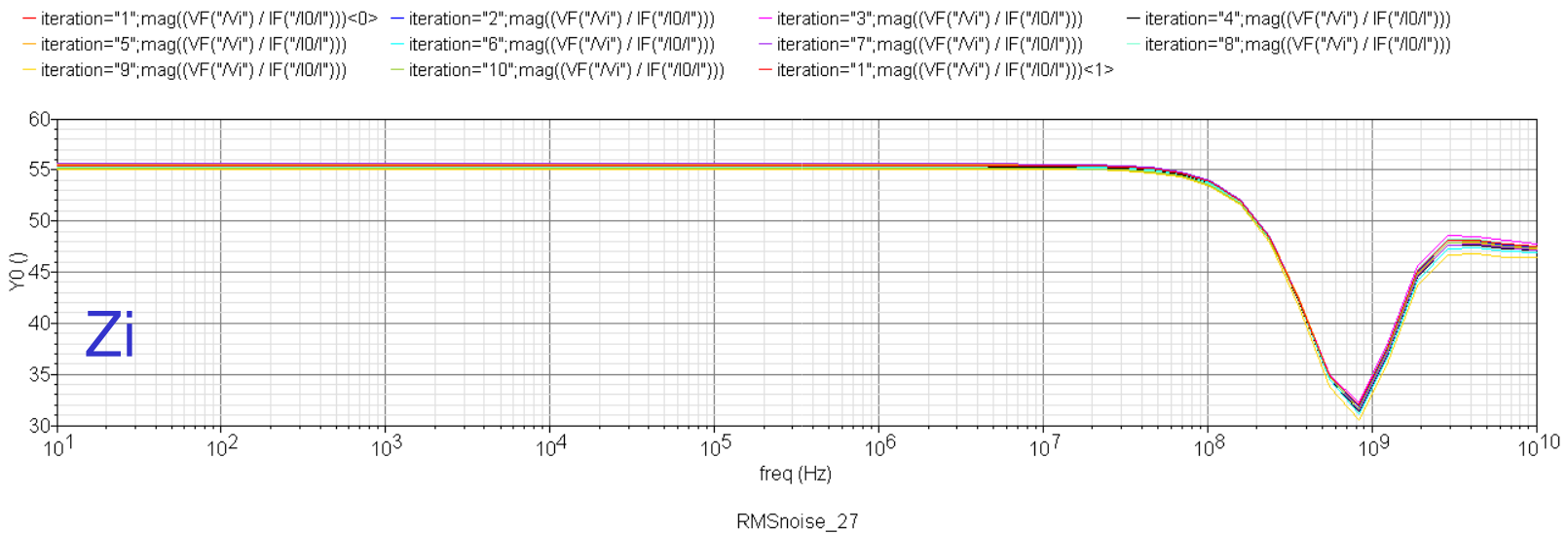
IV. Current output / current feedback

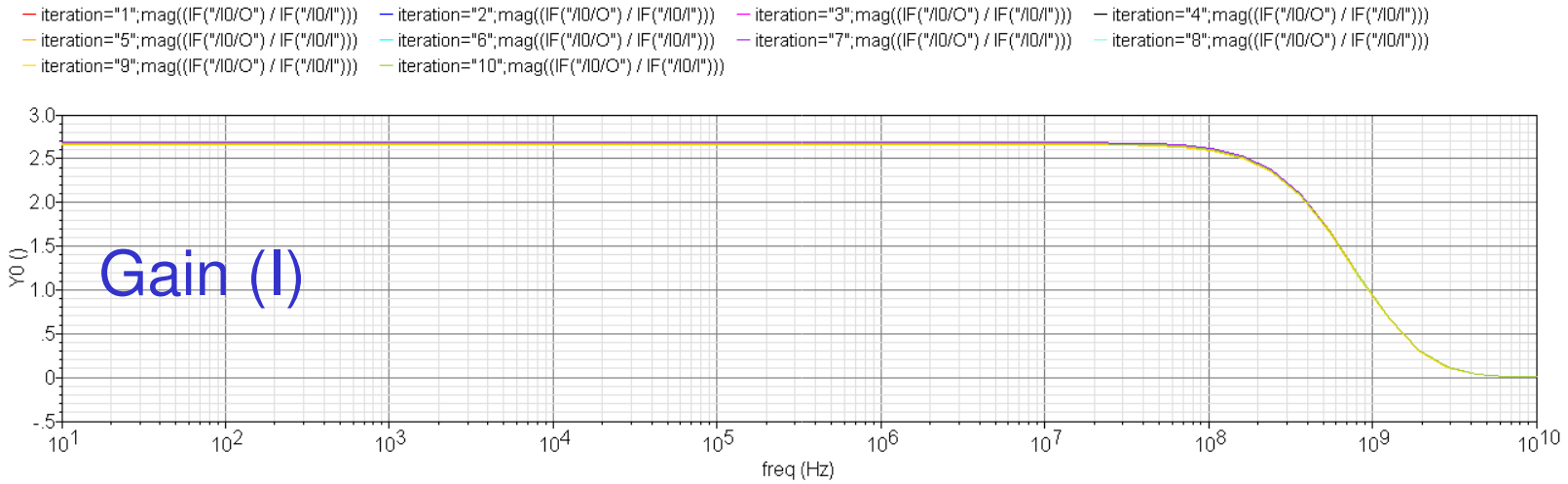
- Dynamic input impedance and linearity



IV. Current output / current feedback

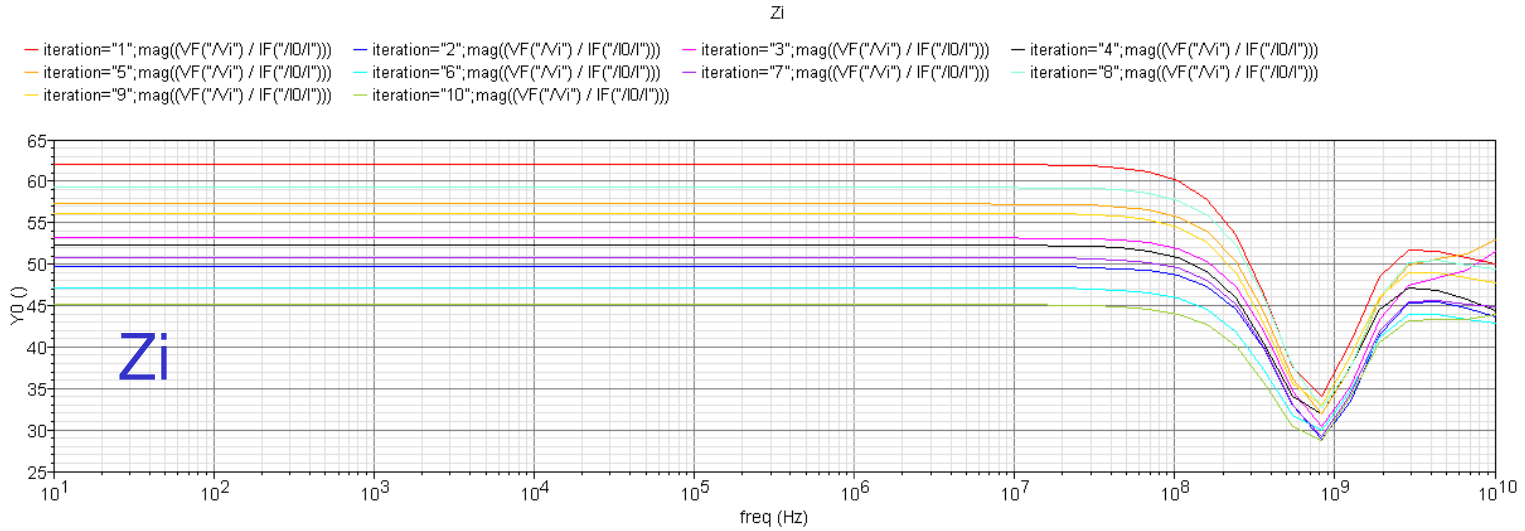
- Monte Carlo simulations: mismatch variation

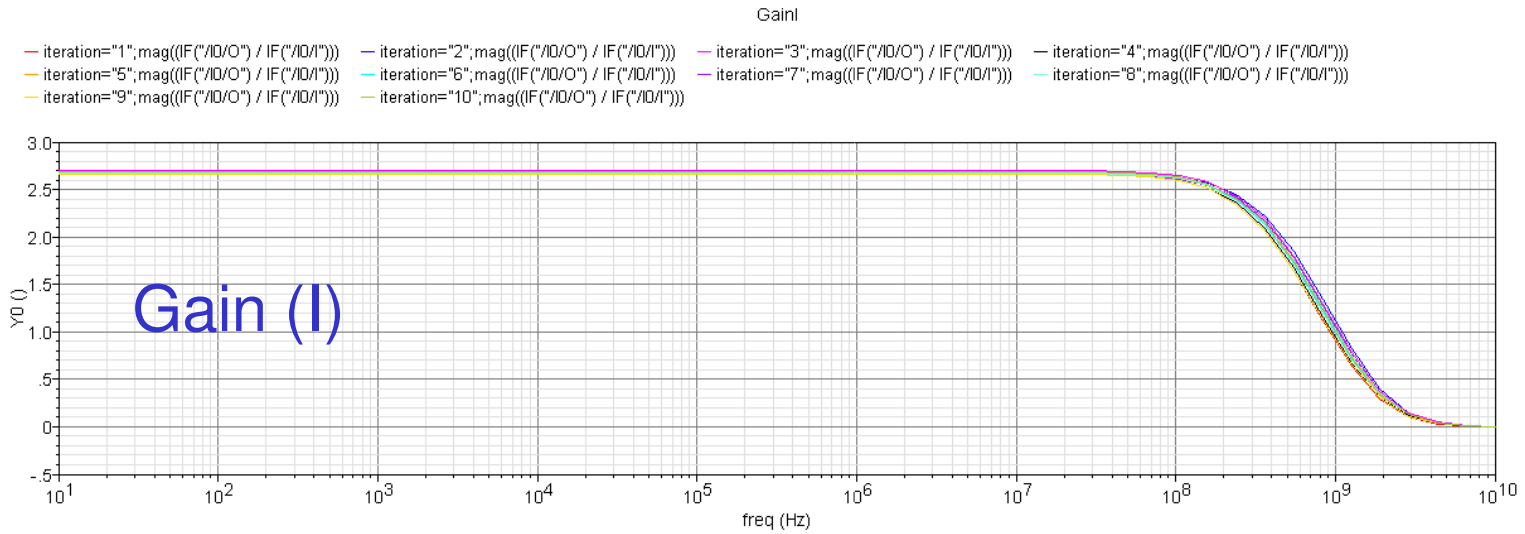




IV. Current output / current feedback

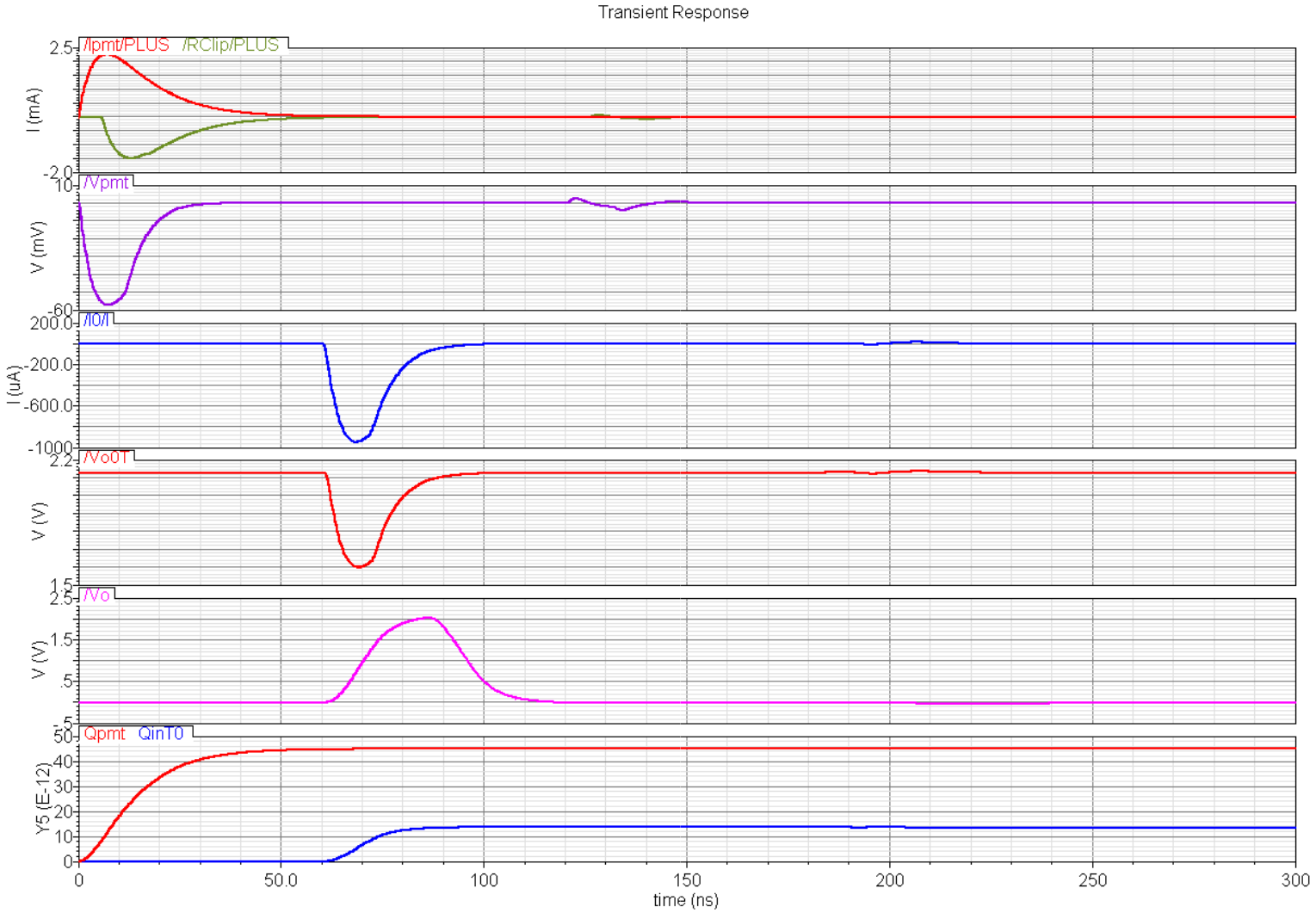
- Monte Carlo simulations: process variation





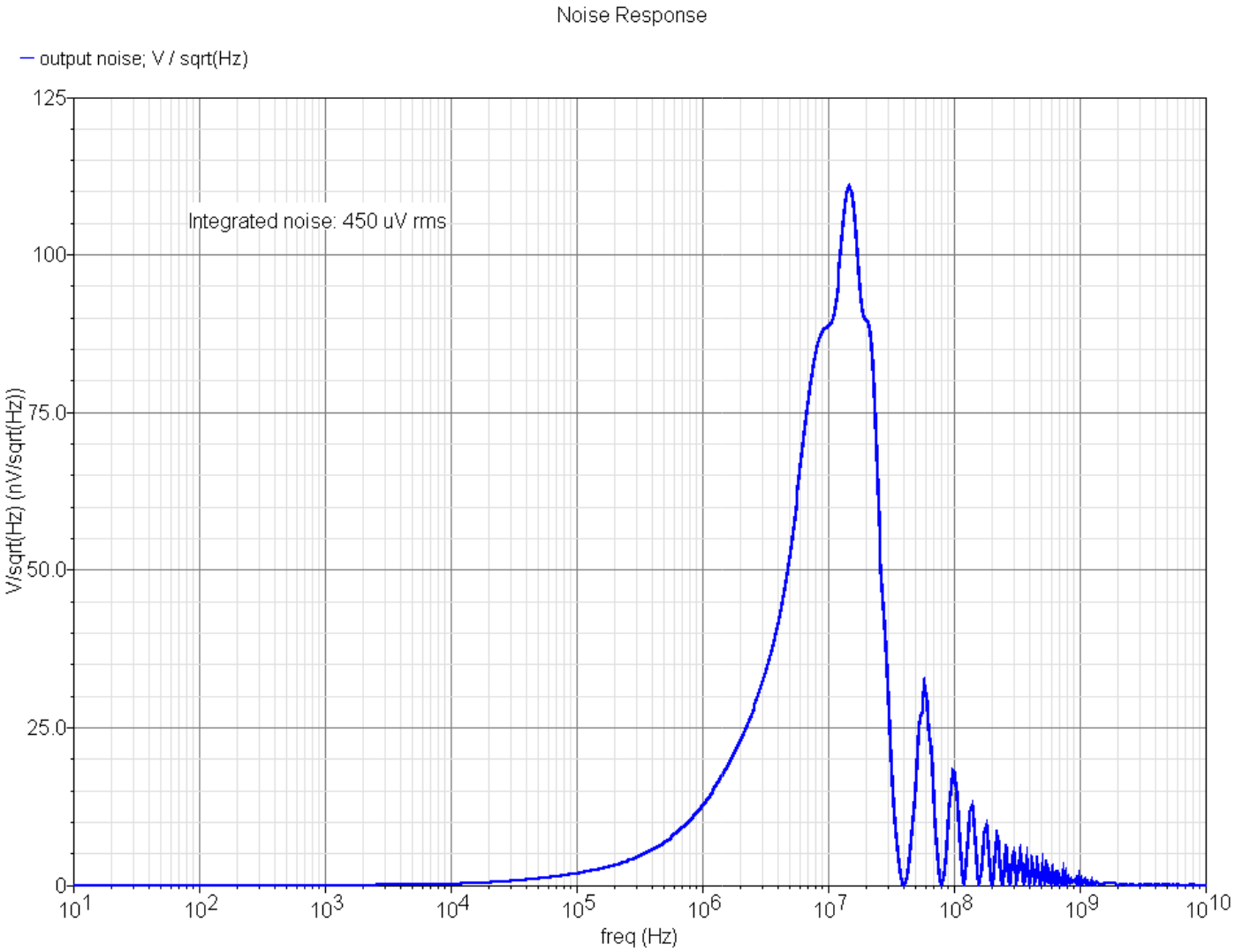
IV. Current output / current feedback

- Full channel simulation: transient response



IV. Current output / current feedback

- Full channel simulation: noise



VI. Discussion

- First simulations of current amplifiers are promising:
  - Z_{in}=50 Ω for full dynamic and BW=100 MHz
  - Noise: 400 μV rms after integration and pedestal subtraction
  - MAIN ISSUE: linearity: 2-3 % error (mirrors not optimized)
    - Trade off: linearity / BW / noise
- Precise analysis:
  - Precise analysis of feedback loops: stability !
  - Noise
- Optimize current mirrors: linearity / dynamic Zi!
- Effect of process variation discussed in general talk
- Plans:
  - Finalize study/optimization
  - Decide to send voltage output or current output (or both)
    - When? March (not mini@sic run) / June