

# Scalable Readout System (SRS)

## intermediate status report

February 24, 2010, RD51 Miniweek

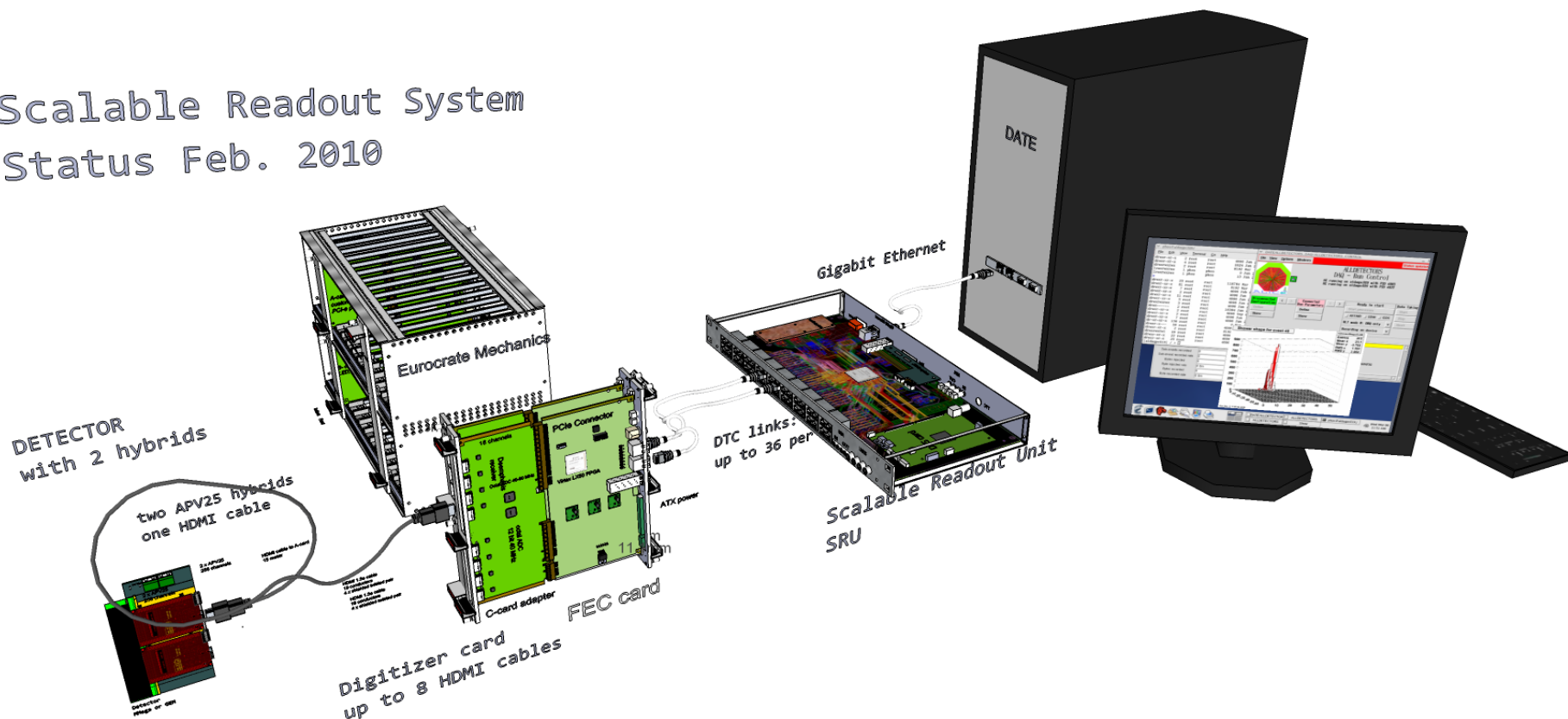
Hans Muller CERN PH Department

Teams, Users , Services involved in the SRS so far:

RD51-WG5 team CERN, NEXT Collaboration UPV Valencia, DATE team ALICE CERN,  
Huazhong Normal University Wuhan, ATLAS MaMa (MiroMega) CERN,  
Florida Tech. University Melbourne USA, PCB shop CERN, Bump Bonding Shop CERN

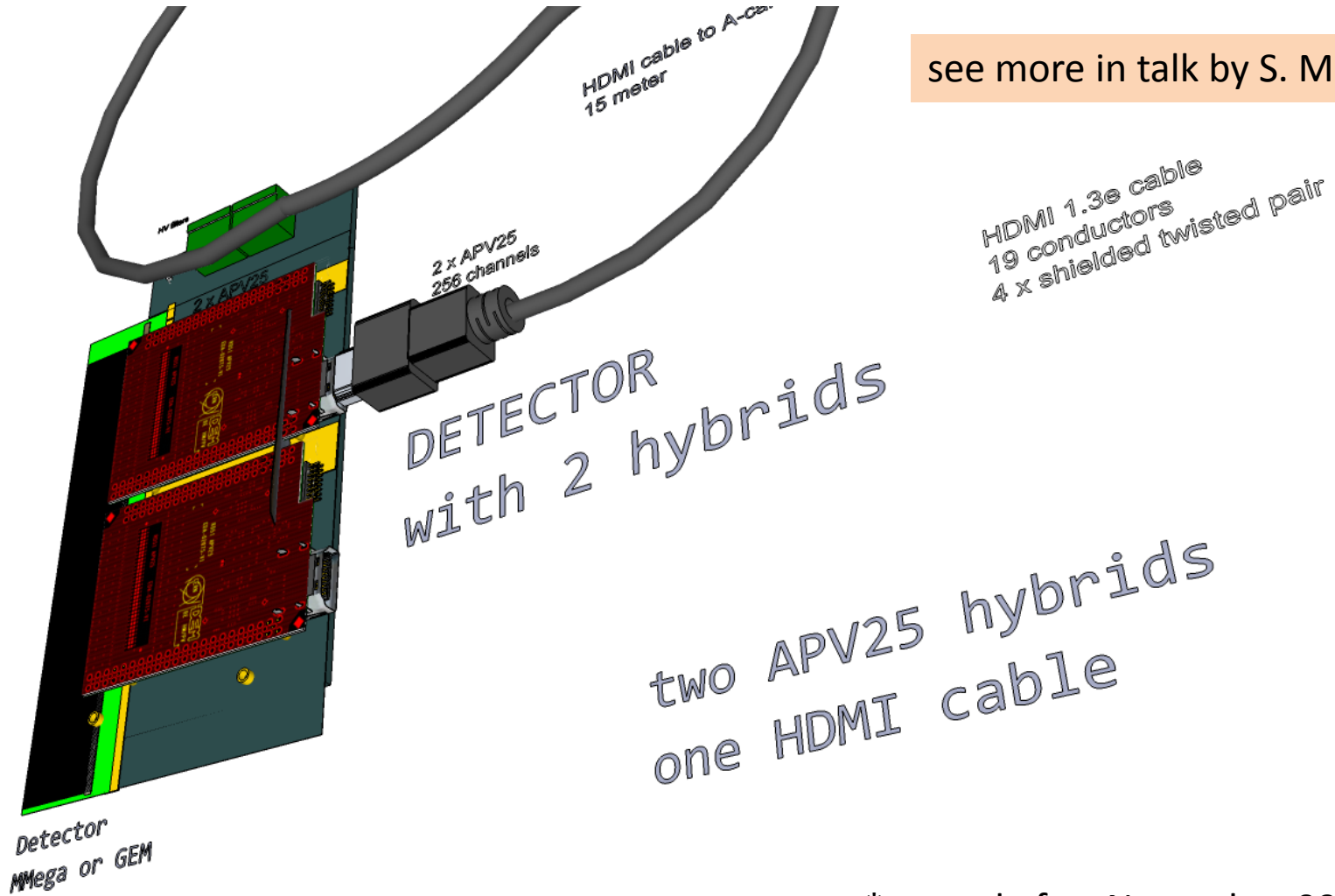
# SRS Overview

Scalable Readout System  
Status Feb. 2010



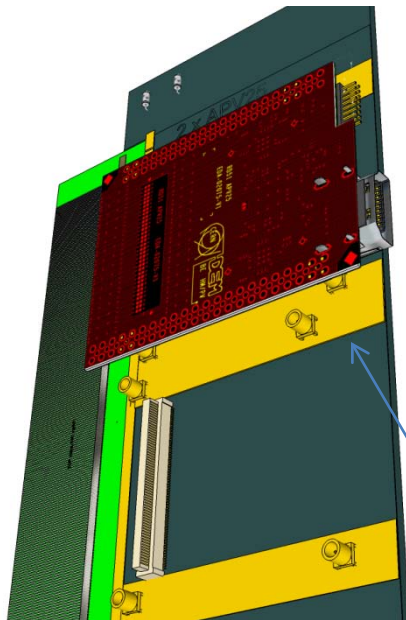
# Hybrid chip design\*

see more in talk by S. Martoiu

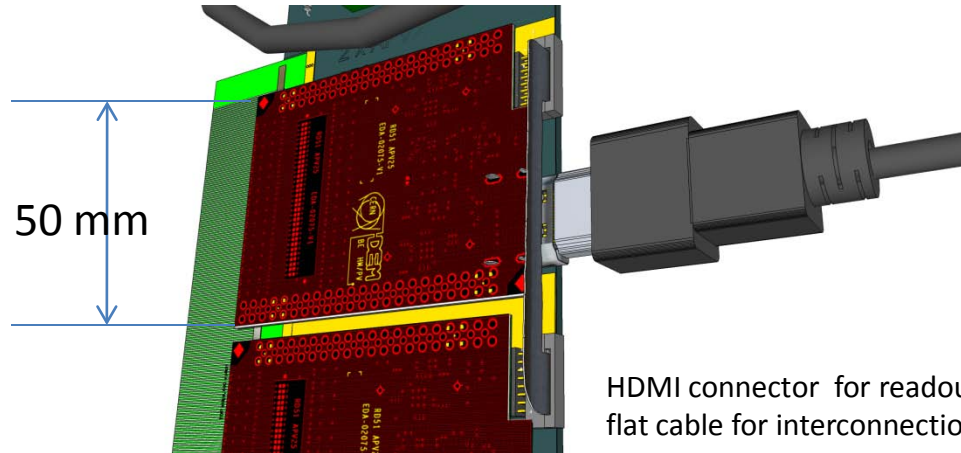


\*started after November 09 meeting

# Hybrid mounting details



Chamber Ground



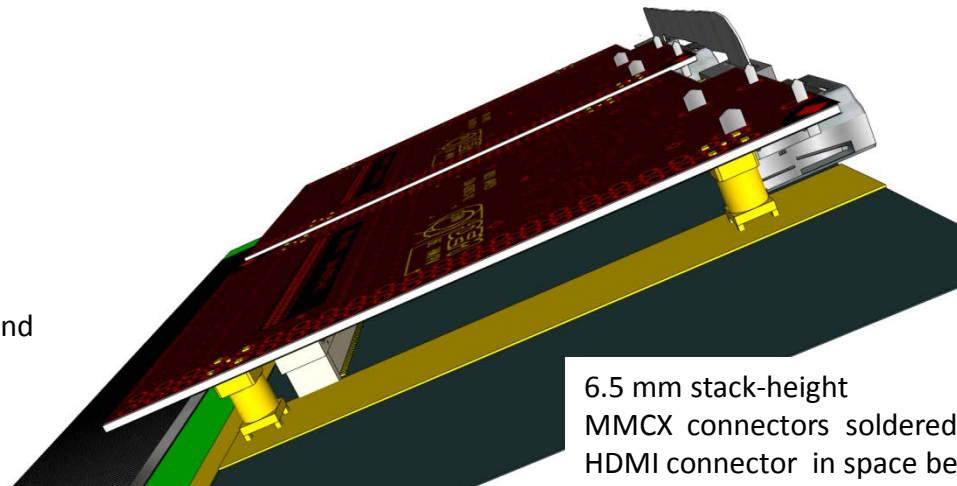
50 mm

HDMI connector for readout cable  
flat cable for interconnection of 2 hybrids

## one hybrid removed:

Residing on MPGD chamber:

- Panasonic 130 pin plug for signals
- Samtec MMCx for low -imp. Ground



6.5 mm stack-height  
MMCX connectors soldered on Chamber GND  
HDMI connector in space between chamber and hybrid

# RD51 standard connectors

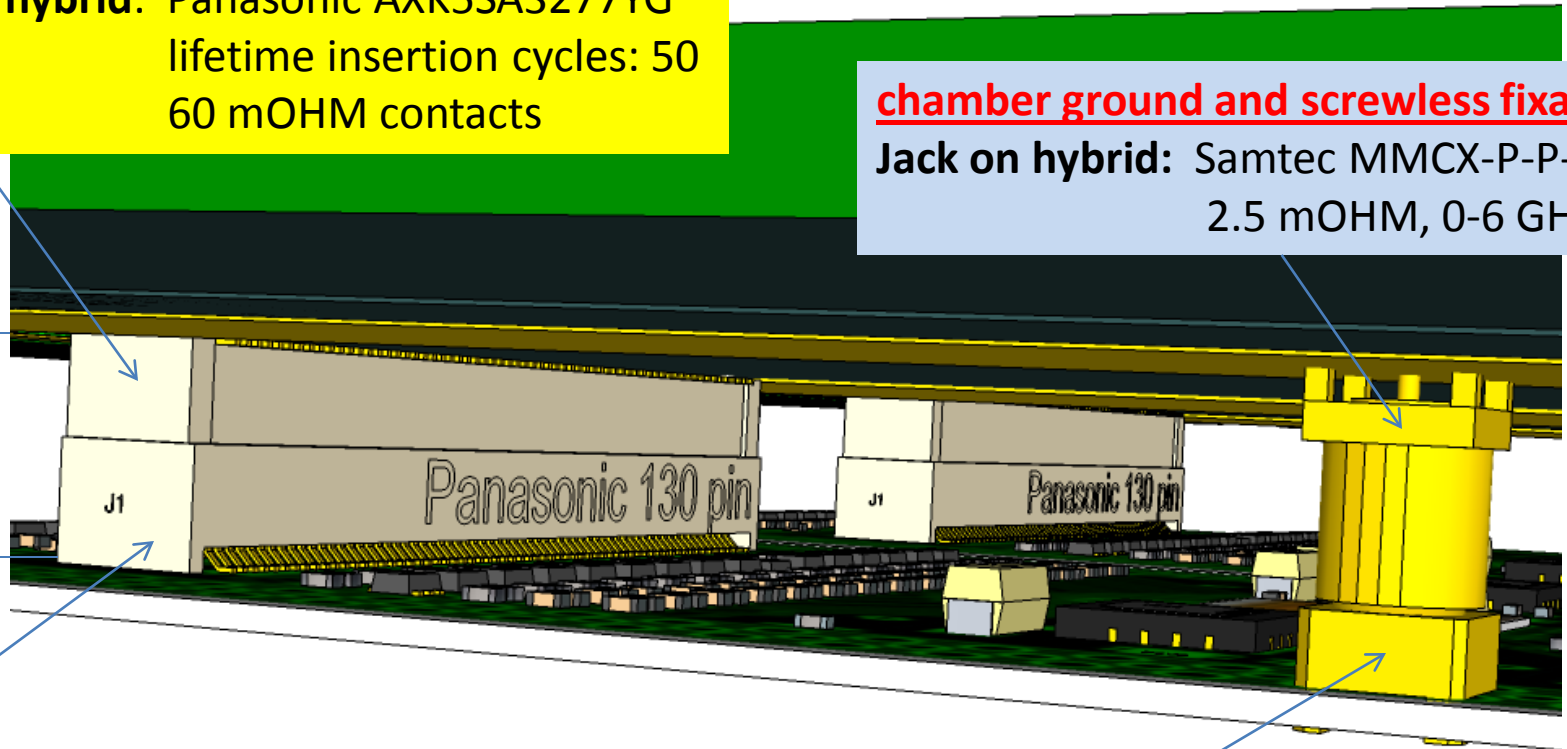
## Signals

**socket on hybrid:** Panasonic AXK5SA3277YG  
lifetime insertion cycles: 50  
60 mOHM contacts

## chamber ground and screwless fixation:

**Jack on hybrid:** Samtec MMCX-P-P-H-ST  
2.5 mOHM, 0-6 GHz

6.5 mm

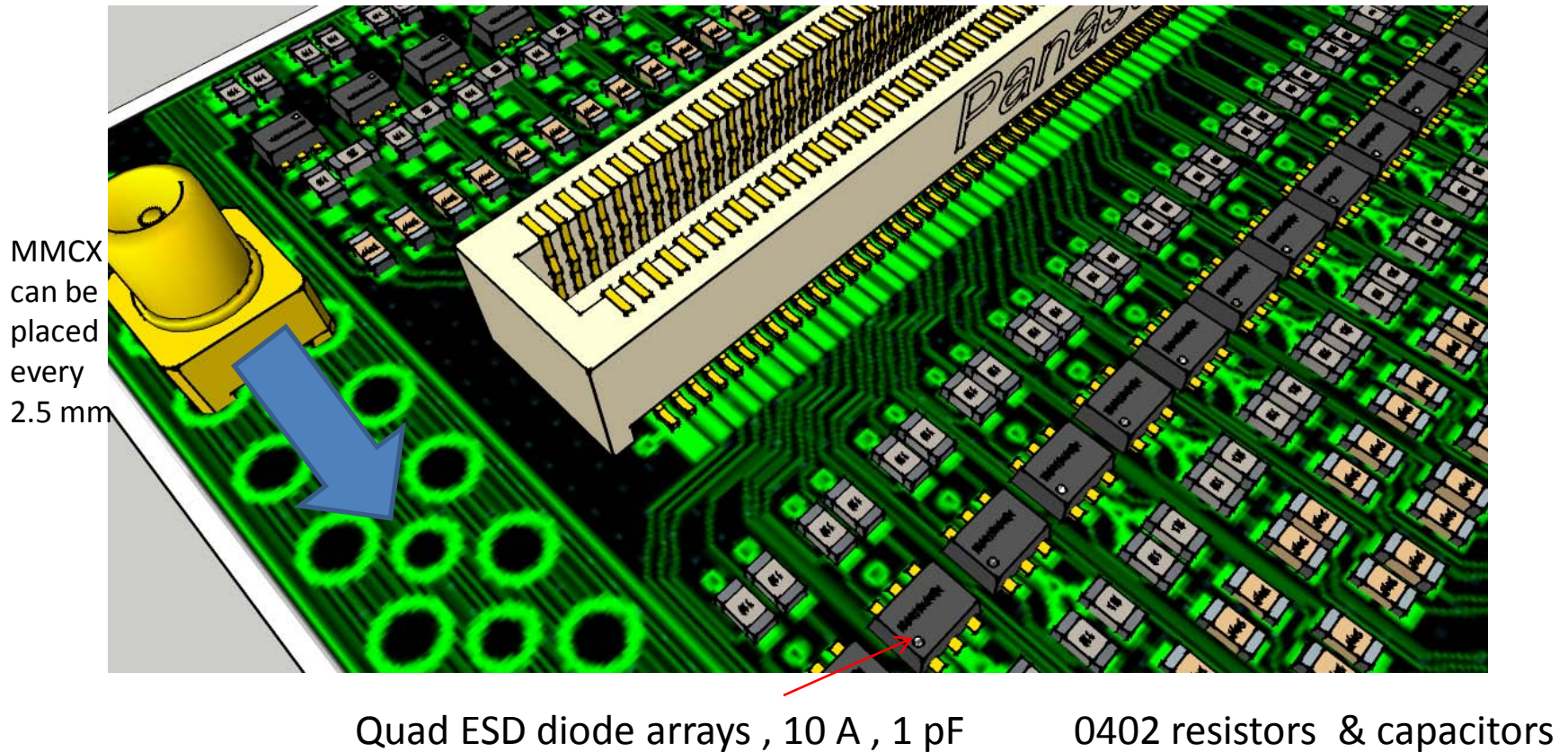


**header on chamber:** Panasonic AXK6SA3677YG

**Plug on chamber:** Samtec MMCX-J-P-H-ST

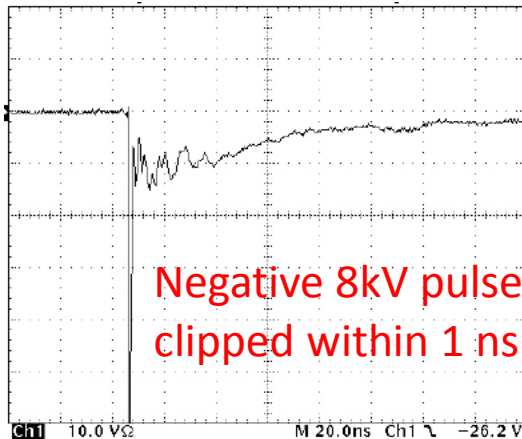


# Some Details



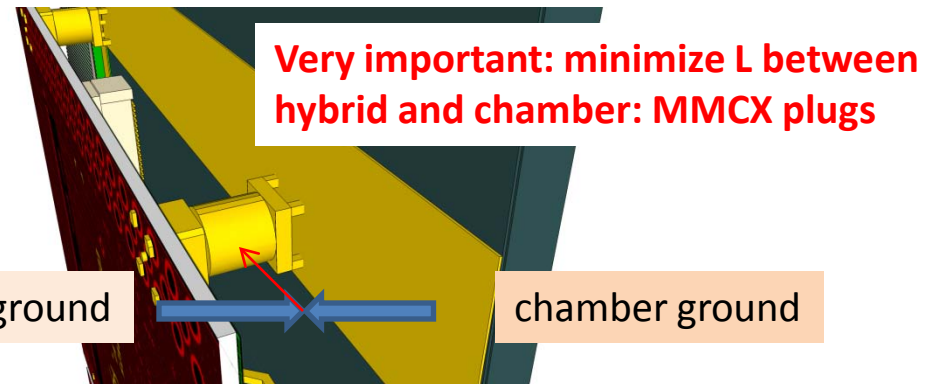
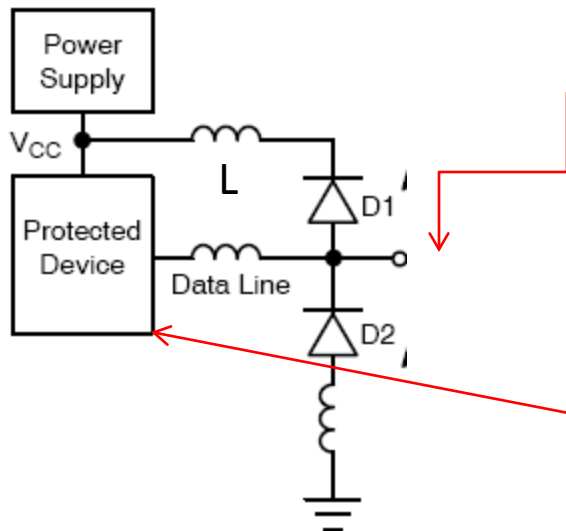
# NUP4114UPXV6

## quad ESD diodes: < 1 pF



IEC 61000-4-2 Spec.

Level	Test Voltage (kV)	First Peak Current (A)	Current at 30 ns (A)	Current at 60 ns (A)
1	2	7.5	4	2
2	4	15	8	4
3	6	22.5	12	6
4	8	30	16	8



Negative clipped:  $V_n = -V_f - L \times \frac{di_{esd}}{dt}$

Positive clipped:  $V_p = V_{cc} + V_f + L \times \frac{di_{esd}}{dt}$

# Hybrid extension cable

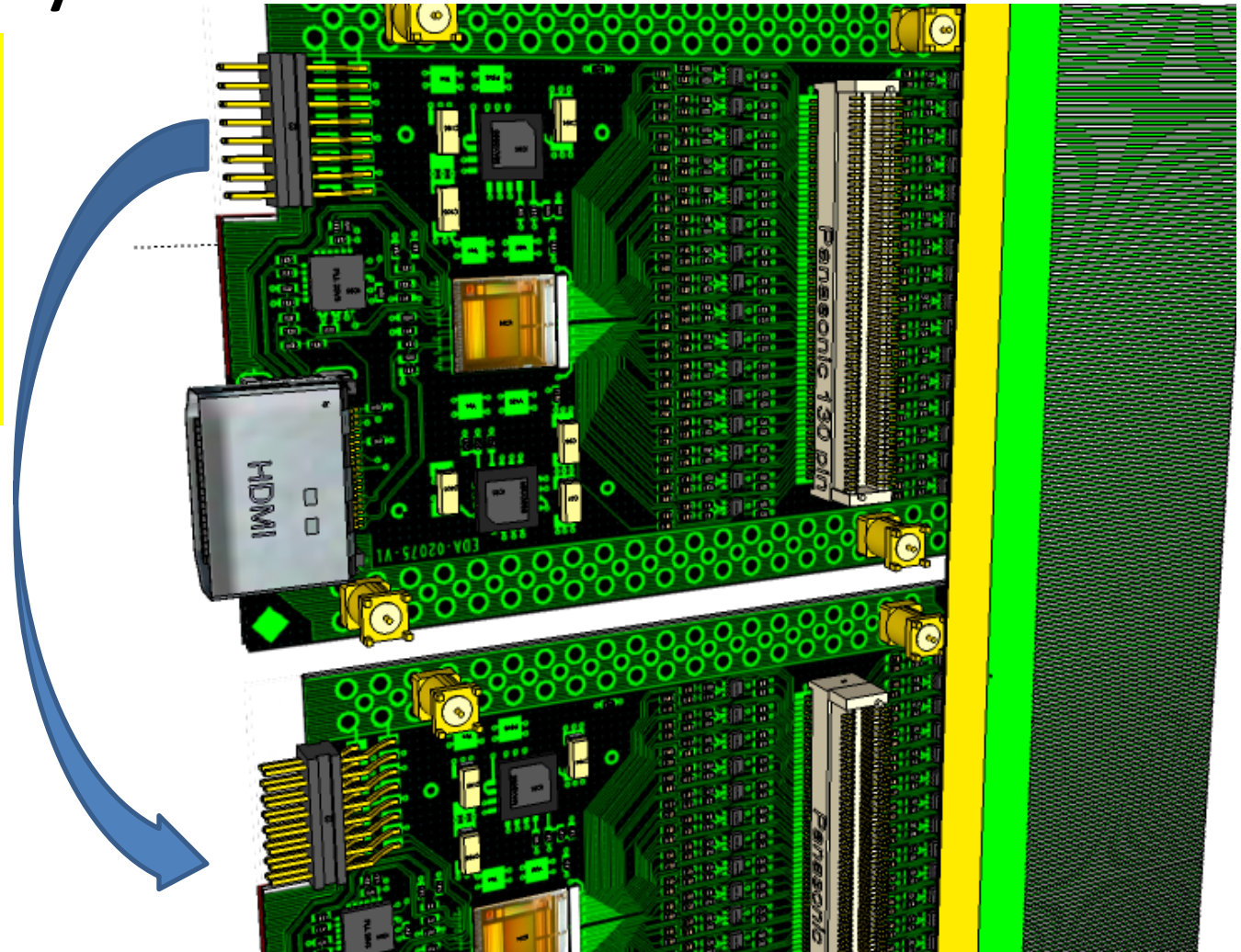
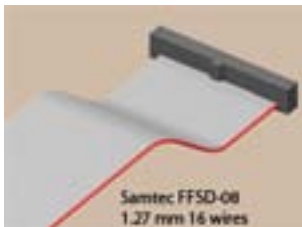
## 2 hybrids = 1 HDMI cable

### Extension connector:

Samtec 16 pin, 1.27 mm  
FTSH-180-1-L-D-DH

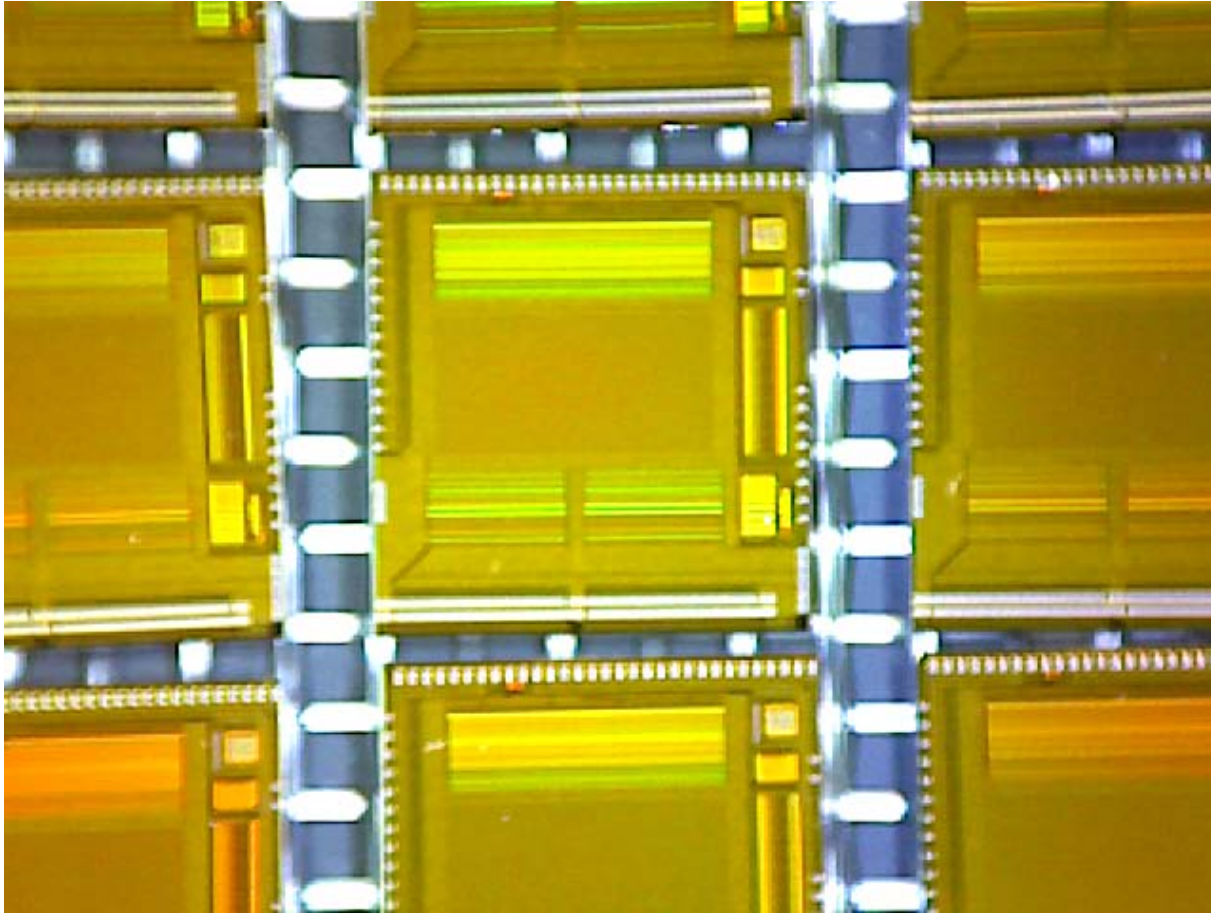
### Extension flat cable

Samtec 3 inch long  
FFSD-08-D-3.0-01-N



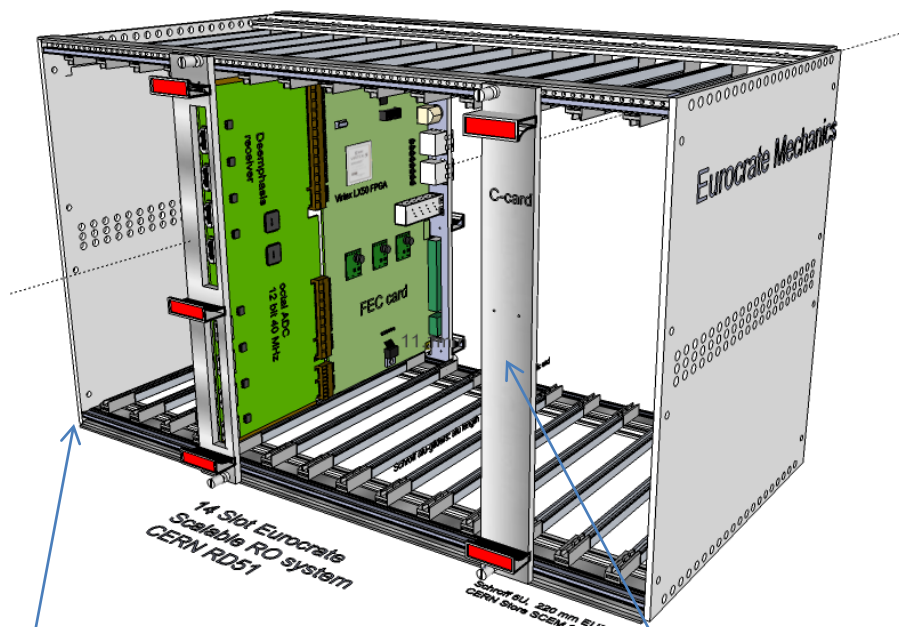


# APV25-S1 chips



For first systems, RD51 purchased 100 chips (to be bonded on hybrids)

# Europa chassis SRS

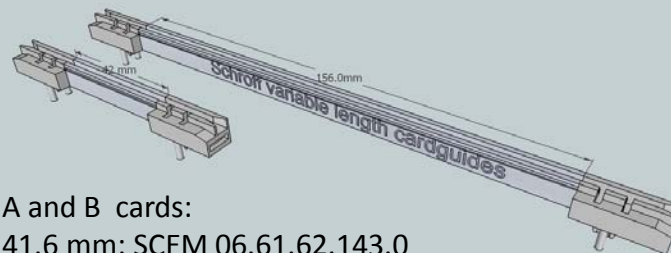


**Chassis:** 6U x 220 mm, Schroff  
CERN SCEN 06.61.61.045.7

## C-cards and FEC cards:

Front panel set 6U-6TE with fixations:  
CERN SCEN 06.61.63.156.3

Card guides for SRS now in CERN store:

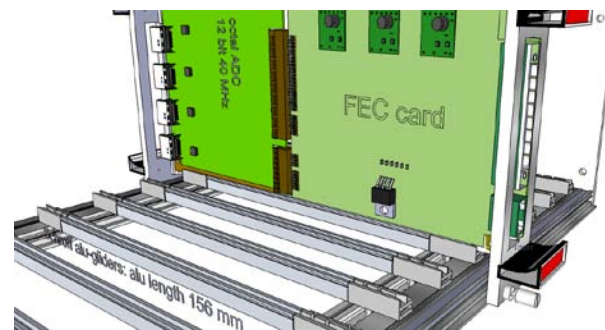


A and B cards:

41.6 mm: SCEN 06.61.62.143.0

C-cards only:

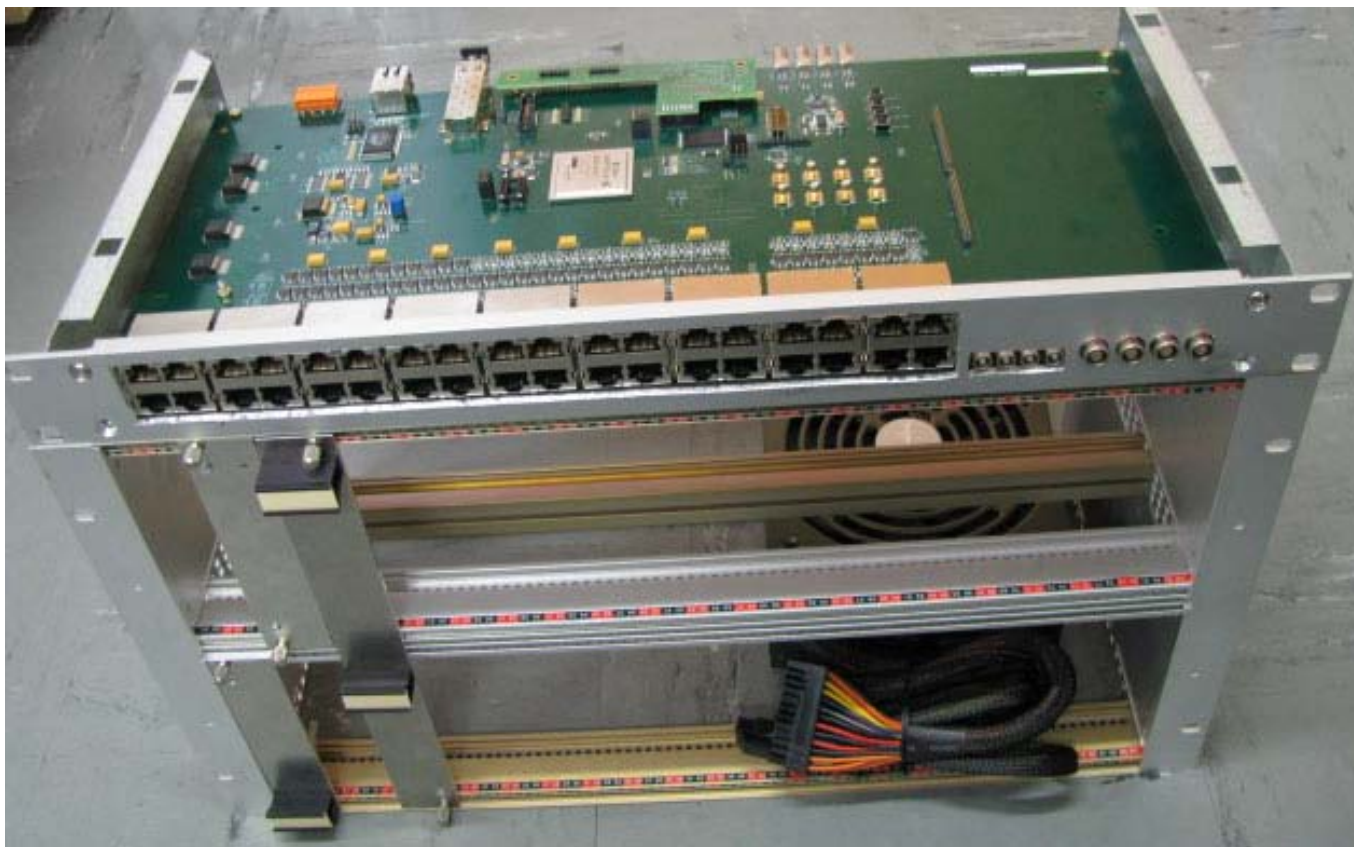
155.6 mm: SCEN 06.61.62.143.1



## A-cards and B-cards

Front panel set 3U-6TE with fixations:  
CERN SCEN 06.61.63.056.6

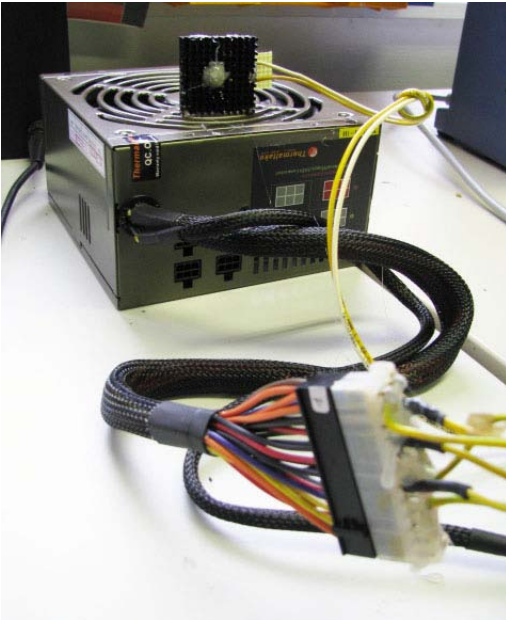
# 19" crate environment



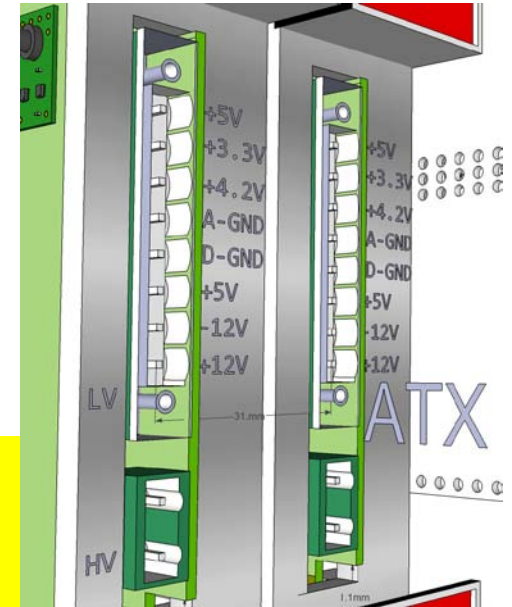
Mechanical work, panels, material procurements and testing to be organized



# ATX Power !

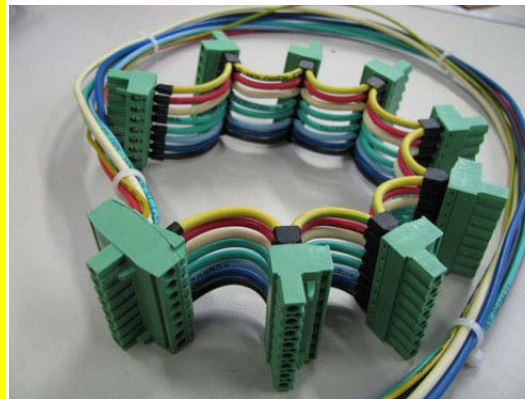


**24 pin Molex Mini-Fit Jr**  
**part No. 44206-0007**  
to connect power chain of FEC cards



We use standard **ATX Rev 2.2**  
**500 Watt , power packs**

+3.3V = 20 A  
+5V = 15 A  
(+12V = 18 A)  
-12 V = 0.3 A



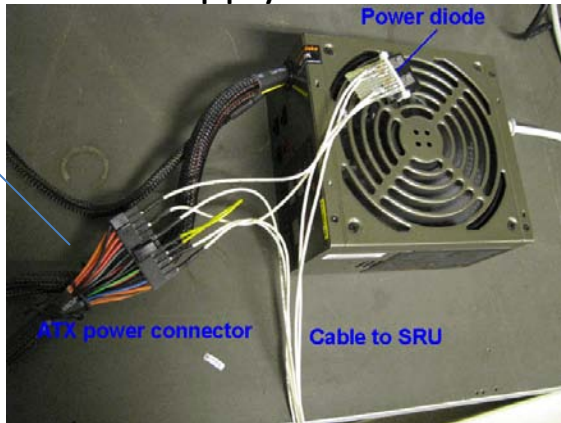
## **FEC card Power chain:**

each FEC card:  
Phoenix plug 1757077  
last FEC card and cable to ATX:  
Phoenix TMSTB 2,5/8-STF-5.08  
Cables: 1.5 mm<sup>2</sup> coded color

# Power interface

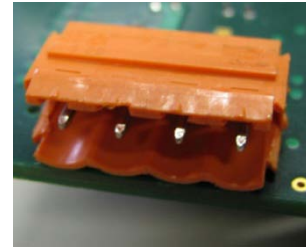
we still need to design a common power interface  
so far case-to-case cabling

ATX supply 450 Watt



SRU connector

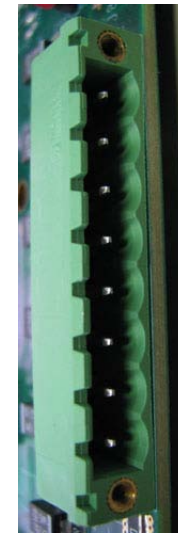
Weidmuller 1958280000



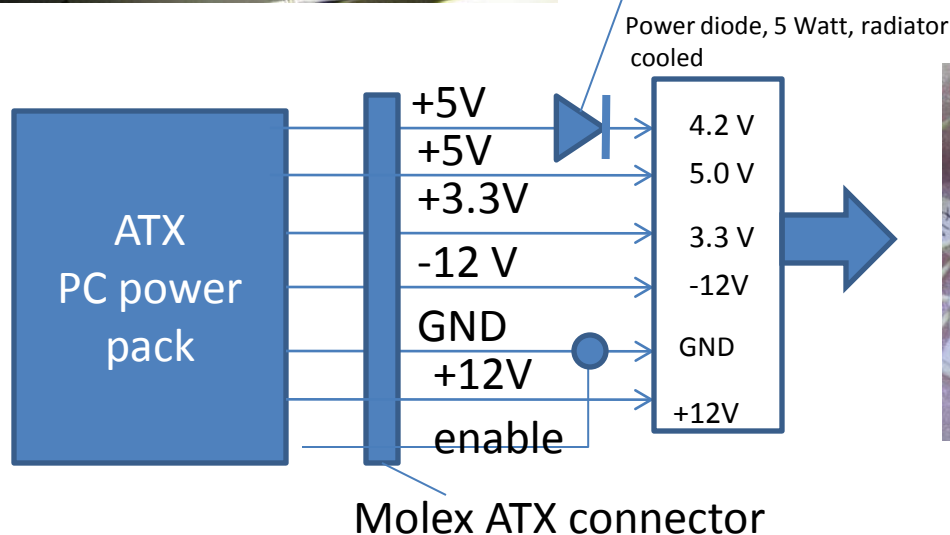
GND +4V2 -12V +3V3

FEC card connector:

Phoenix MSTB 2,5/8-GF-5,08



+5V  
+3V3  
+4.2  
A-GND  
D-GND  
+5V  
-12V  
+12V



Faston cable patch

ATX power interface

..to be designed...  
-5 Watt cooled diode  
-add Fuses !  
-connector for FEC  
-connector for SRU  
--fixation

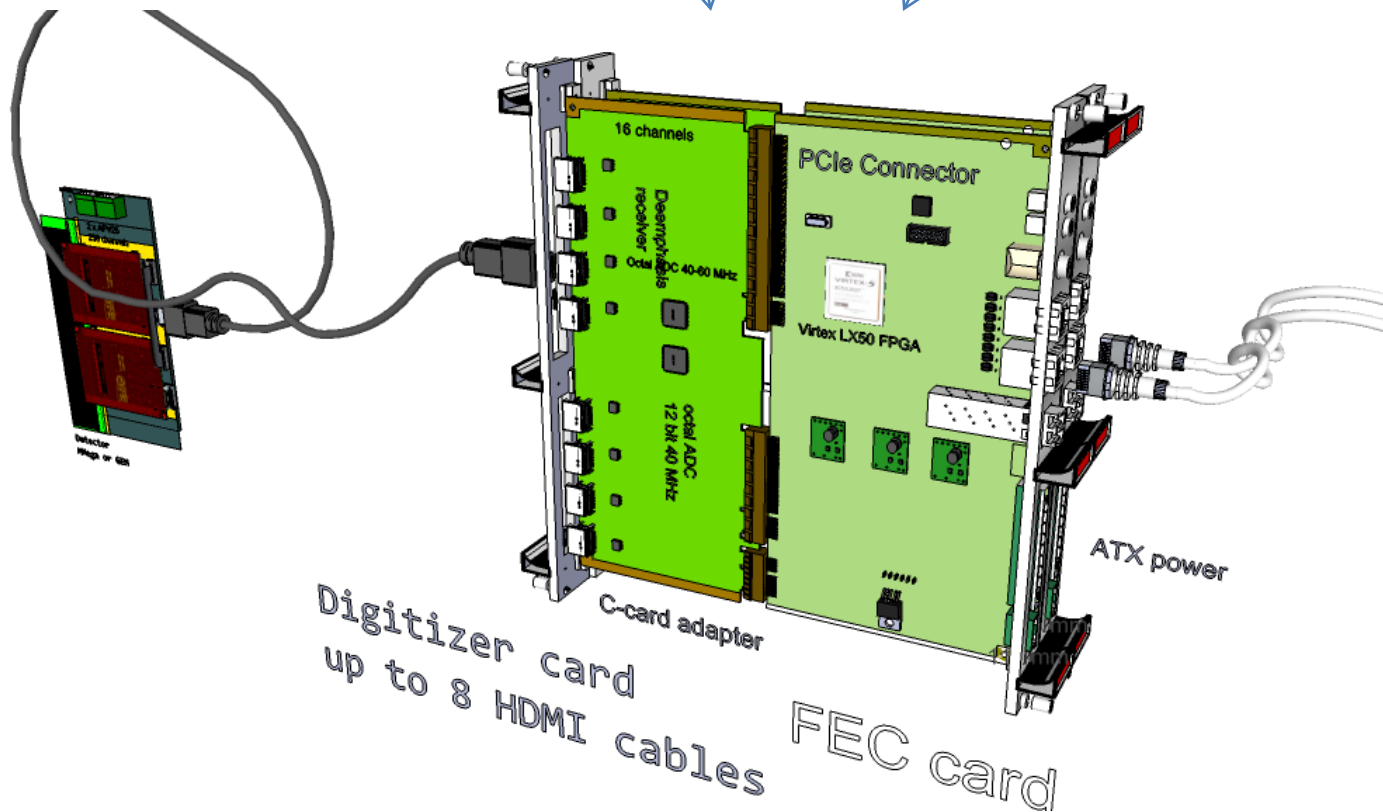


# Digitizer and FEC cards

also great progress since November 09 meeting

see talk by S. Martoiu

see talk by J. Toledo

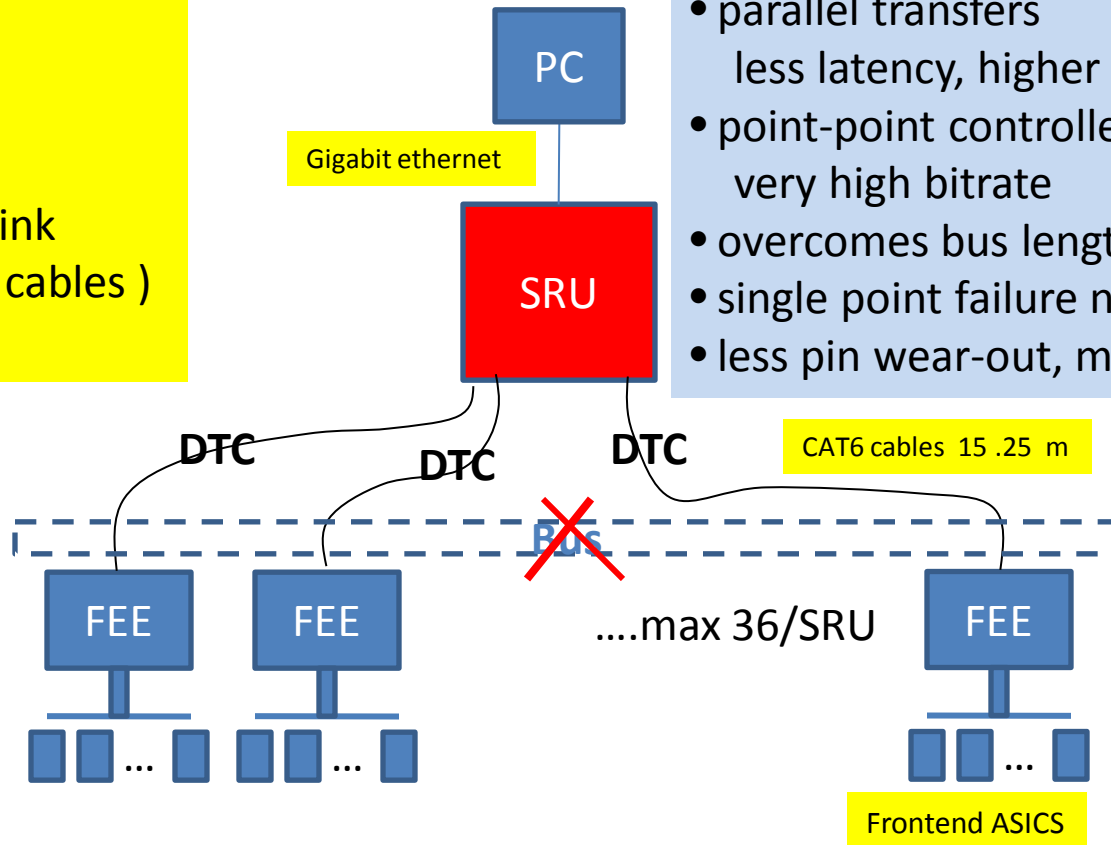


# DTC links

## (buses are obsolete)

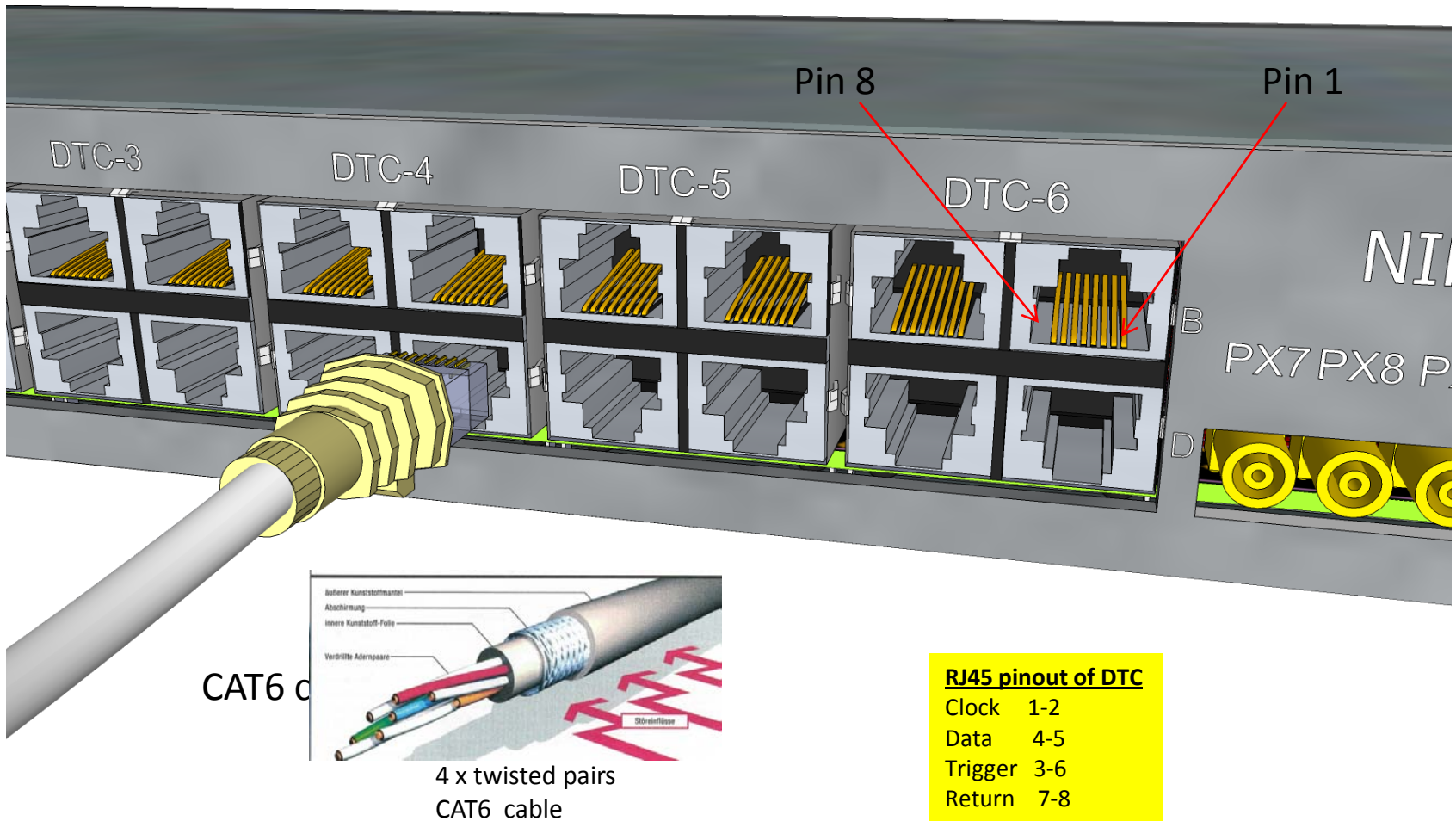
### DTC link

Data  
Trigger  
Control  
via the same link  
(initially CAT6 cables )



- parallel transfers  
less latency, higher bandwidth
- point-point controlled impedance  
very high bitrate
- overcomes bus length limit to SRU
- single point failure not fatal
- less pin wear-out, more cost effective

# DTC link pinout: 2-in 2-out



# DTC link protocol

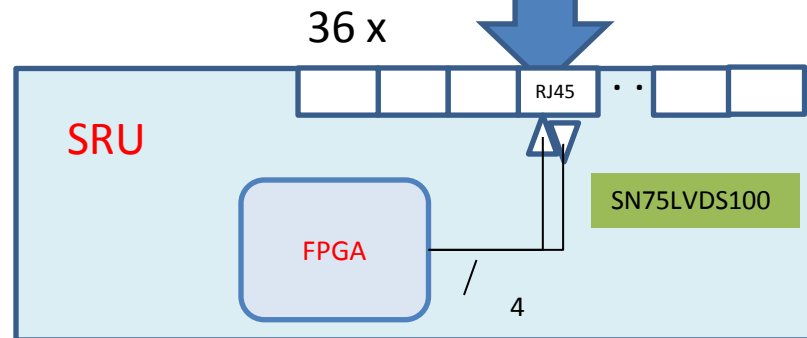
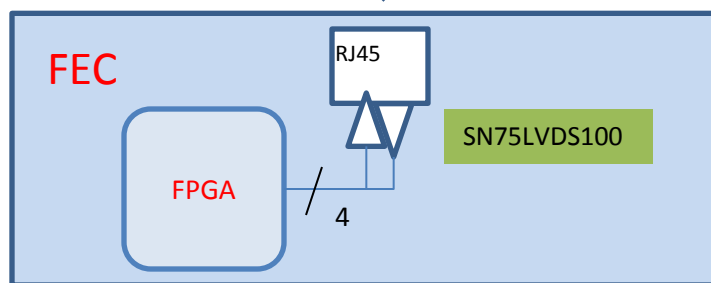
➔ revised DTC protocol by Fan Zhang , CCNU Wuhan:

Constant SRU clock. Coded trigger and Control for dynamic actions.

Assume SRU clock 240 MHz: Input stream from 36 FEC's @ 200 Mbit/s = 8.6 Gbit/s

Clock ← DTC\_CLK clock to FEC      pin 1-2  
 Data → DTC\_DATA data from FEC      pin 4-5  
 Select ← DTC\_TRIG coded trigger to FEC      pin 3-6  
 Return → DTC\_RETURN status or local trigger      pin 7-8

buffered , terminated LVDS signalling over 15-25 m CAT6



## Control mode:

- DTC\_CLK to FEC
- DTC\_DATA = Serial data or ACK to SRU
- DTC\_TRIG = Serial data or ACK to FEE
- DTC\_RETURN = Coded status to SRU (Ready or Error ~)

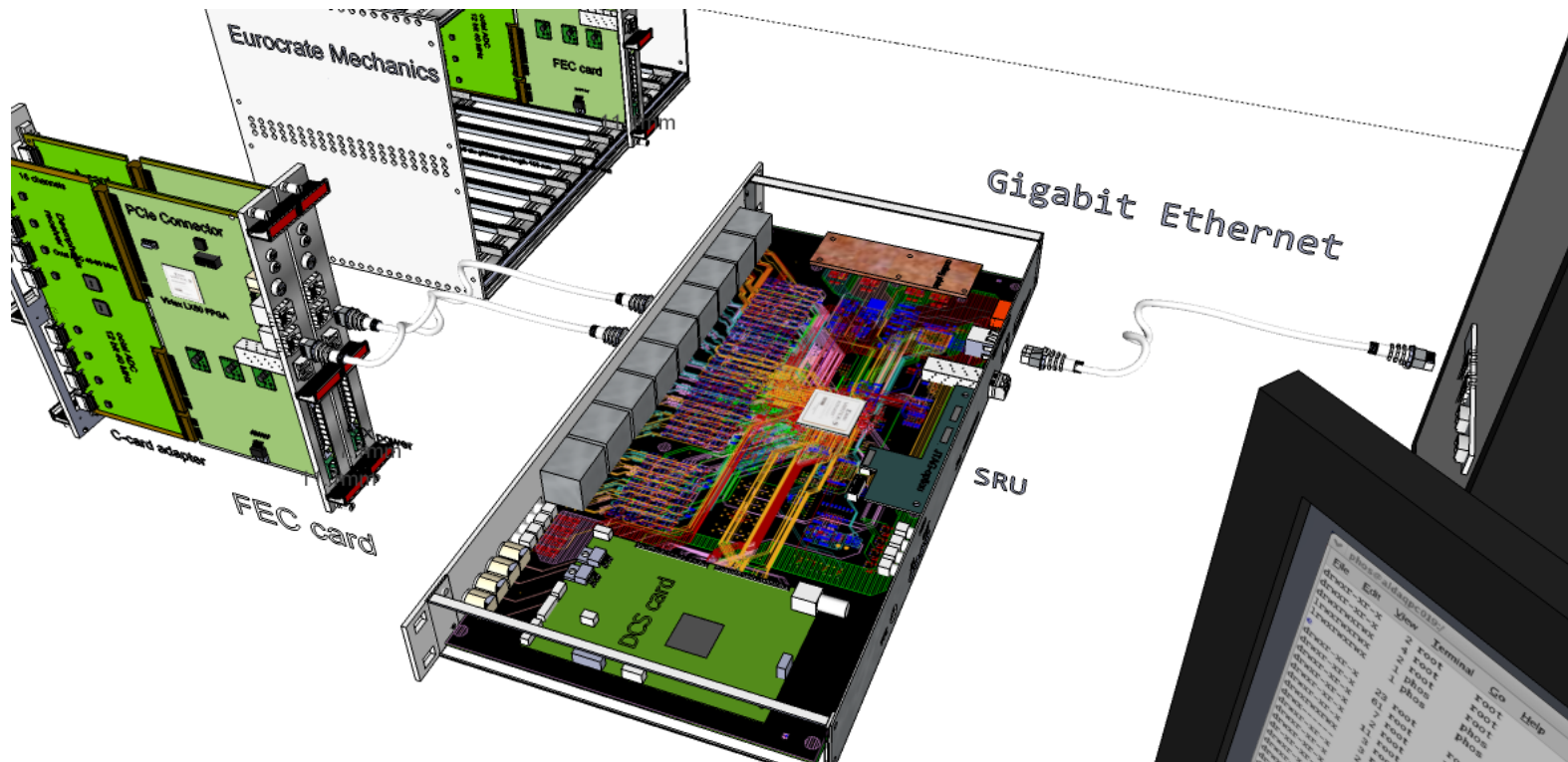
- Note: for disabling a defective FEC card (bad FPGA) we need a unique code : stop CLK at high level, clock trigger line.

## Mode detection : detect DTC TRIG pulse

- If (Widths of DTC\_TRIG pulse, number of  $T_{DTC\_CLK}$ )
  - 2 : Level-0 trigger
  - 4 : Level-1 trigger
  - 6 : Level-2 trigger = Readout command
  - 8 : Control operation follows
  - >=9 : Error

# SRU – Readout Unit

- parallel readout of FEC via DTC links
- 10 Gigabit target performance via Ethernet to DATE computer equipped with 10 GBE port(s)
  - user defined readout trigger inputs, TTC optical link option
- slow controls via ALICE DCS card , or via software on DAQ computer





# SRU panel functions

DTC links  
36 x



FRONTSIDE

NIM and LVDS signals for  
user-defined trigger , timing or clock combinations ( FPGA code)

BACKSIDE



DCS card Ethernet

TTC fiber input

NIM inputs

Differential JTAG via  
cable form JTAG master

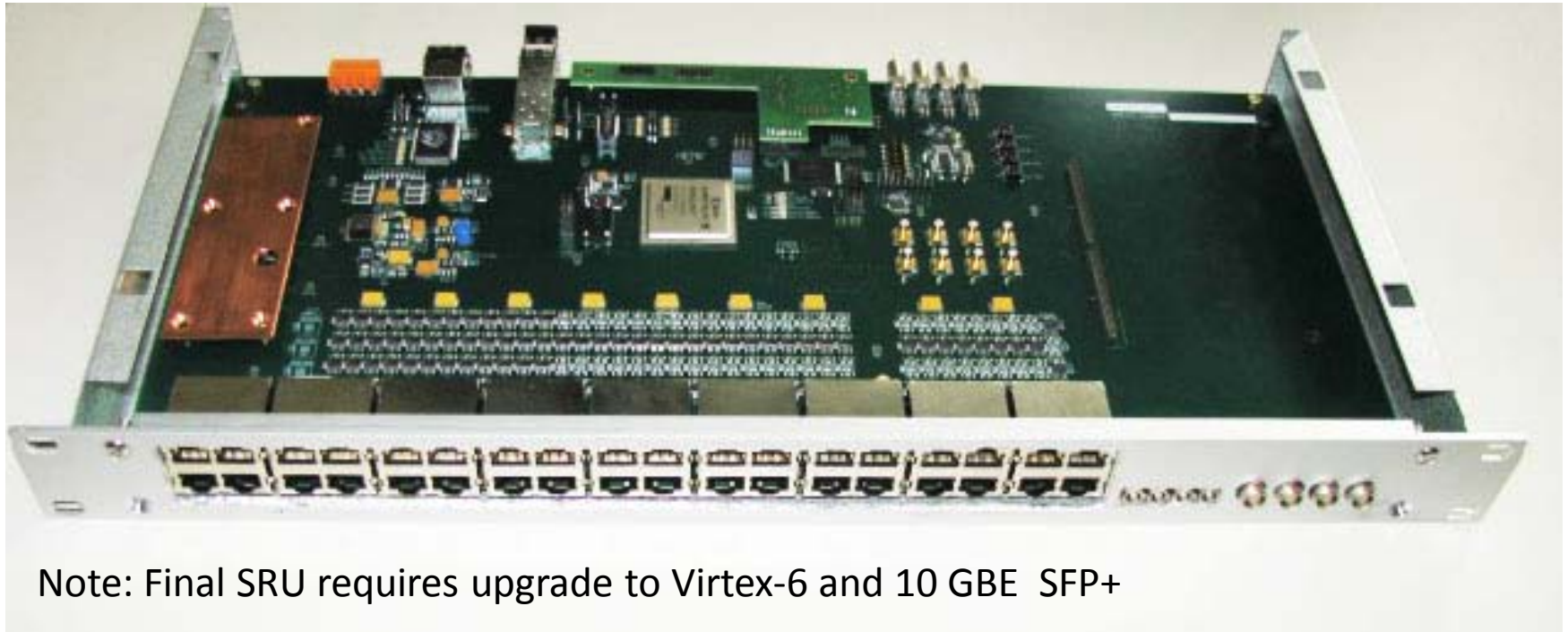
GBE copper  
and optical

Power from ATX

# SRU photo

First 4 SRU boards arrived last Wednesday, 18 Feb 2010.

After solving minor problems , FPGA and Flash programming works, tests are ongoing  
Some missing components delay the availability of next 2 SRU boards\*



Note: Final SRU requires upgrade to Virtex-6 and 10 GBE SFP+

\*Mouser parts did not get delivered due to unpaid CERN bills !!

# SRU testing.. ongoing



Status 23 Feb 2010  
( Fan Zhang & Alfonso Tarazona)

- Power via ATX =OK
- Local Voltages = OK
- Cooling =OK
- System Clocks =OK
- JTAG programming FPGA =OK
- Flash Programming OK
- DCS card booting = OK
- Programmed DCS control of FPGA=OK
- Sending clock to LVDS link =OK  
( see picture)

# Readout via Gigabit Ethernet:

## DATE and Slow Controls

see also talk by Filippo Costa, November 2009, WG5

A new **equipment type for DATE** has been

developed by Filippo Costa of the DATE team that allows to receive data through the Ethernet socket. Data are sent as **UDP Packets with a datagram of 9 kbyte to obtain a throughput of 300 MB/s.**

The input to the DATE computer was a commercial, **dual port 10 GBE Intel card**

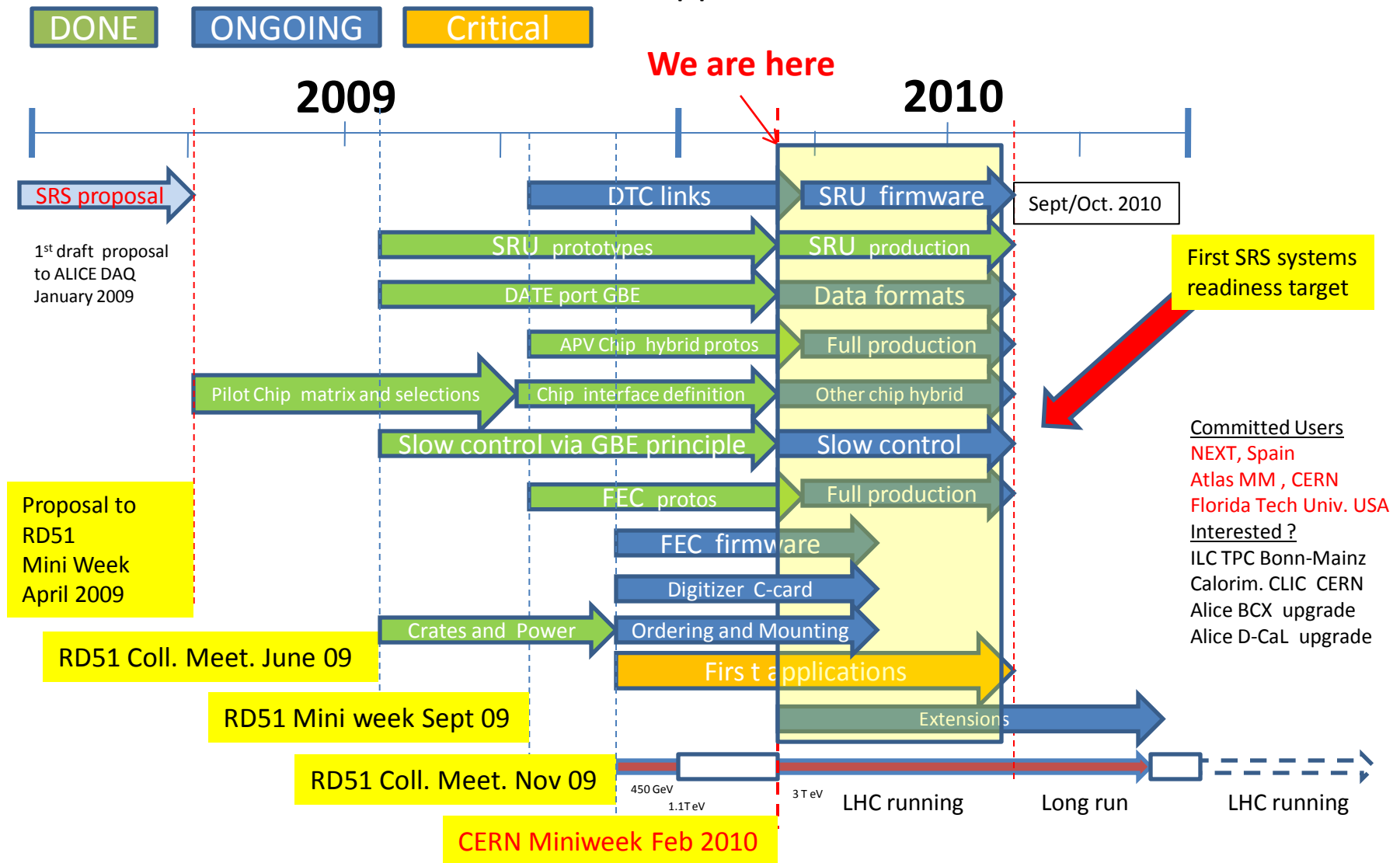
On the SRU side, **Gigabit Ethernet firmware** was developed for the Virtex-5 FPGA with integrated MAC (by Alfonso Tarazona).

It allows for example to send 90 kbyte events over 10 packets.

The **slow controls software** can be run on the same DAQ computer as DATE, it uses **IP ports for each slow controls service with 32 bit read/write control** to all parts of an SRS architecture.

# SRS project timing Feb. 2010

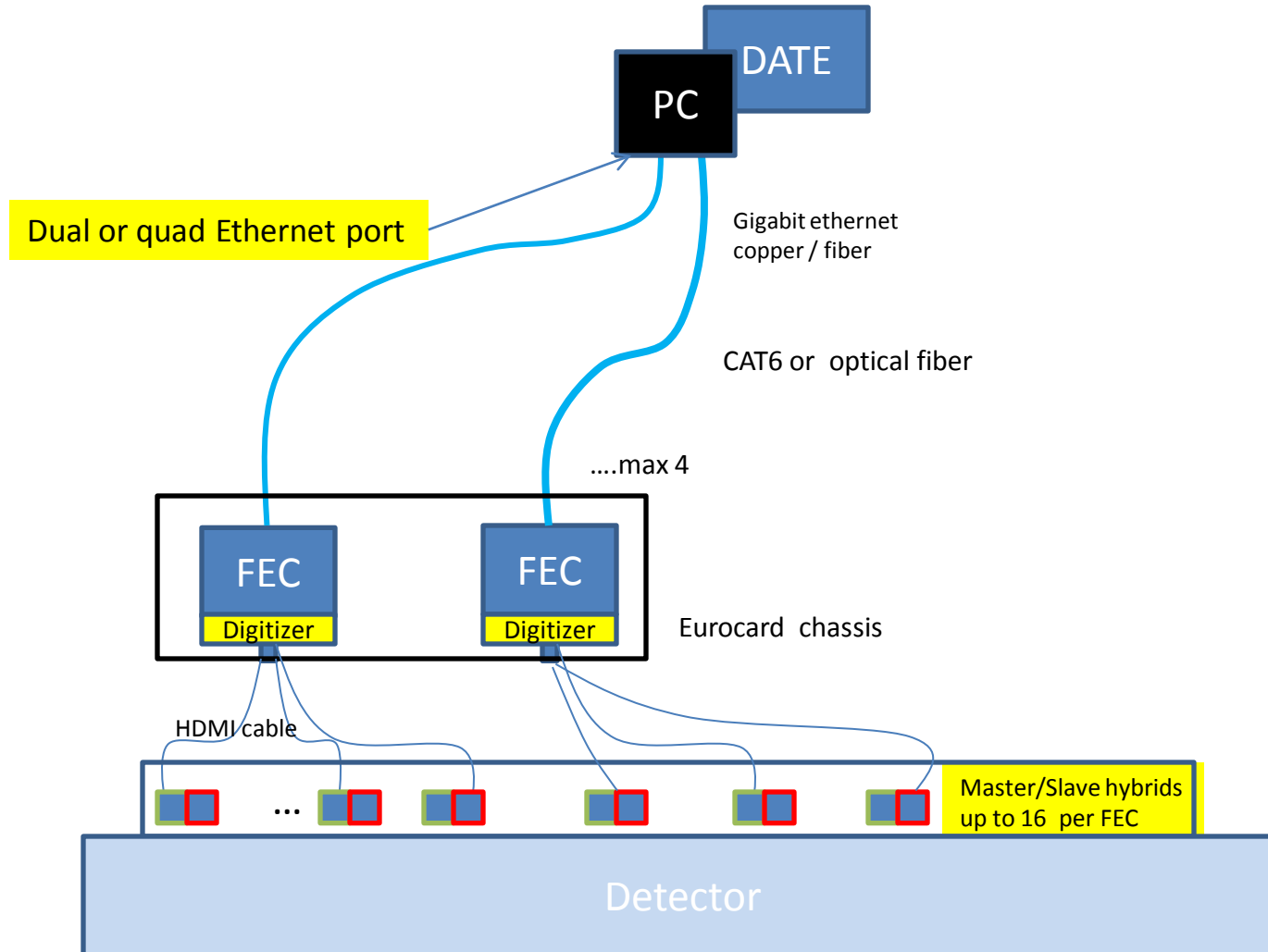
towards first applications in 010





# SRU-less test systems

up to 4 FEC cards **directly** connected to DAQ



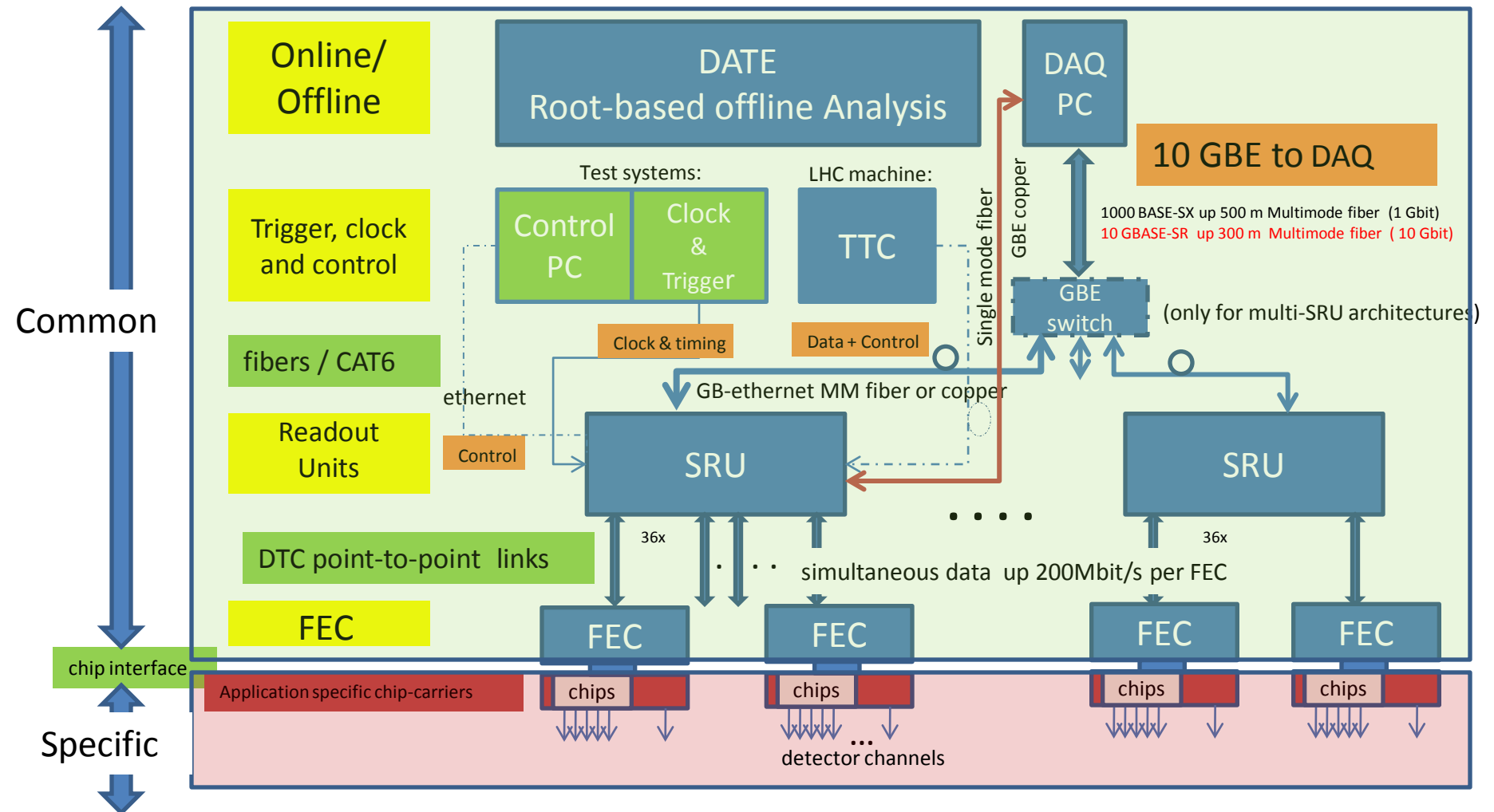
# Summary

Progress since November 09 Collaboration meeting

1. Chip hybrid with APV25 chip is already in prototype production  
Procurements for production of 250 hybrids started
2. Standard connectors for RD51 detectors
3. Spark absorption solution integrated on the hybrid
4. One HDMI cable needed for 2 hybrids ( 256 channels)
5. chip power provided via HDMI cable
6. Digitizer bench-tests looks good  
Allegro layout of Digitizer C-card (8 HDMI cables) imminent
7. Euro-crate mechanics finalized, off the shelf items
8. Power and packaging, procurement etc needs to be organized
9. FEC card design and PCB layout under way at UPV Valencia
10. First SRU boards arrived and are under test
11. First 3 applications committed
12. SRS user group needed for coming important SRS integration issues

# Backup material

# SRS proposal April 2009



# SRS User's Group

## **Chips and hybrids**

The 1<sup>st</sup> RD51 frontend hybrid is based on the APV25 chip with analogue readout, powered by HDMI cables. This subgroup consists of the ones who think of new applications and they should recommend new or different RO chips for more RD51 applications. Related issues are: digital versus analogue readout and trigger or no trigger.



# SRS-UG

## Architectures

- The 1<sup>st</sup> RD51 systems use an external hardware trigger signal to copy chip data into an intermediate event buffer from where formatted events are transmitted via IP packets to the DAQ computer. However SRS can be used for different trigger and readout architectures. This subgroup should therefore address more optimized architectures, like N-level trigger, trigger-less, shared memory, etc

# SRS-UG

## Packaging and Commissioning

The 1<sup>st</sup> SRS applications are based on chip carriers that are connected via long, powered HDMI cables to digitizer/FECs which are housed in a 6Ux220 Euro-chassis and get powered via standard ATX supplies. Up to 36 FEC's are connected via CAT6 network cables to a single Scalable Readout Unit (SRU). The D.T.C. link protocol between FECs and SRU consists of two phases: 1.) Data & Trigger 2.) Controls. The SRU is mastered by control and DAQ software running on the DAQ computer(s) and the Trigger signals are to be provided to LVDS or NIM inputs on the SRU.

Users of the pilot SRS applications should participate in setting up a first template for reproducing SRS systems. This includes component procurement, packaging, powering, connectivity, reliability and qualification test procedures.

# SRS-UG

## **Slow Controls**

The slow controls is a tree of addresses that are mastered by the controls software on the DAQ computer. Each controls branch is associated with a dedicated port which controls a group of Ethernet addresses. The control targets are local read-write addresses which implemented in the hardware units, like SRU, FEC, Digitizer or Extension card, Chips. The intermediate transport of control data is transparent to the user and to be handled by the card resident firmware. The mapping between physical addresses and logical addresses inside each port is based on a configuration file. Some configuration files are static, like for SRU or FEC. Others depend on the choices taken, in particular choice of the readout chip. This subgroup should provide the first basic configuration files as templates for future users.

# SRS-UG

## Triggering

- The 1<sup>st</sup> SRS applications work with a precisely timed trigger signal that is provided by external trigger logic to one of the signal inputs of the SRU, or directly to the corresponding FEC card input. This trigger signal initiates event-synchronized transfer of data from the frontend chip to the FEC card buffer and defines an event number to associated with the chip data. In principle it is possible to allow for a second-level trigger signal to arrive at some latency after the first level. A second level signal allows to enable or discard transfer of accumulated events that can be processed at the FEC buffer level. In case of a single level trigger, all data received from the readout chips get transferred to the DAQ computer. A second level trigger allows for online processing and discarding of (empty) events. The choice depends on the bandwidth limit into the DAQ computer which is targeted as 10 Gbit/s per SRU ( but only 1 Gbit/s for the first SRU prototypes in 2010). This subgroup should work on dataflow and bandwidth with simulations based on measured SRS parameters.

# SRS-UG

## Data formats

The event data that are received from frontend chips must be uniquely and safely formatted before being wrapped in IP systems. Initially, we should “lend” a format from some detector that uses DATE for readout. This subgroup should however identify a common SRS data format that works with all packets that are transmitted and unpacked in a destination buffer on the DAQ computer. Ideally all data belonging to the same event-number should get routed and unpacked into a the same destination buffer (implicit event-building). In order to get first applications bootstrapped the first SRS systems will use a format that already exists. The APV data will be digitized into event blocks of 12 bit samples, preceeded by a header with wordcount, timestamp etc . However in order to support different chips for the final system, SRS needs a suitable format that can be transmitted over IP packets without overhead penalty, hence it should include Multi-event packing for small payloads a la LHCb. Further it would be very desirable that data include a data type identifier in their header such that the unpacker software can automatically switch to the correct unpacker mode ( the alternative is to have 1 unpacker code per chip and per detector) This subgroup should consist of persons having online and offline experience in experiments and recommend a Data format that eventually allows to combine different detectors and different chips without changing the unpacker.

# SRS-WG

## Data Acquisition and offline

- The default Data Acquisition system for SRS is the ALICE DATE software <http://ph-dep-aid.web.cern.ch/ph-dep-aid/> over Gigabit Ethernet. As presented in previous WG5 meetings, the porting of DATE to the SRS is well advanced. The use of DATE by RD51 is free however requires to sign and comply to the MoU rules of the Alice DAQ team. DATE works with raw and with Root file formats, the latter being normally preferred for offline data evaluation based on standard methods. The DATE control panel is easy to handle and to learn also by non software experts. The stability of DATE has proven to be excellent and does not require an on call expert, hence users of SRS with DATE profit from a stable software environment. In the simplest case, detectors up to 10K channels require no SRU . Up to 4 FEC cards can get directly connected to 4 GBE Ethernet plugs of a the DATE computer. Systems up to 50 k channels can use a single server PC if one SRU is used to connect up to 36 FEC cards, however the CPU load situation may call for the use of several PC's like it is the case in the ALICE experiment. This subgroup should be composed of both online and offline experts that are concerned about SRS applications, but also of future users and shifters



# SRS-UG

## Firmware algorithms

The programmable hardware (Virtex-5 FPGA) in each FEC card consists of both system-defined and user-defined modules, written by firmware developers, i.e. typically students with VHDL or Verilog expertise. In the simplest case, the chip data assembled in an event buffer of the FEC is merely formatted by a header and shipped to the DATE computer. However if online processing ( peak amplitude, pedestal averaging/ subtraction etc ) is needed, a user-defined firmware algorithm is needed. This algorithm must comply with the allowed trigger latency. Before embarking however on such algorithms, one should carefully trade off available bandwidth and CPU power against hardware algorithms. If enough bandwidth and CPU is available, it is preferable to transfer the data to the DAQ computer(s) and perform the algorithms there. Zero-suppression algorithms are user-defined firmware that depend on the readout chip. Once developed for one particular chip, it can and should be shared with all Rd51 users of the SRS. Other parts of the firmware are serial line protocol conversions like I2C or SPI, JTAG etc. This subgroup should consist of a mix of physicists, hardware and software engineers in order to decide which algorithms are needed and to write the proper Firmware code.