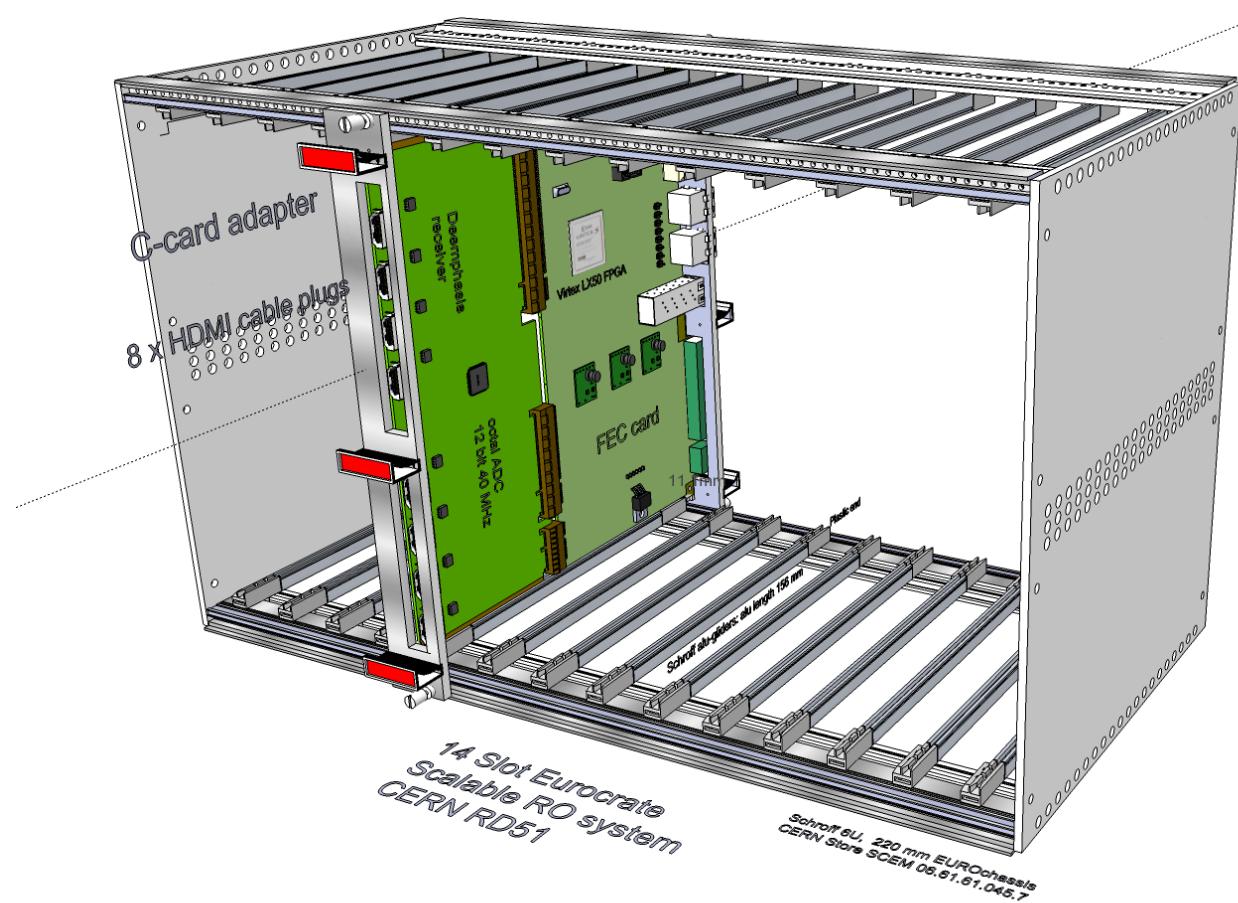


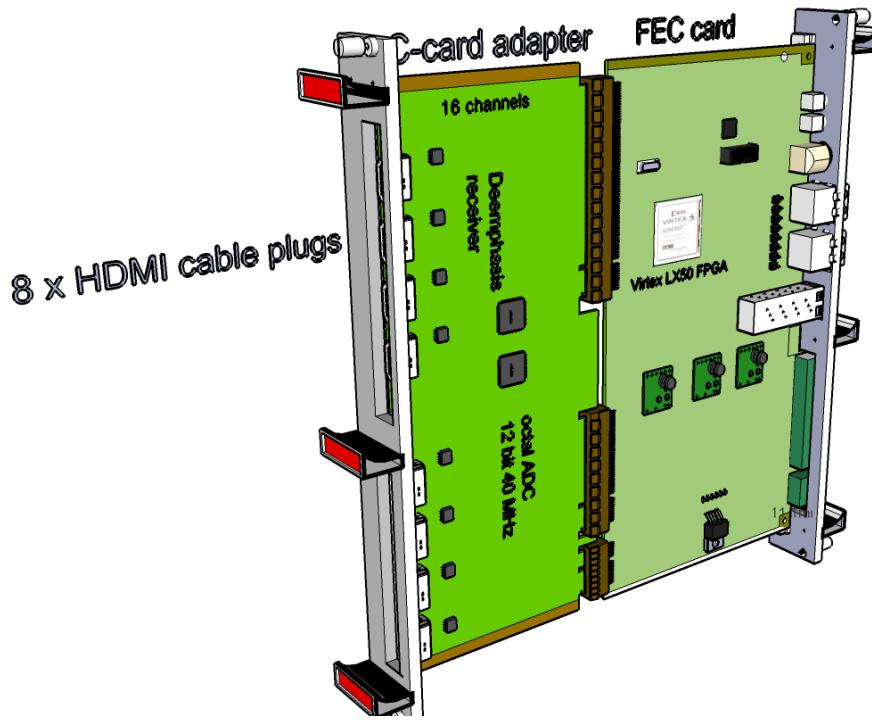
Digitizer Card in SRS “C-format”

Sorin Martoiu, CERN PH/DT

Scalable Readout System



ADC C-Card



ADC C-Card:

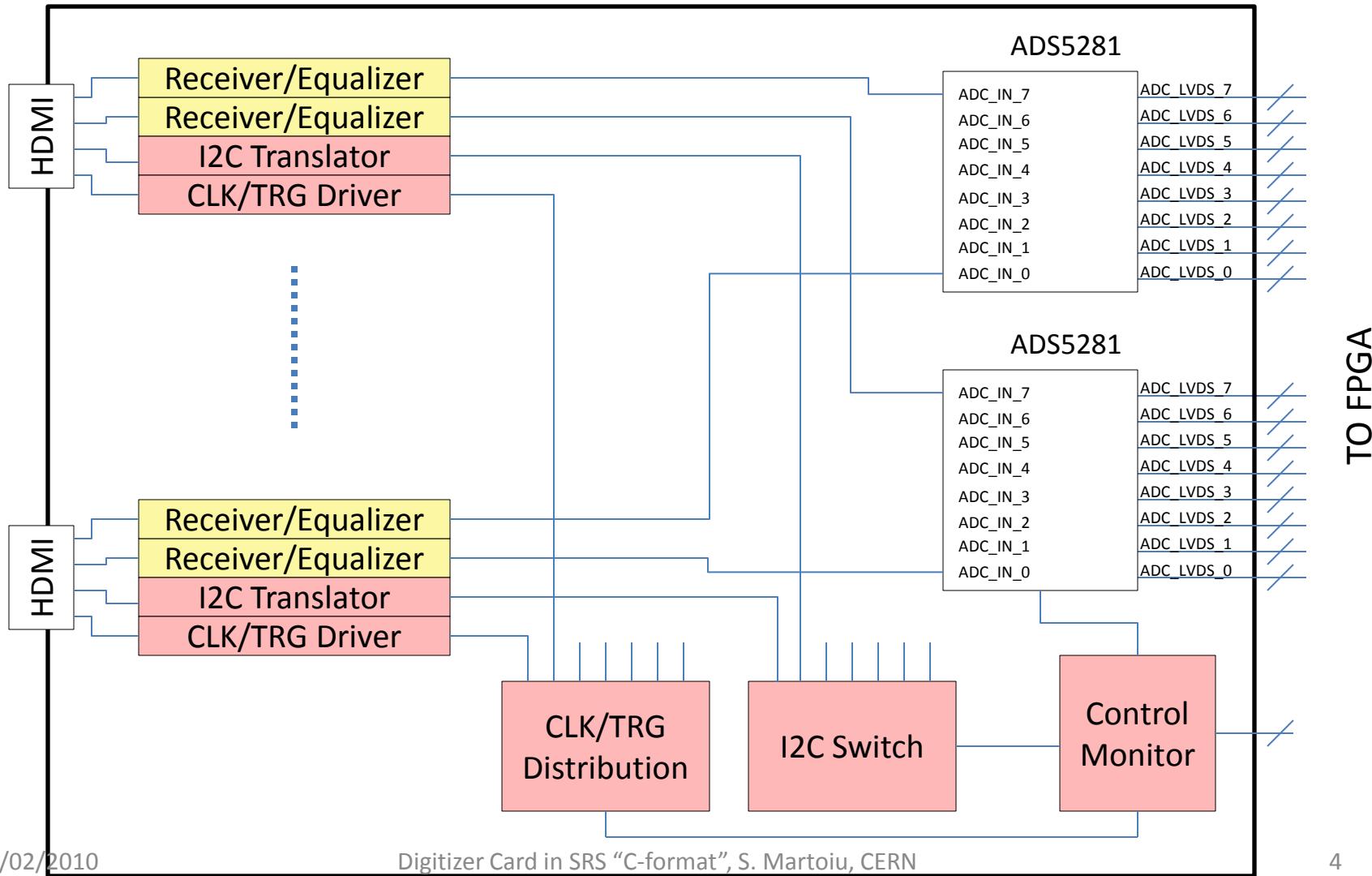
- 2 Octal ADCs with LVDS serial outputs (TI-ADS5281)
 - 16 Analog Inputs
 - 40MHz sampling
- Support for
 - 8 MASTER hybrids
 - 16 MASTER/SLAVE hybrids
- Power distribution
- Power/Temp monitoring
- Compatibility for future hybrids
(Beetle chip (?)

FEC Card (FPGA Firmware):

- ADC control and de-serialization
- APV Hybrid Slow-Control
- Data Acquisition
 - Data Format (?)
 - Data Reduction (zero-suppression, feature extraction, etc.) (?)

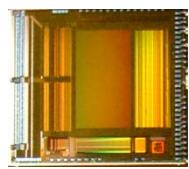
Simplified Block Diagram

C-type Card



Input Equalization

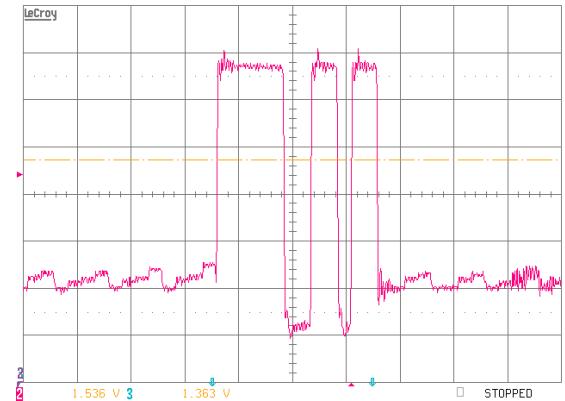
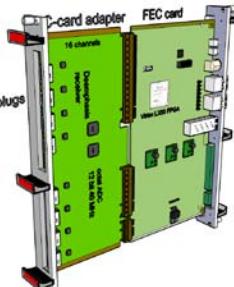
APV25



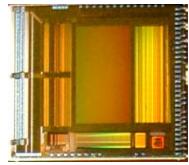
Short Cable



8 x HDMI cable plugs



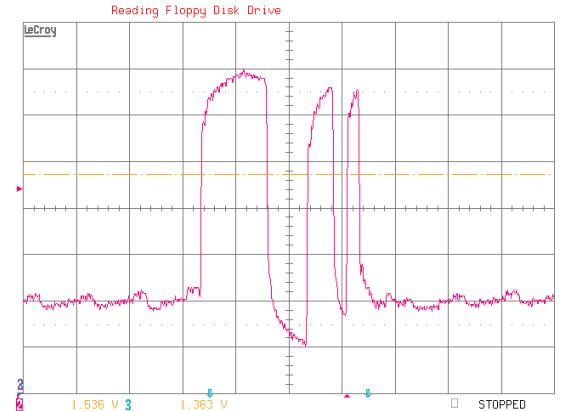
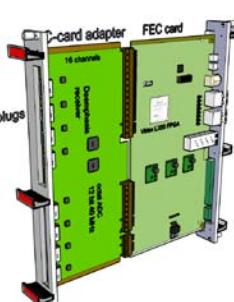
APV25



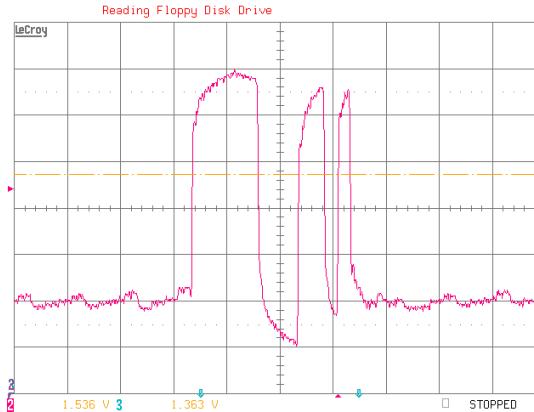
Long Cable



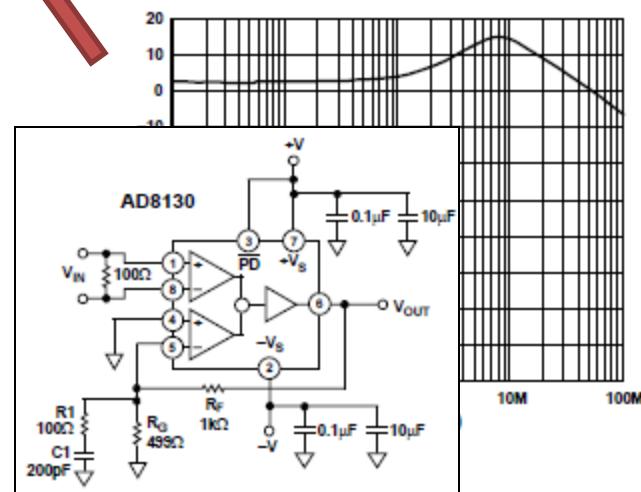
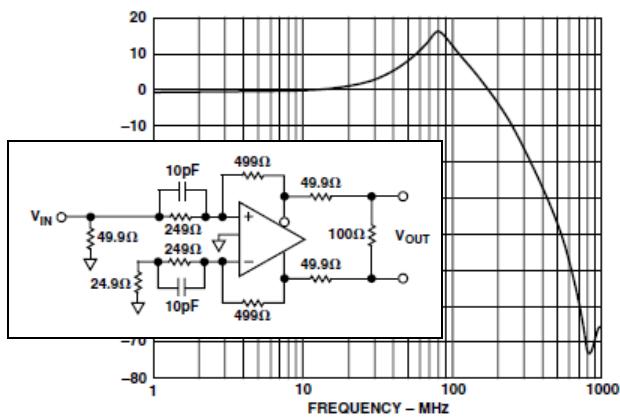
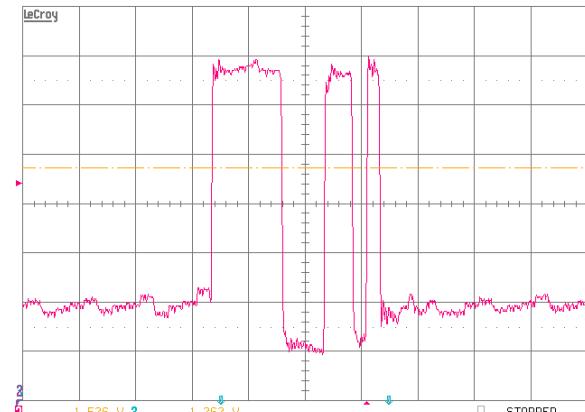
8 x HDMI cable plugs



Input Equalization

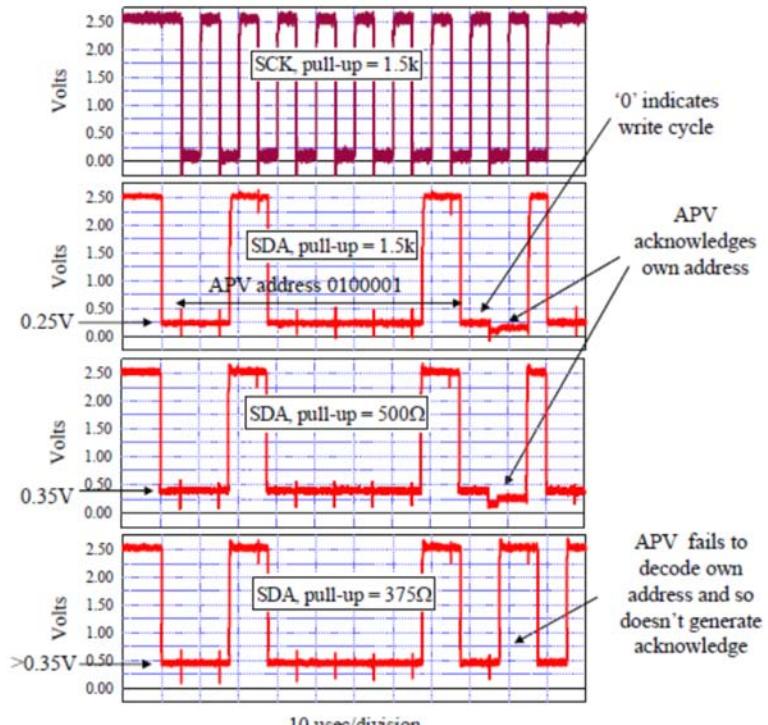


Equalizer



I²C Level Translation

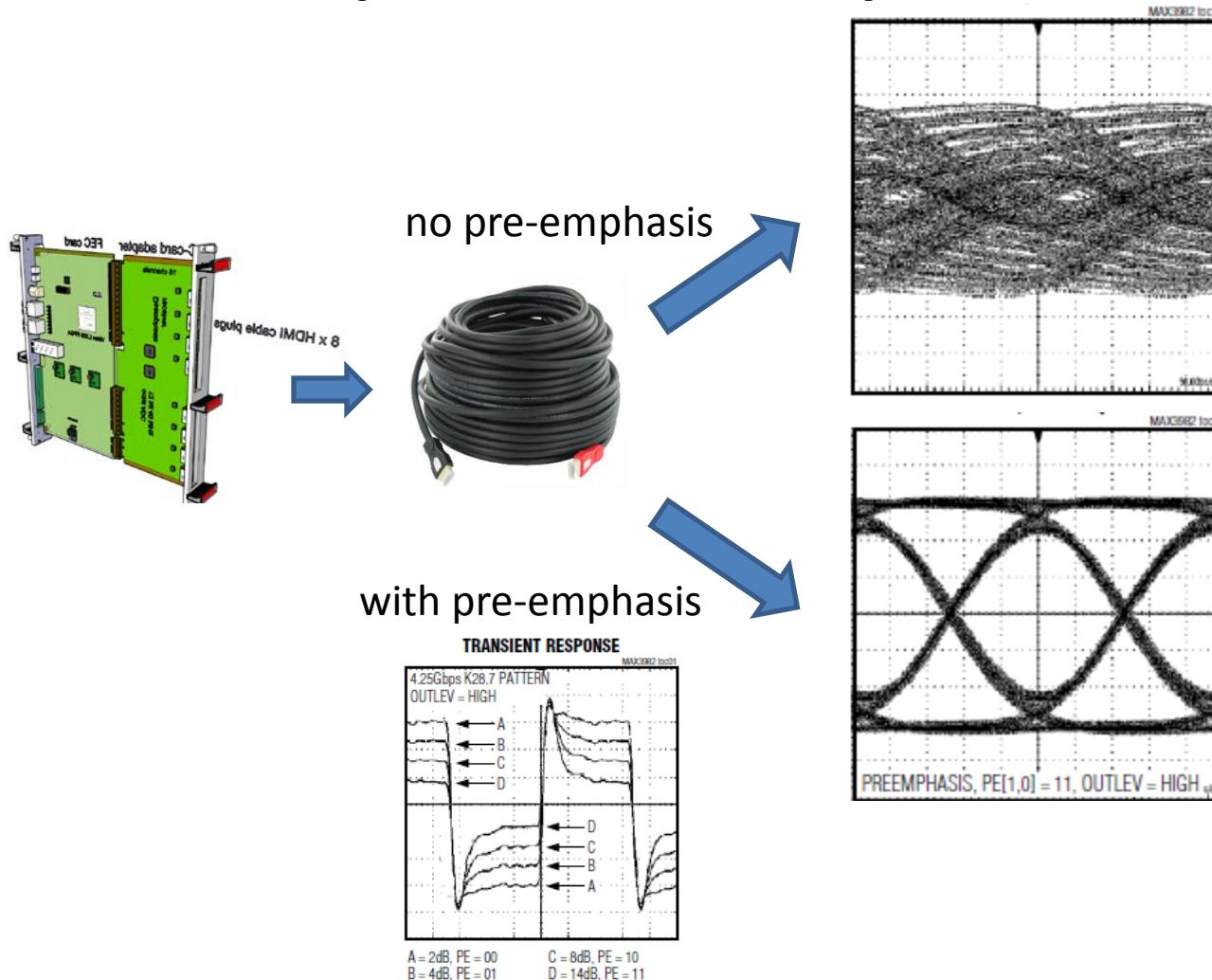
Measurements on the CCU module/hybrid setup



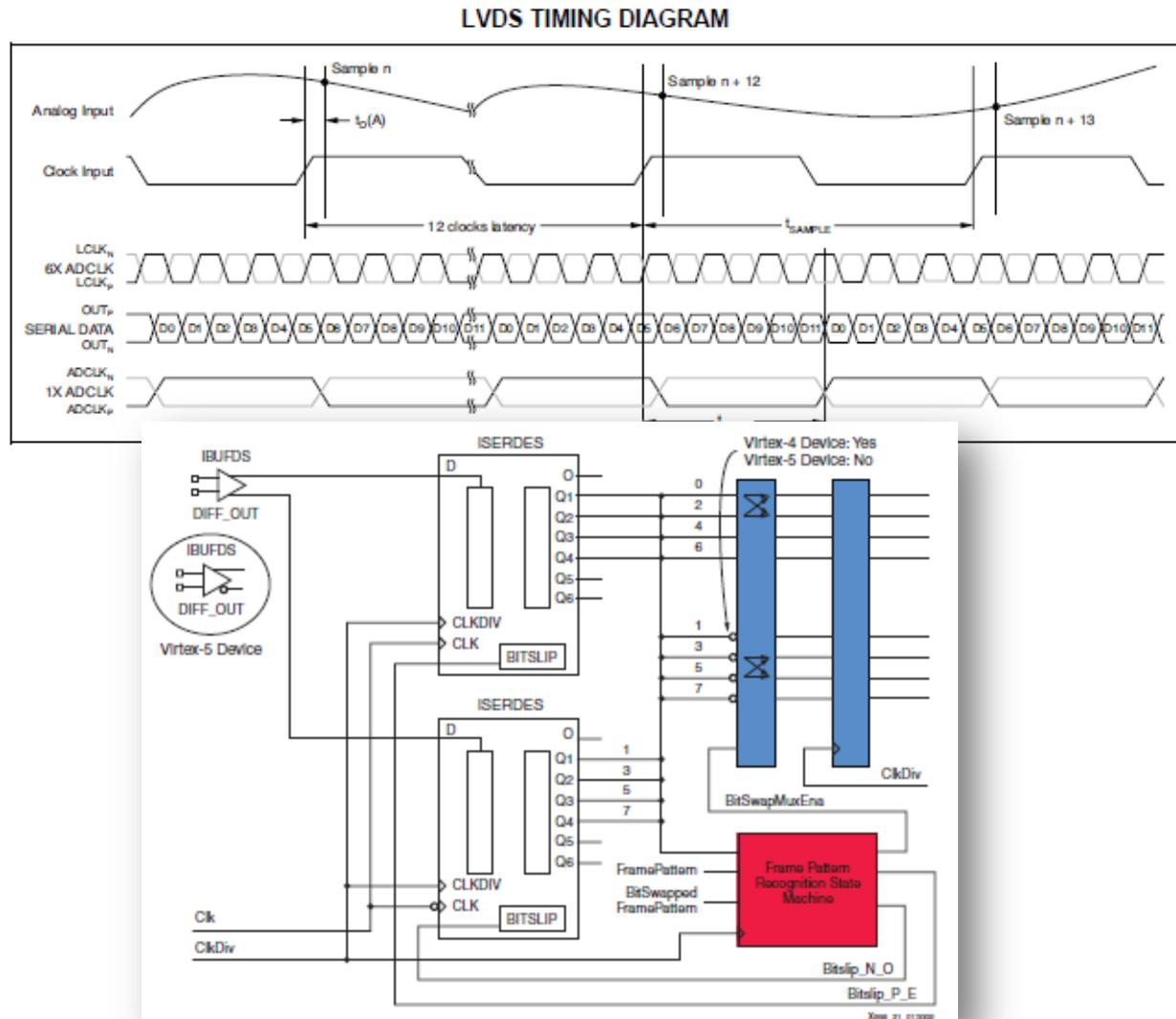
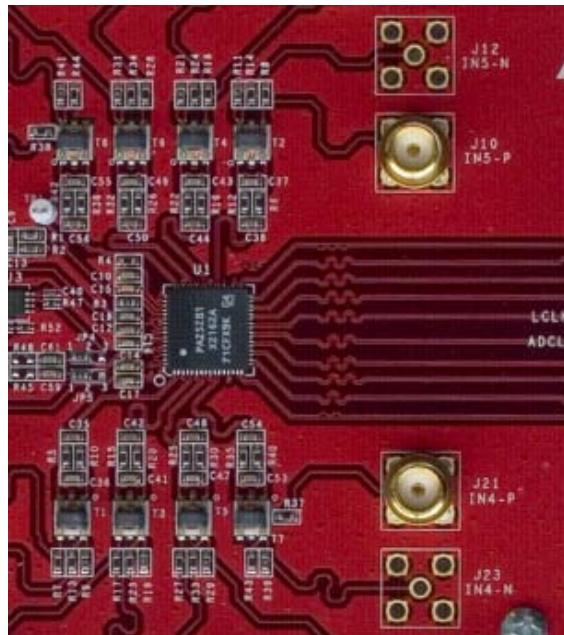
I²C transaction fails at pull-down voltage $> \sim 0.35V$
corresponding to pull-up resistance of
 $375\Omega = 1.5k \parallel 500\Omega$
(1.5k is built in resistance on CCU module)

- APV25 $V_L < 0.35V$
- I²C Standard $V_{L,max} = 0.4V$
- *in general, commercial I²C ICs multiplexers/switchers/etc. do not guarantee adequate low-level voltage*
- *some low-voltage translators may work (PCA9517 – TI, NXP)*
- *discrete circuitry*

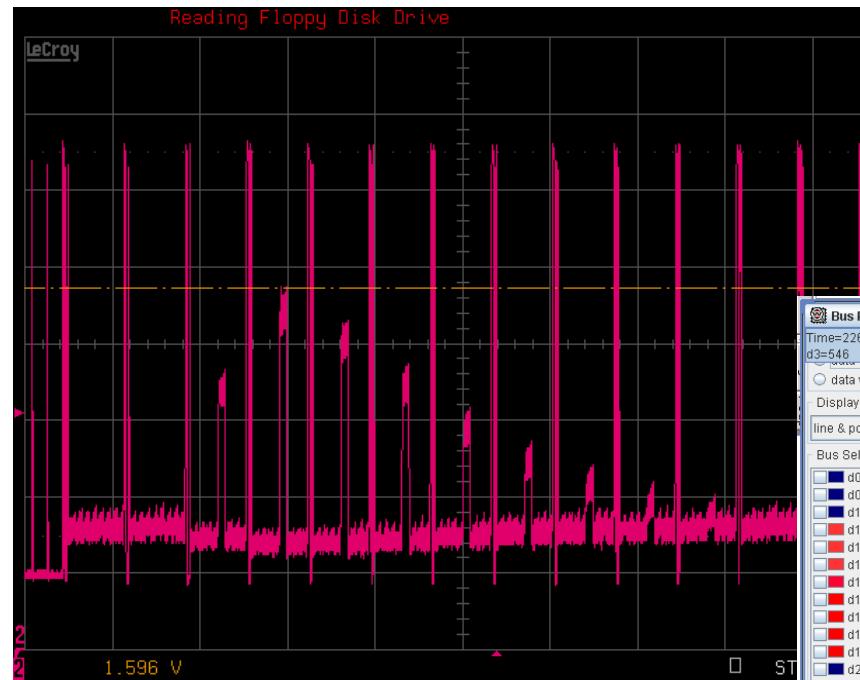
Output Pre-Emphasis



ADC De-serializer

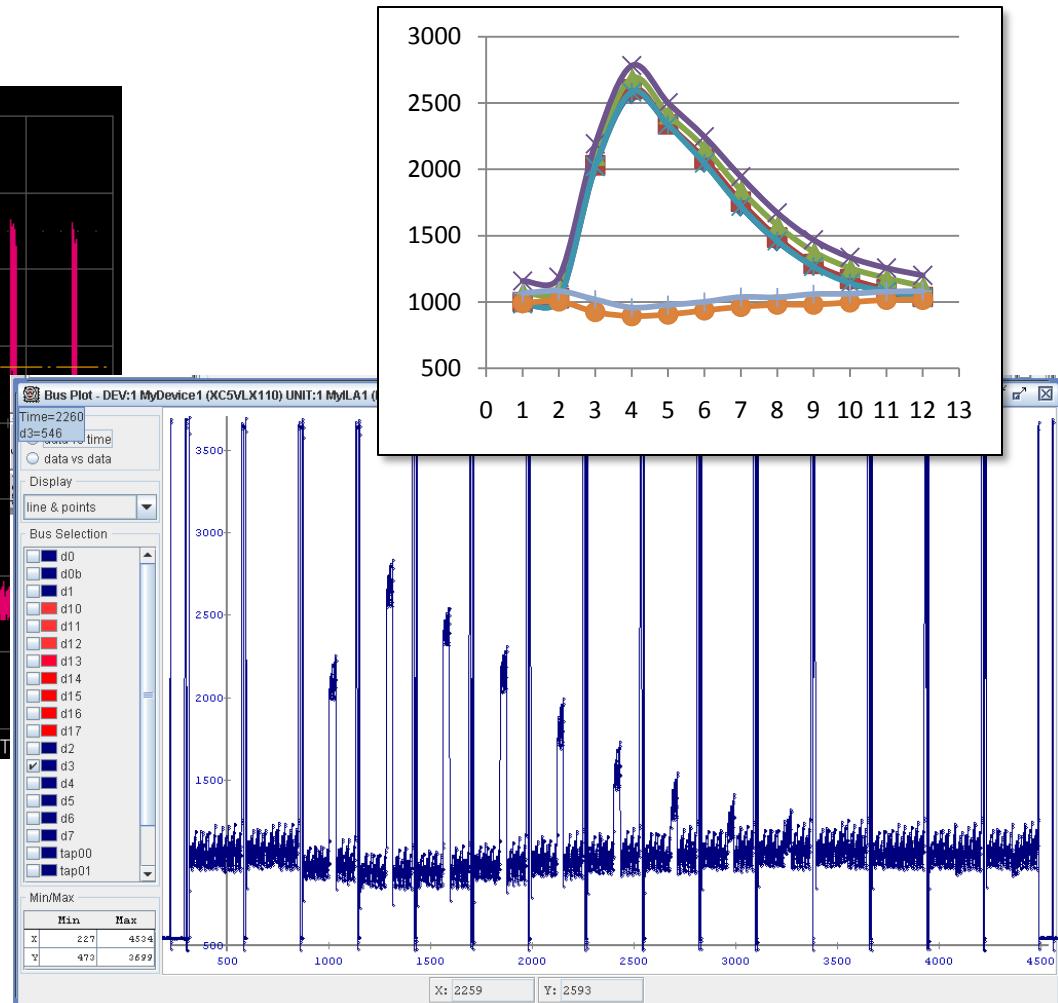


Firmware Development



Oscilloscope – APV Output

Virtex5 FPGA



Chipscope – Digitized Data from FPGA

TestBench

