FEC: features and an application example

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NEXT Experiment

Outline

- **A list of features in the FEC card**
- **Prototype production schedule**
- **FEC firmware development**
- **Application: NEXT-1 phase of the NEXT experiment**

A list of features in the FEC card.

A list of features in the FEC card

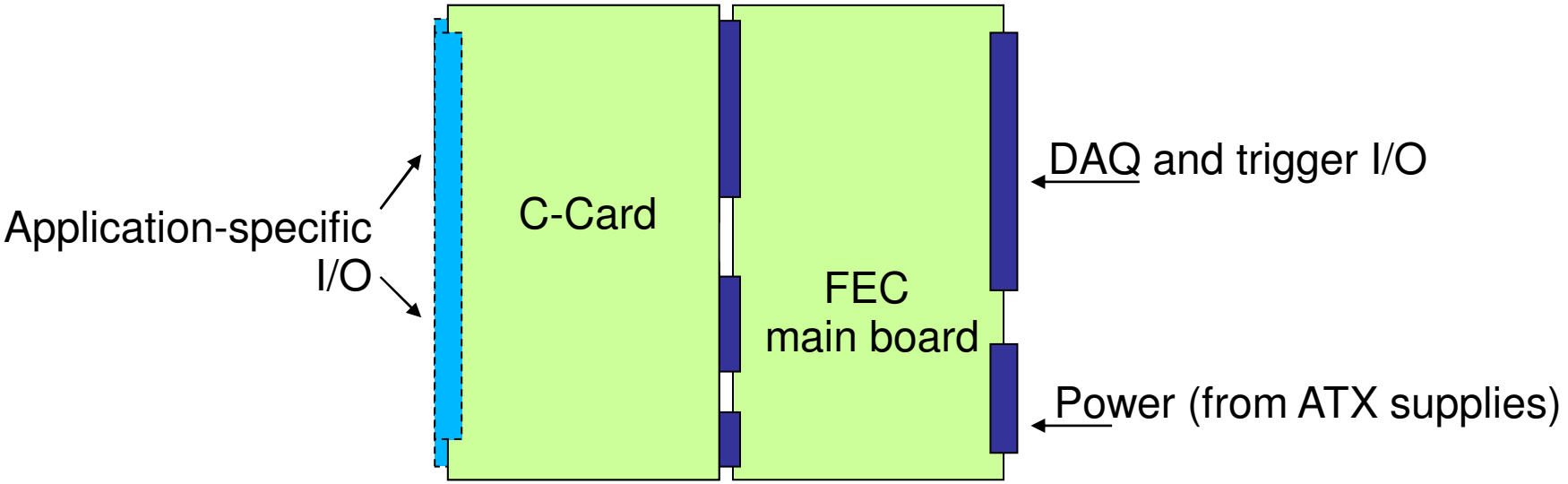
Concept

Design a common interface between the RD51 DAQ (SRUs and/or DATE PCs) and a wide range of front-end electronics designs.

This requires modularity, I/O flexibility and reconfigurability.

Common FEC mainboard
+ additional A, B and C-sized interface cards

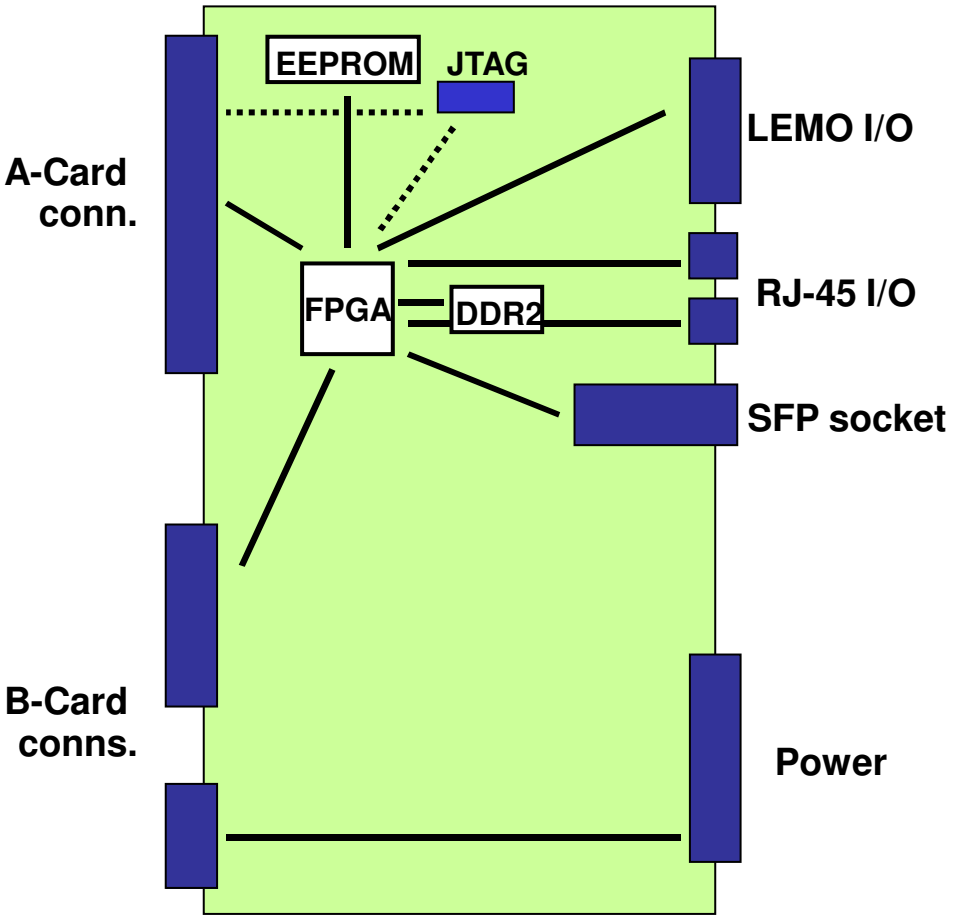
FPGA



6Ux220mm mechanics for Eurocard chassis

A list of features in the FEC card

What's in the FEC mainboard?



- FPGA: Xilinx Virtex-5 LX50T FF665
- Buffer: 2Gbit DDR2(MT47H128M16)@400 MHz
- 1Kb EEPROM for ID

- 1 LEMO-00 NIM input
- 1 LEMO-00 NIM output
- 1 LEMO-0B LVDS input

- 2xRJ-45 LVDS I/O (2 pairs in, 2 out each)

- 1 SFP module (GbE copper or optical)

- 1 daisy-chainable power input (3.3V, 5V, 12V, -12V, -5V) from an ATX power supply

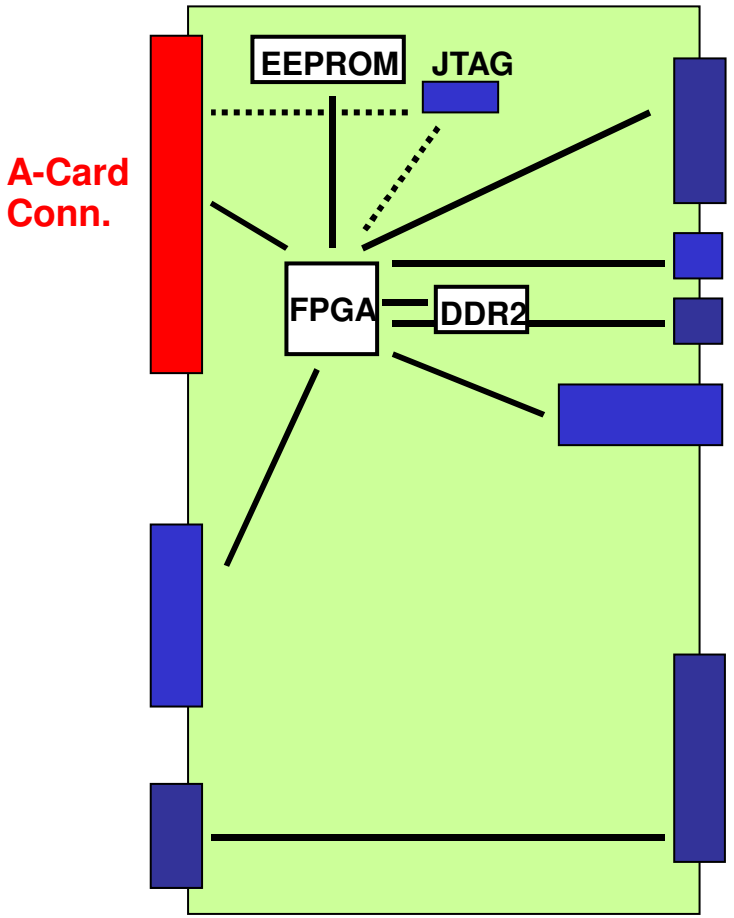
- 2-pin bias voltage input (up to 400V)

- 1x PCIe x16 (164 pin)
- 1x PCIe x8 (98 pin)
- 1x PCIe x1 (36 pin) for power

- Daisy-chainable JTAG
- On-board voltages monitor

A list of features in the FEC card

What I/O is available for the A-Card?



➢ Available I/O lines

- 20 LVDS pairs (8 can be clock inputs to the FPGA)
- 32 I/Os configurable as 32 slow SE, 16 fast SE or 16 differential, with selectable I/O signaling (VPIO: 1.8V, 2.5V, 3.3V)
- 1 full MGT interface (in, out + clock pairs)
- JTAG interface (2.5V levels, 3.3V tolerant)
- I2C bus (2.5V levels)
- Present and powergood lines
- Power lines: 2xVPIO, 4x5V, 1x12V, 1x-12V

➢ EEPROM interface via I2C bus

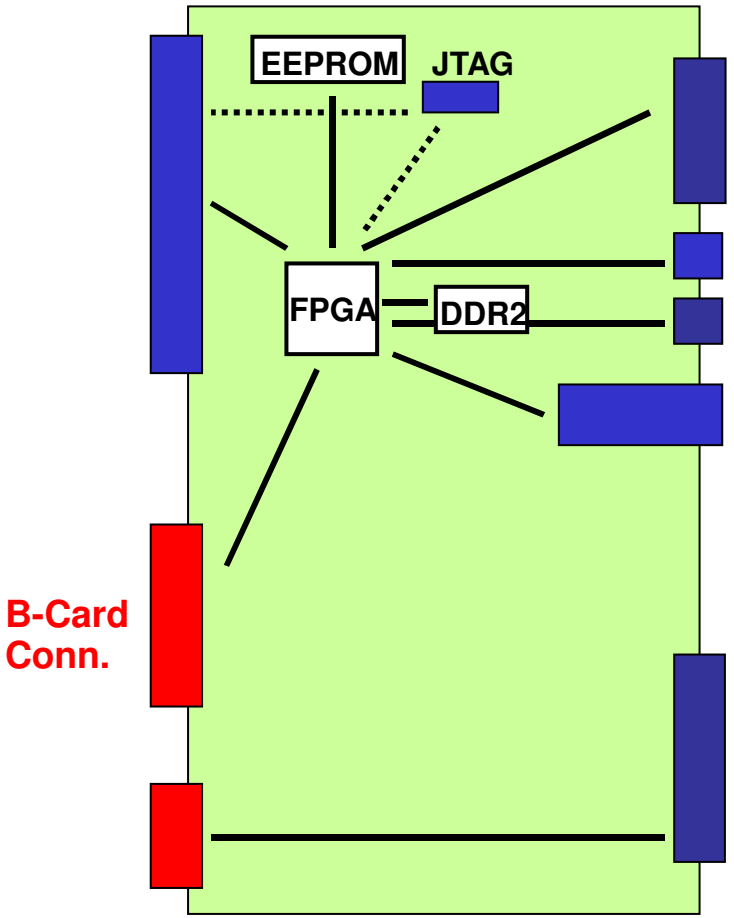
- Mandatory: A-Cards have a AT24C01B compatible EEPROM
- This is used for Card ID
- After configuration, FPGA I/Os inactive until A-Card EEPROM is checked

➢ Temp and voltage monitoring via I2C bus

- Optional: A-Cards can have an I2C ADC for such purpose. First supported device: AD7417 (OTI line via powergood and CONVST via present line)

A list of features in the FEC card

What I/O is available for the B-Card?



➢ Available I/O lines

- 20 LVDS pairs (8 can be clock inputs to the FPGA)
- 28 I/Os configurable as 28 SE or 14 differential, with selectable I/O signaling (VPIO: 1.8V, 2.5V, 3.3V)
- 2 MGT interfaces (in, out + clock pairs)
- I2C bus (2.5V levels)
- Present and powergood lines
- Power lines: 2xVPIO, 5x5V, 5x3.3V, 2x12V, 2x-12V, 2x-5V
- Bias voltage: 2xBias_GND, 2xBias_HV

➢ EEPROM interface via I2C bus

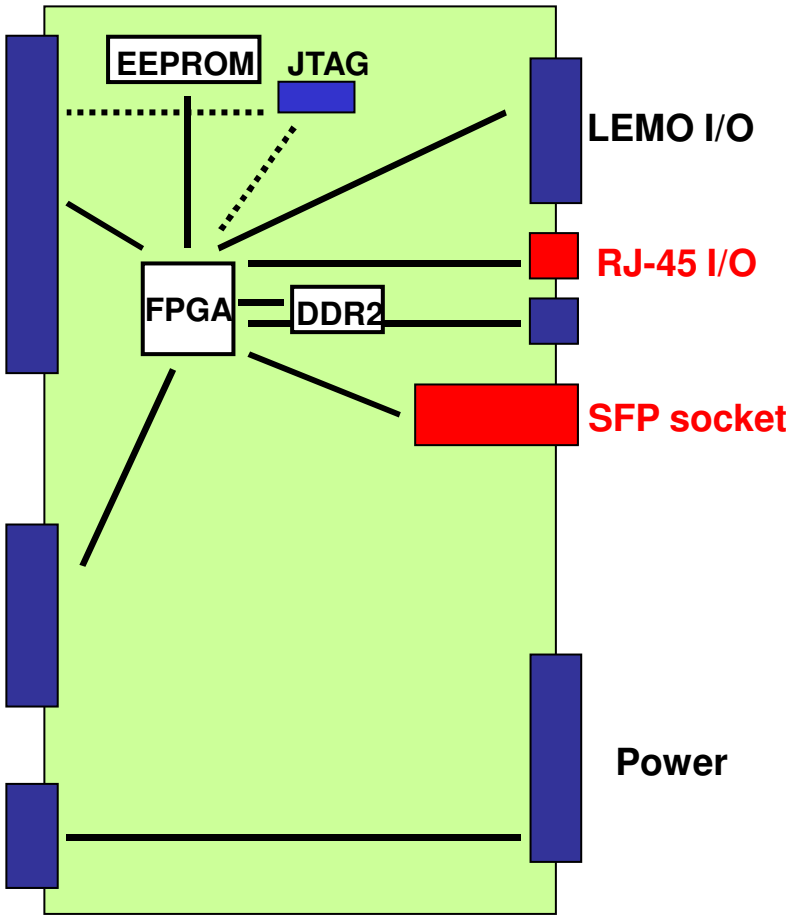
- Mandatory: Same functionality as described for A-Cards

➢ Temp and voltage monitoring via I2C bus

- Optional: Same functionality as described for A-Cards

A list of features in the FEC card

How do I connect it to the DAQ?



- Option 1: GbE to DATE via SFP module
  - Intended for stand-alone, test and small systems
  - This solution has been developed and tested (collab.CERN+U.P.Valencia)

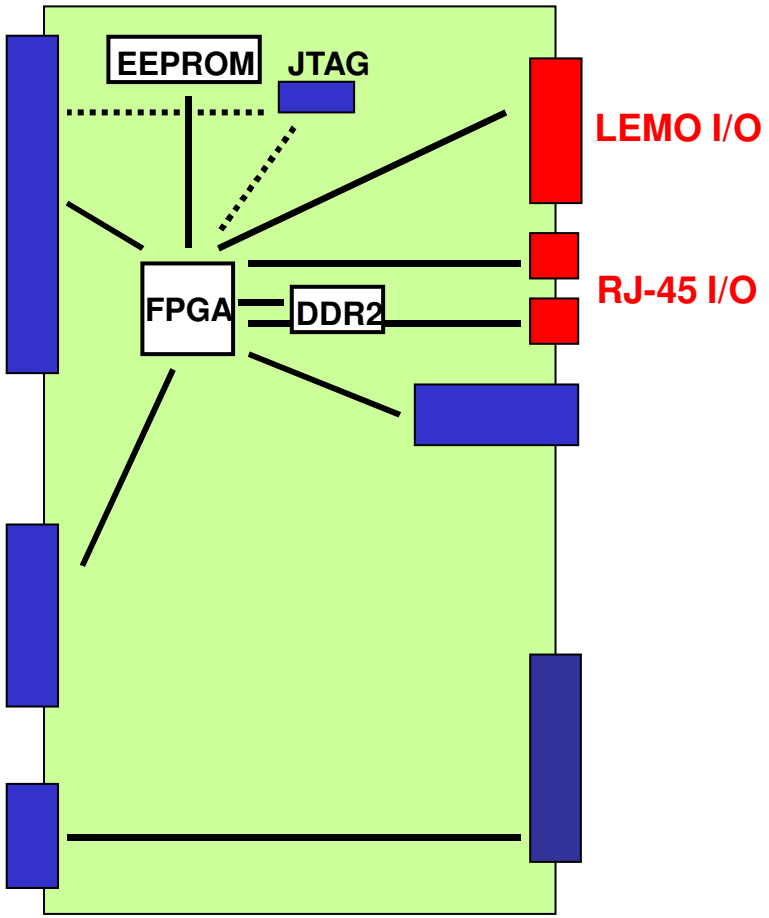
- Option 2: To SRU via RJ-45 conn. and DTC link protocol
  - Intended for larger systems
  - This solution is being developed (collab.CERN+U.Wuhan)

- Option 3: To SRU via SFP module

  Foreseen as an option for “SRU v2”

A list of features in the FEC card

How do I connect it to trigger and clock distributions?

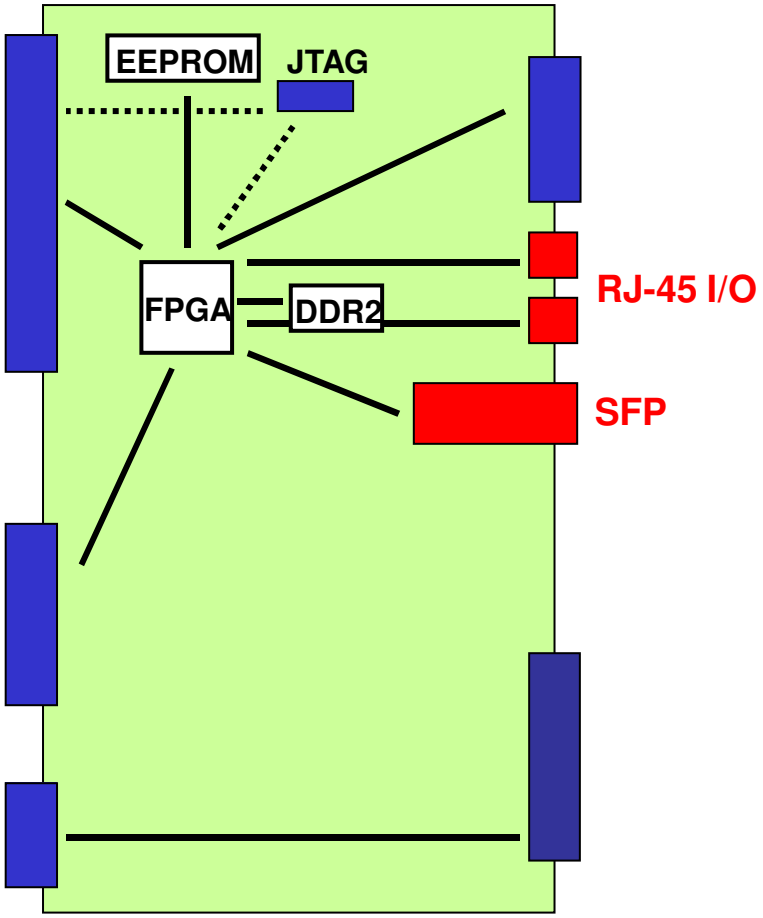


- Possible clock inputs
  - LEMO LVDS input
  - LVDS on RJ-45: SRU conn. or second conn.
  - Additionally, on-board 200 MHz and 125 MHz clocks
- Possible trigger inputs
  - LEMO NIM input
  - LEMO LVDS input
  - LVDS on RJ-45: SRU conn. or second conn.
- Possible trigger outputs
  - LEMO NIM output
  - LVDS on RJ-45: SRU conn. or second conn.

- Possible? connection to future CERN GBT via A-Card or B-Card

A list of features in the FEC card

How about slow-controls?



➢ Option 1: slow-controls from SRU via RJ-45 and DTC link protocol

- Available only is SRUs are present in the architecture
- DCS card production stopped…

➢ Option 2: slow-controls from DATE via SFP module

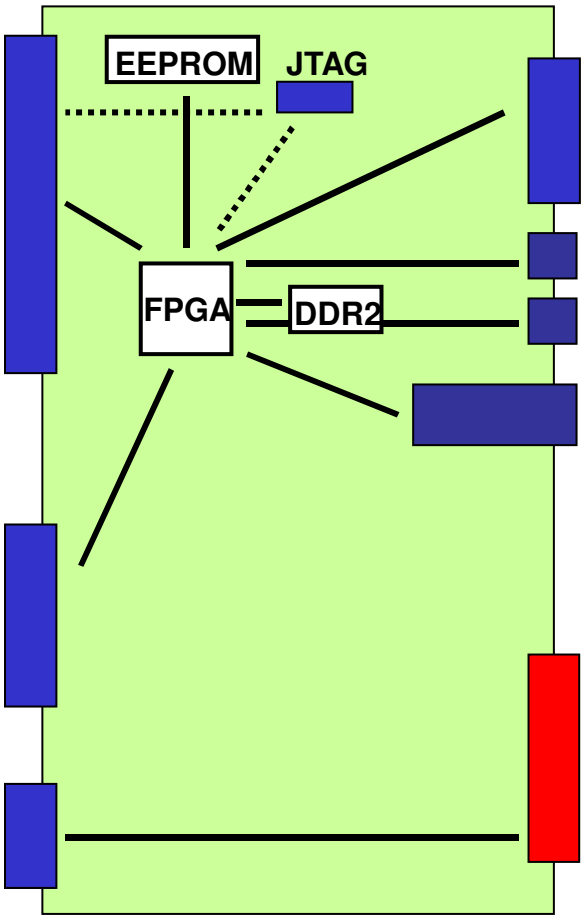
- First tests are successful… Work in progress (CERN+UP Valencia)

➢ Additional alarms-system

- Options 1,2 do not seem to allow slow-controls during data taking in the current configuration (can this be changed?)
- Additional alarms-system needed in some applications for power supply failure, module overheating,…
- We are developing an alarms system based on PLCs
- Second RJ-45 could be used to interface the alarms-system

A list of features in the FEC card

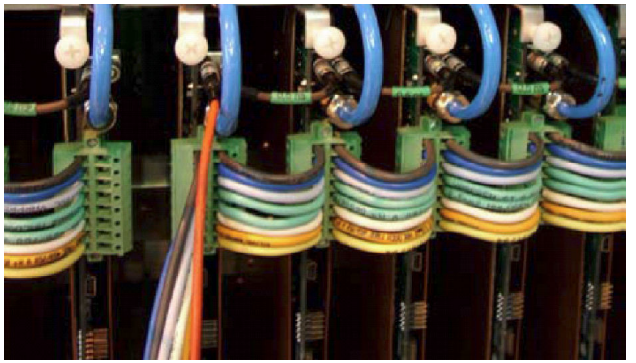
Can I hear a bit more on the power?



➢ 8-pin power connector from Phoenix

- Daisy chainable

- Standard ATX power supplies can be used



- No fuses on the FEC card… these can be included in the ATX-to-FEC connector (to be developed)

➢ Additional 2-pin connector for bias voltage (<400V)

- Directly fed to the B-Card after filtering (10nF cap + transient suppression double diode)

Prototype production schedule.

Prototype production schedule

Boards design

- Schematic capture is finished
- Board layout in progress

PCB production

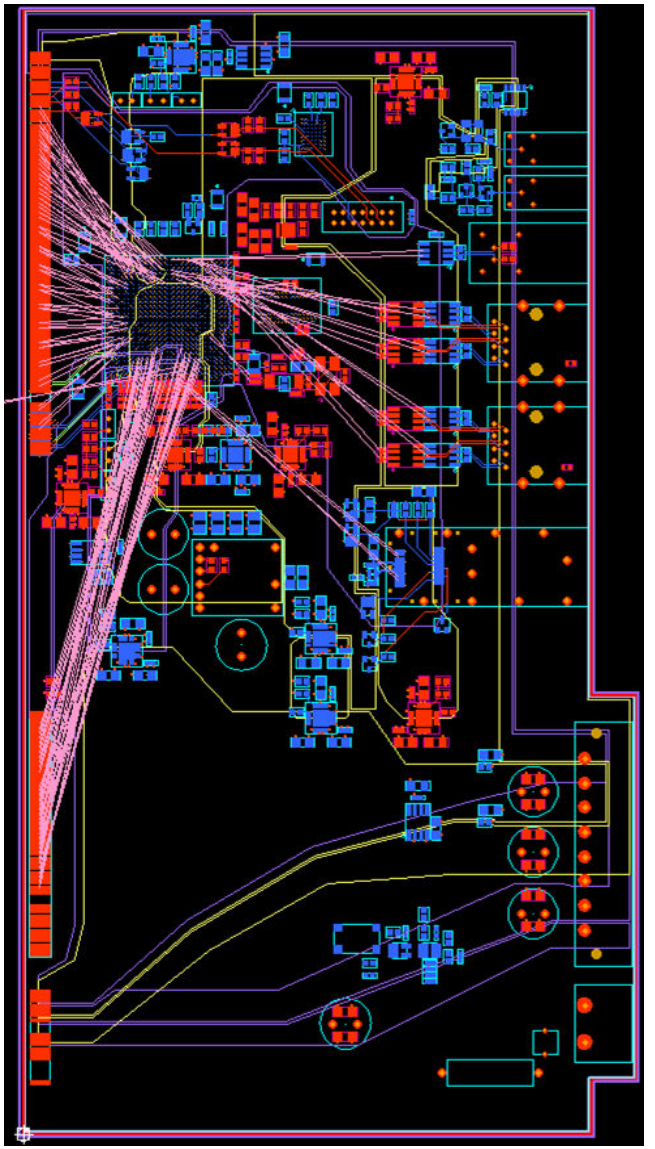
- Scheduled for March/April
- 20 PCBs in the first batch

Component mounting

- Scheduled for April
- BGAs and other ICs to be mounted in a company
- Passives to be mounted in-house at University

Board test

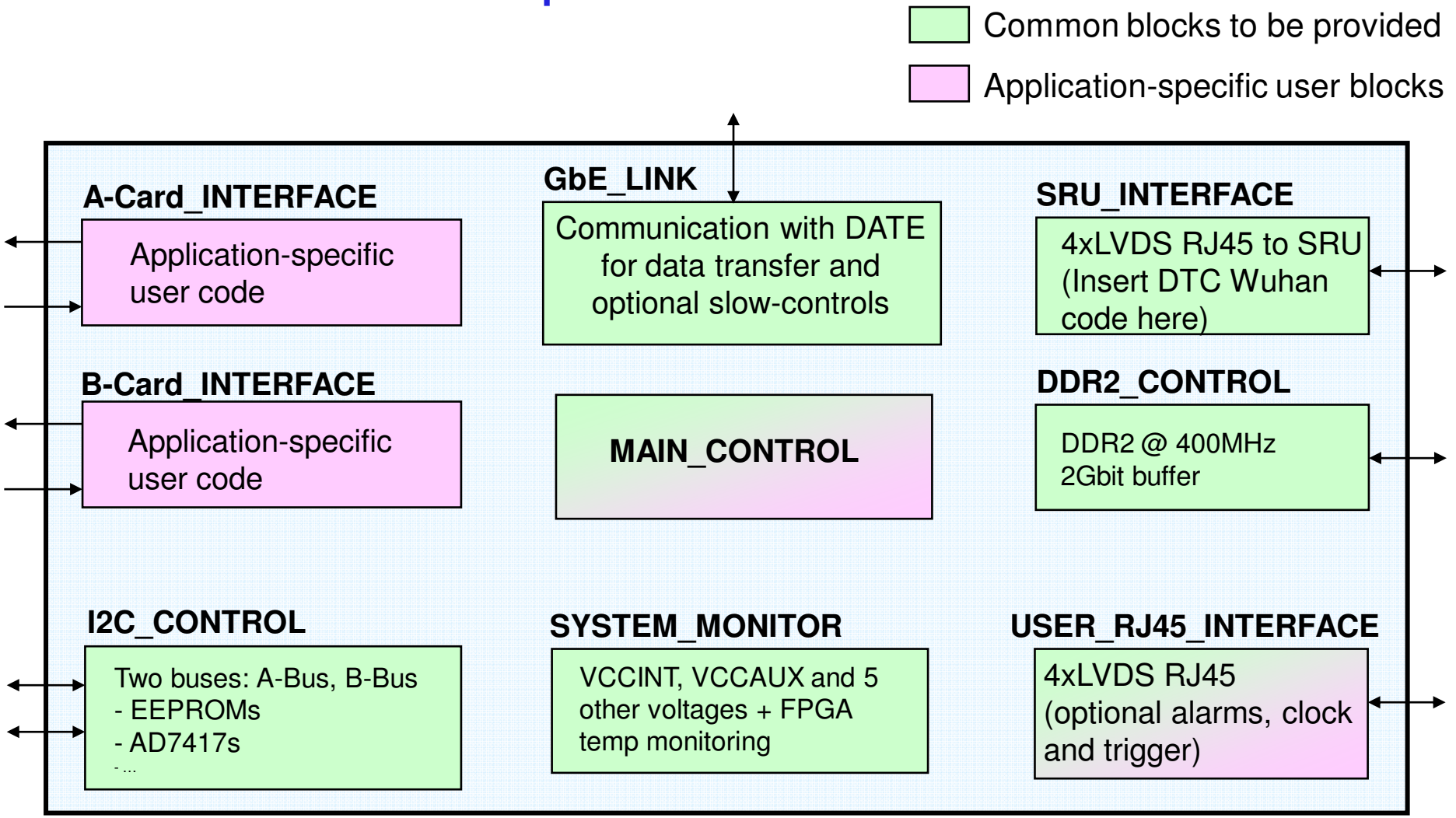
- Scheduled for May
- Basic FPGA firmware is being developed



FEC firmware development.

- We can provide a basic set of features to RD-51 users
- Users must then add their application-specific code

FEC firmware development



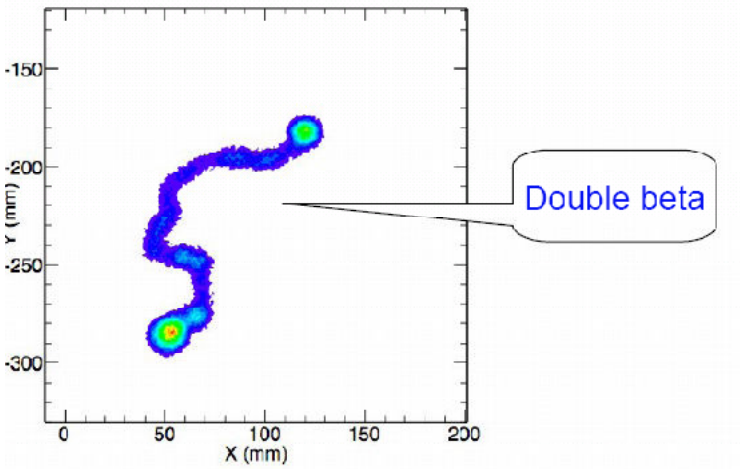
- Manpower for green blocks: 1,5 engineers
- Basic code development started in Valencia in mid February, to be released by June

First application: NEXT-1 phase of the NEXT experiment.

NEXT-1 phase of the NEXT experiment

NEXT-1

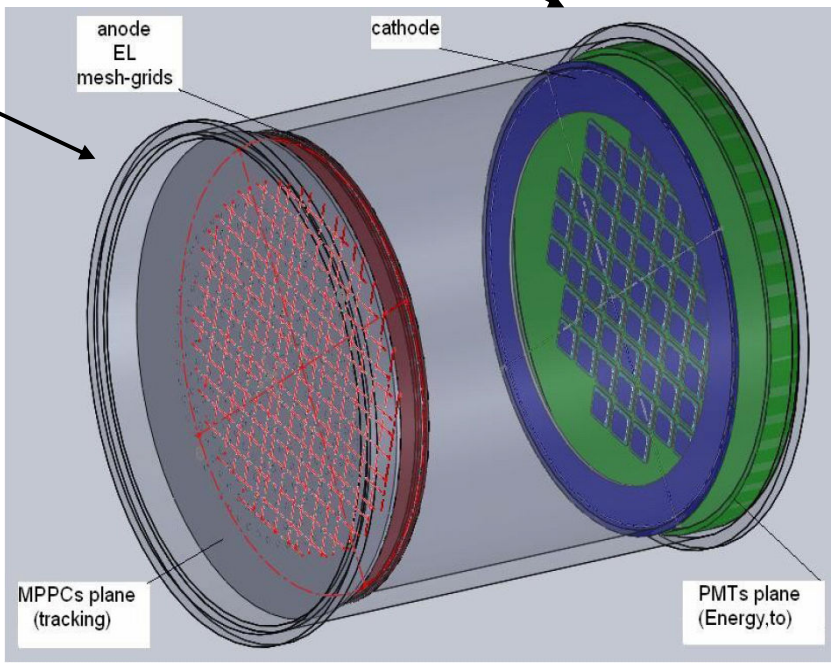
- Small-scale electroluminiscent TPC filled with ^{136}Xe gas
  - PMT plane for Energy and primary light measurement (trigger)
  - Opposite SiPM tracking plane



The track length at 10 bar is 30 cm. The ββ event track is a tortuous cord because of the multiple-scattering. The cord is ended by two blobs of energy.

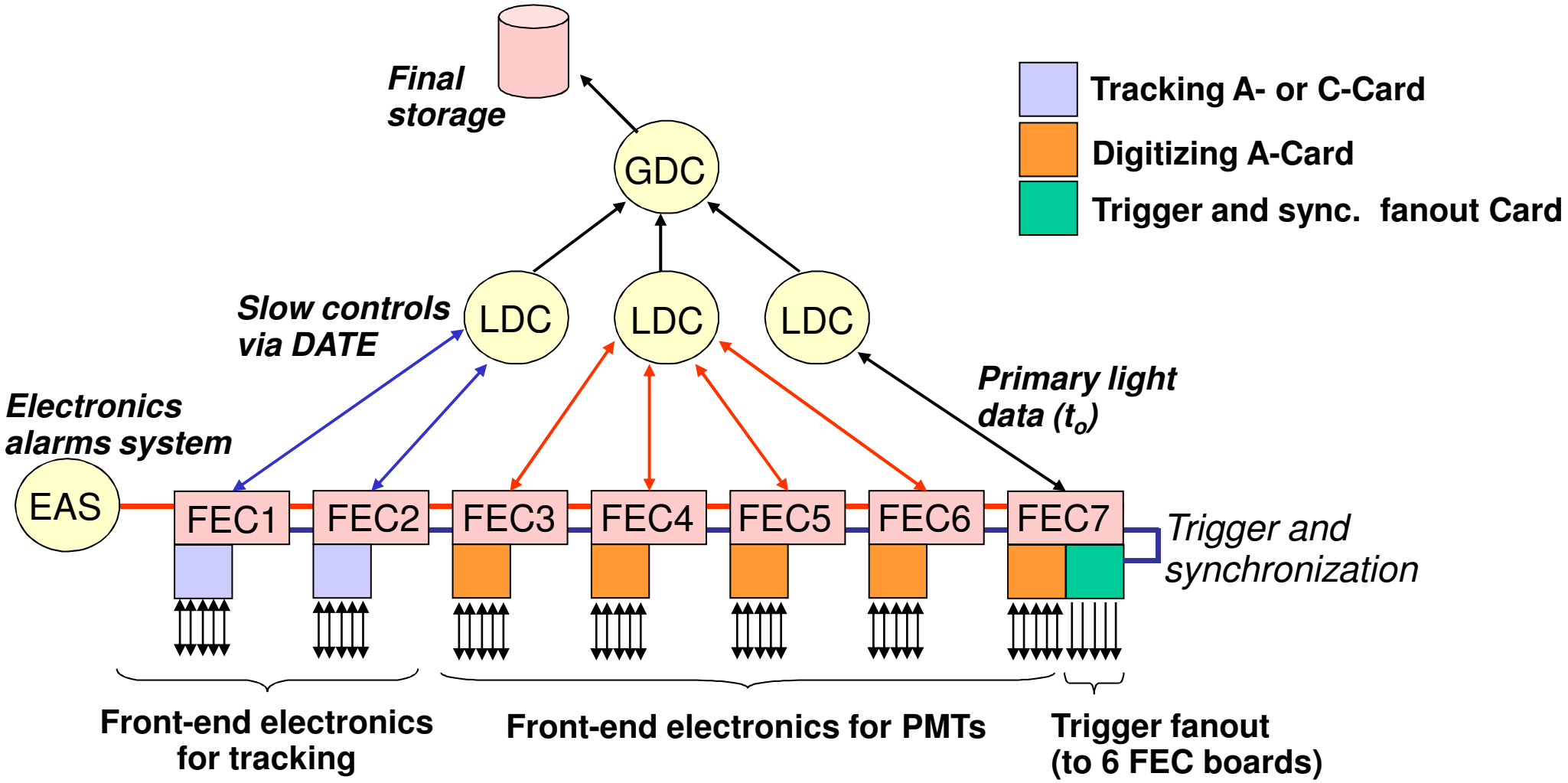
This pattern is distinguishable from the one electron track with energy near Qββ

LXe cannot resolve blobs



- Find out more about this ββ0ν experiment at: http://arxiv.org/PS_cache/arxiv/pdf/0907/0907.4054v1.pdf

NEXT-1 phase of the NEXT experiment



440 tracking channels
14 FE cards (32ch/card)

64 Energy ch (4 FE cards, 16ch/card)
+(1-to-4) primary light channels

NEXT-1 phase of the NEXT experiment

- No SRUs are needed for NEXT-1

- FEC cards with GbE link connect directly to DATE PCs (tested!)

- No GbE routers (DATE accepts unique data sources per GbE link in the current configuration)

- For NEXT-1 we need:

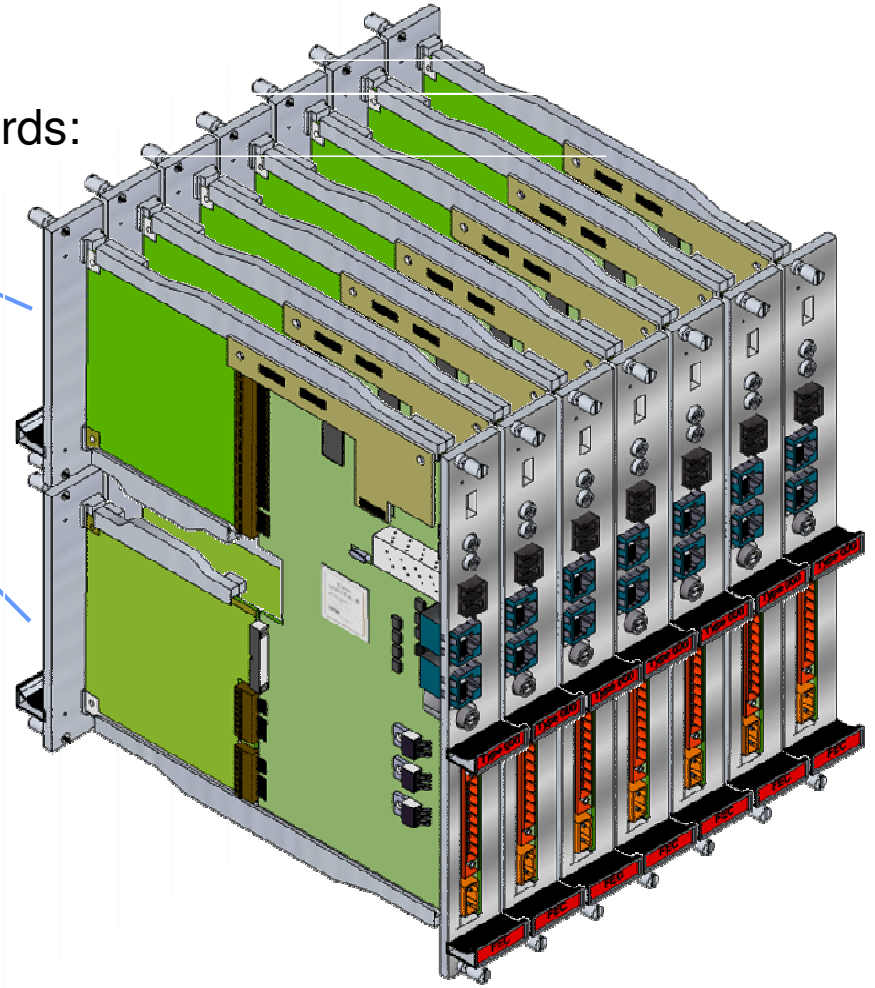
  -7 FEC modules equipped with function cards:

    -5 digitizing A-Cards

    -2 tracking A-Cards or C-Cards

    -1 trigger fanout B-Card

  - 4+ DATE PCs (3xLDC + GDCs)



This accounts for:
- 440 tracking channels
- 64 PMT channels (EL)
- <8 PMT channels (primary light)
- Primary-light based trigger and distribution

NEXT-1 phase of the NEXT experiment

Interface to the front-end electronics

➢ Analog front-end (PMTs): we receive 16 analog differential signals and send an I2C control bus for channel settings

- 68-pin VHDCI connector with differential pinout?
- 50-pin D Sub?
- Flat cable?

➢Digital front-end (SiPMs) for tracking: 4xLVDS RJ-45 connector, full duplex: clock+data in each direction
(similar to FEC-SRU LVDS link)

- FEC-to-frontend data: short frames with timestamp sync, trigger and monitoring request
- Frontend-to-FEC data: digitized sensor data + monitoring response

- We will not not power the front-end from the FEC
- We will digitally control the SiPM bias from the FEC

Thank you !