CNGS Irradiation Tests
April 2010

WIC- Crate

(Same material is installed in US85 for Warm Magnets protection)

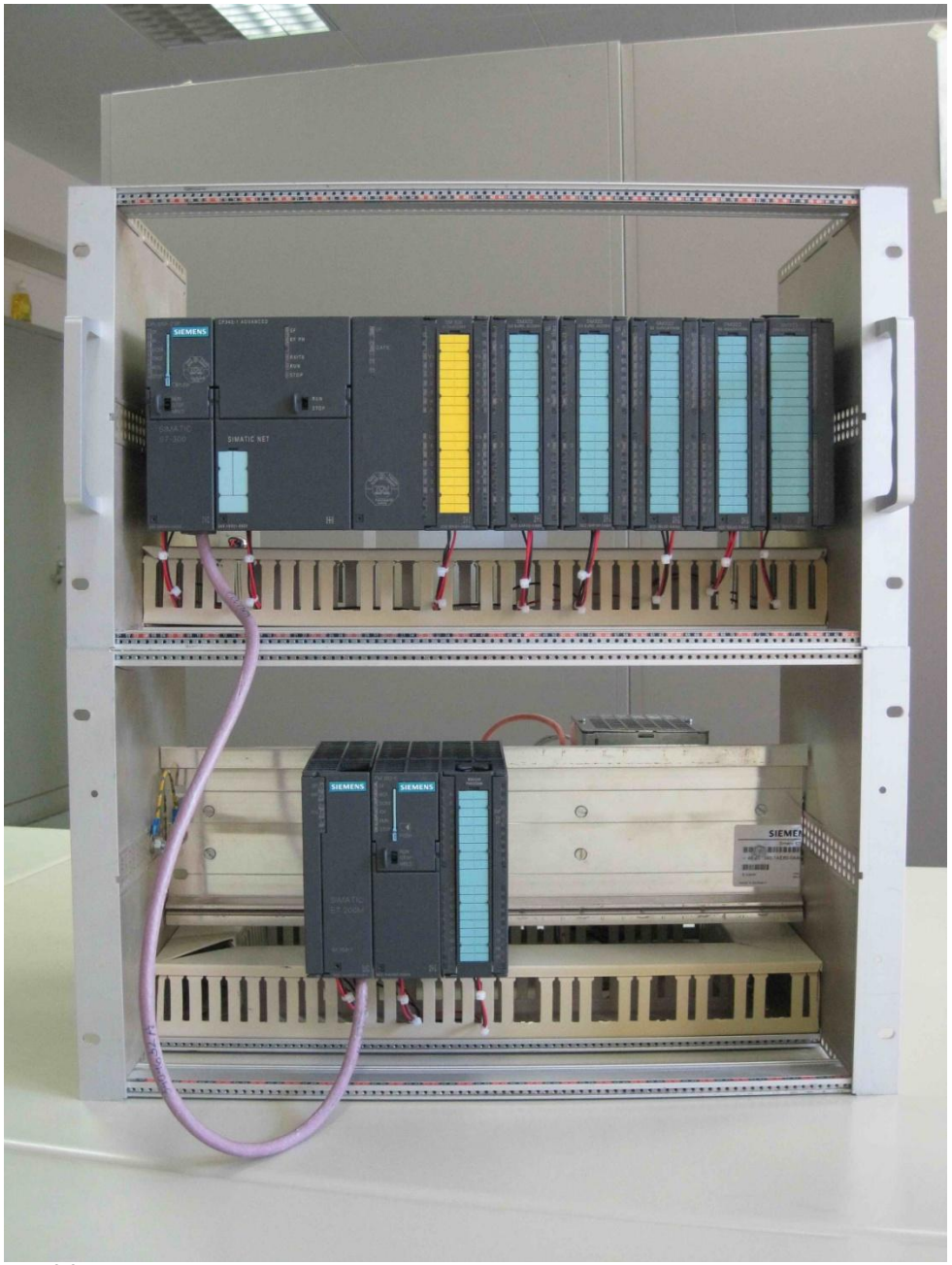
Materiel installed:

1 - Crate containing:

- PLC 315F 2 DP: **6ES7 315-6FF01-0AB0**
- Ethernet controller: **6GK7 343-1GX21-0XE0**
- 24 DI safety input module: **6ES7 326-1BK-0AB0**
- 2 x DO Relay output module: **6ES7 322-5HF00-0AB0**
- 2 x 32 DO module: **6ES7-322-1BL00-0AA0**

2 - Crate containing:

- IM153.1 - ET 200M: **6ES7 153-1AA03-0XB0**
- Boolean Processor - FM 352-5: **6ES7 352-5AH00-0AE0**



Extract from PVSS History buffer

1st error

2010.04.22 09:01:49.450	CIW	TEST	RBXWH.L8	CMD_ABORT_B_WIC	WIC output signal (channel B) for opening the FABORT loop in order to stop the power converter of circuit	BAD
2010.04.22 09:01:52.575	CIW	TEST	RBXWH.L8	CMD_ABORT_B_WIC	WIC output signal (channel B) for opening the FABORT loop in order to stop the power converter of circuit	OK
2010.04.22 09:01:54.734	CIW	TEST	RBXWSH.L8	CMD_ABORT_B_WIC	WIC output signal (channel B) for opening the FABORT loop in order to stop the power converter of circuit	BAD
2010.04.22 09:01:57.744	CIW	TEST	RBXWSH.L8	CMD_ABORT_B_WIC	WIC output signal (channel B) for opening the FABORT loop in order to stop the power converter of circuit	OK
2010.04.22 09:01:59.442	CIW	TEST	RBXWSH.R8	CMD_ABORT_B_WIC	WIC output signal (channel B) for opening the FABORT loop in order to stop the power converter of circuit	BAD
2010.04.22 09:02:02.457	CIW	TEST	RBXWSH.R8	CMD_ABORT_B_WIC	WIC output signal (channel B) for opening the FABORT loop in order to stop the power converter of circuit	OK
2010.04.22 09:02:03.824	CIW	TEST	RCBWH5.L8B1	CMD_ABORT_B_WIC	WIC output signal (channel B) for opening the FABORT loop in order to stop the power converter of circuit	BAD
2010.04.22 09:02:06.936	CIW	TEST	RCBWH5.L8B1	CMD_ABORT_B_WIC	WIC output signal (channel B) for opening the FABORT loop in order to stop the power converter of circuit	OK
2010.04.22 09:02:08.205	CIW	TEST	RCBWH5.L8B1	CMD_ABORT_A_WIC	WIC output signal for opening the FABORT loop in order to stop the power converter of circuit	BAD
2010.04.22 09:02:11.178	CIW	TEST	RCBWH5.L8B1	CMD_ABORT_A_WIC	WIC output signal for opening the FABORT loop in order to stop the power converter of circuit	OK
2010.04.22 09:02:12.040	CIW	TEST	RBXWH.L8	CMD_ABORT_A_WIC	WIC output signal for opening the FABORT loop in order to stop the power converter of circuit	BAD
2010.04.22 09:02:15.214	CIW	TEST	RBXWH.L8	CMD_ABORT_A_WIC	WIC output signal for opening the FABORT loop in order to stop the power converter of circuit	OK
2010.04.22 09:02:15.969	CIW	TEST	RBXWSH.L8	CMD_ABORT_A_WIC	WIC output signal for opening the FABORT loop in order to stop the power converter of circuit	BAD
2010.04.22 09:02:18.945	CIW	TEST	RBXWSH.L8	CMD_ABORT_A_WIC	WIC output signal for opening the FABORT loop in order to stop the power converter of circuit	OK
2010.04.22 09:02:19.702	CIW	TEST	RBXWSH.R8	CMD_ABORT_A_WIC	WIC output signal for opening the FABORT loop in order to stop the power converter of circuit	BAD
2010.04.22 09:02:22.692	CIW	TEST	RBXWSH.R8	CMD_ABORT_A_WIC	WIC output signal for opening the FABORT loop in order to stop the power converter of circuit	OK
2010.04.22 13:51:43.105	CIW	TEST	CIW.BB4.TTEST	CMD_UPERM_B1B2_A_FM352_1	First FM352 Output signal A sent by the Warm Magnets Interlock System to the nearest BIC in case of failure in any Warm Magnet	BAD
2010.04.22 13:51:43.105	CIW	TEST	CIW.BB4.TTEST	CMD_UPERM_B1B2_B_FM352_1	First FM352 Output signal B sent by the Warm Magnets Interlock System to the nearest BIC in case of failure in any Warm Magnet	BAD
2010.04.22 13:51:56.484	CIW	TEST	CIW.BB4.TTEST	CMD_UPERM_B1B2_A_FM352_1	First FM352 Output signal A sent by the Warm Magnets Interlock System to the nearest BIC in case of failure in any Warm Magnet	OK
2010.04.22 13:51:56.484	CIW	TEST	CIW.BB4.TTEST	CMD_UPERM_B1B2_B_FM352_1	First FM352 Output signal B sent by the Warm Magnets Interlock System to the nearest BIC in case of failure in any Warm Magnet	OK

Errors from Boolean Processor

Action taken:

- 22/04/2010 - 11h30 AM 1st Hard reset after PLC failure:
  ➔ PLC work again
- 22/04/2010 - 1h51 PM Error from Boolean Processor :
  ➔ No reset needed

- 23/04/2010 – 6h30 AM : - No communication with the PLC
  - No Error in the PVSS history buffer
  Multiple Hard reset after PLC failure:
  ➔ No response from PLC
  ➔ **PLC HS**