First prototyping run

Upgrade of the front end electronics of the LHCb calorimeter

Calorimeter upgrade meeting – Phone Conference– May 5th 2010

Outlook

I. Introduction

II. Possible channel architecture

III. Key issues to be tested

IV. Summary

I. Introduction: requirements

- Requirements as agreed during last year (PM gain 1/5):

	Value	Comments
Energy range	0-10 GeV/c (ECAL) Transverse energy	1-3 Kphe / GeV Total energy
Calibration	4 fC /2.5 MeV / ADC cnt	4 fC input of FE card: assuming 25 Ω clipping at PMT base 12 fC / ADC count if no clipping
Dynamic range	4096-256=3840 cnts :12 bit	Enough? New physic req.? Pedestal variation? Should be enough
Noise	<≈1 ADC cnt or ENC < 5 -6 fC	< 0.7 nV/√Hz →
Termination	50 ± 5 Ω	Passive vs. active
AC coupling	Needed	Low freq. (pick-up) noise
Baseline shift Prevention	Dynamic pedestal subtraction (also needed for LF pick-up)	How to compute baseline? Number of samples needed?
Max. peak current	4-5 mA over 25 Ω 1.5 mA at FE input if clipping	50 pC in charge
Spill-over correction	Clipping	Residue level: 2 % ± 1 % ?
Spill-over noise	<< ADC cnt	Relevant after clipping?
Linearity	< 1%	
Crosstalk	< 0.5 %	
Timing	Individual (per channel)	PMT dependent

See talk about noise in June's meeting:

http://indico.cern.ch/materialDisplay.py?contribId=1&sessionId=0&materialId=slides&confId=59892

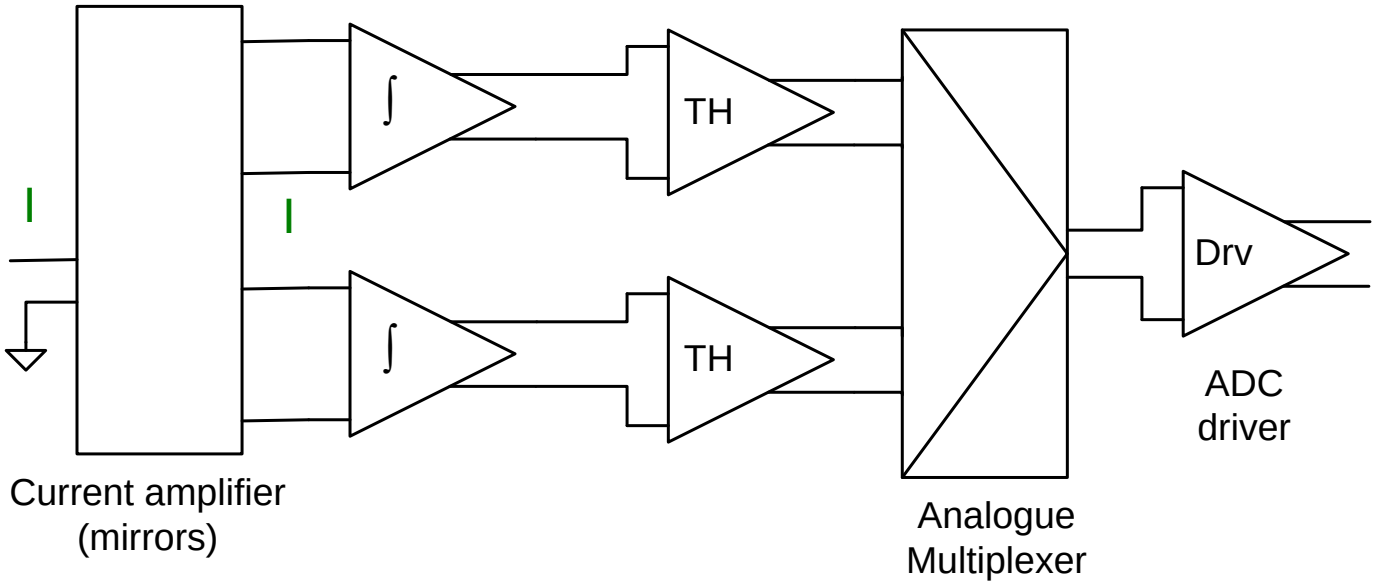
I. Introduction: mini@sic run

- AMS 0.35µm SiGe-BiCMOS S35 4M/4P
- Mini@sic run:
  - Smaller minimum area: 2 mm^2
  - Low cost: 800 € / mm^2

austriamicrosystems	J	F	M	A	M	J	J	A	S	O	N	D
austriamicrosystems 0.35µ CMOS C35B3C3 3M/2P/HR/5V IO		8		12			12				2	6
austriamicrosystems 0.35µ CMOS C35B4C3 4M/2P/HR/5V IO		8		12			12				2	6
austriamicrosystems 0.35µ CMOS C35OPTO 4M/2P/5V IO				12							2	
austriamicrosystems 0.35µ HV CMOS H35 50V 3M				26							8	
austriamicrosystems 0.35µ HV CMOS H35 50V 4M				26							8	
austriamicrosystems 0.35µ SiGe-BiCMOS S35 4M/4P						**7**					22	
austriamicrosystems 0.18µ CMOS C18 6M/1P/MIM			29								15	
austriamicrosystems 0.18µ HV CMOS H18 50V 4M/MIM		22			10			2			2	

II. Possible channel architecture

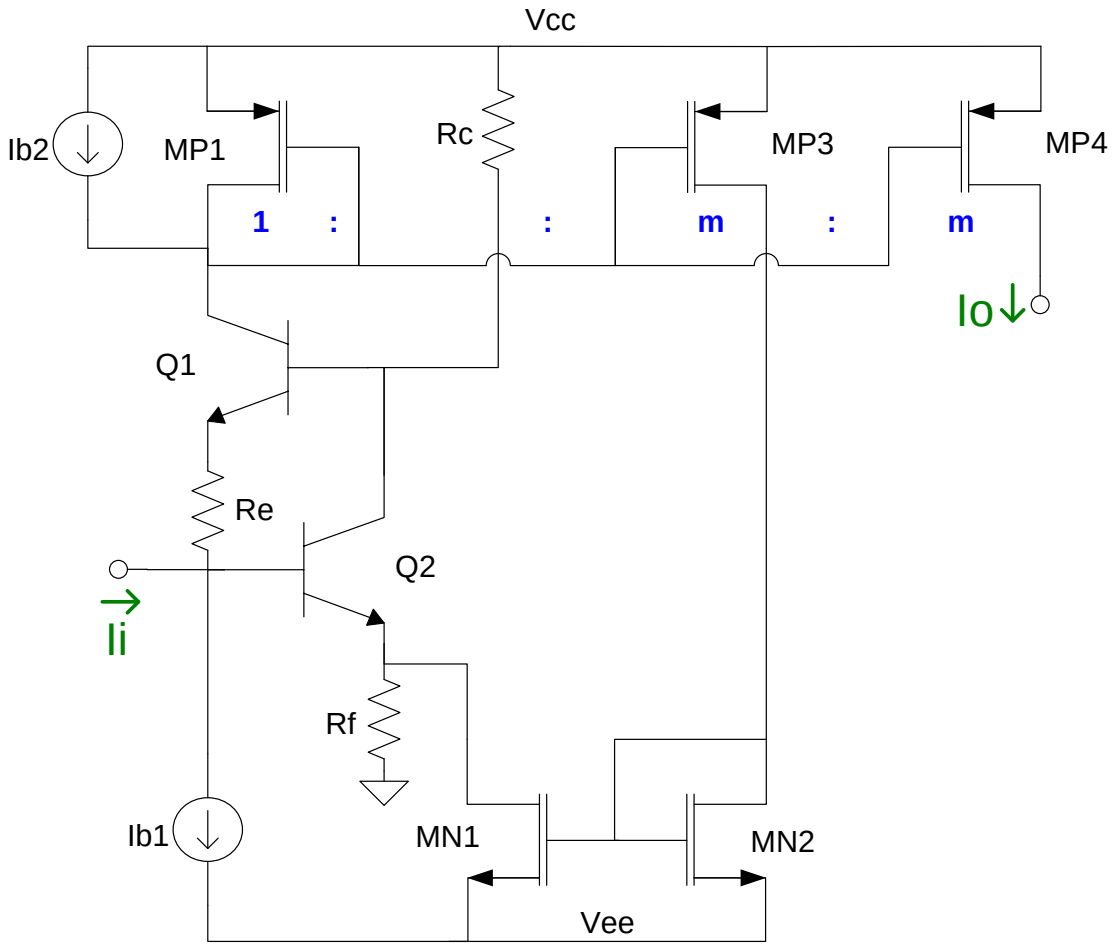
- Current mode amplifier
- Switched integrator
  - Fully differential Op Amp
- Track and hold
  - ADC has already got one, really needed?
- Multiplexer
- ADC driver
  - Depends on ADC input impedance: resistive or capacitive ?



III. Key components: amplifier: current output / mixed feedback

- Mixed mode feedback:
  - Inner loop: lower input impedance
    - Voltage feedback (gain): Q2 and Rc
  - Outer loop: control input impedance
    - Current feedback: mirrors and Rf
- Variation of LAr preamplifier
- Current gain: m
- Input impedance

$$Z_i \approx \frac{1/g_{m1} + Re}{g_{m2} Rc} + mR_f$$

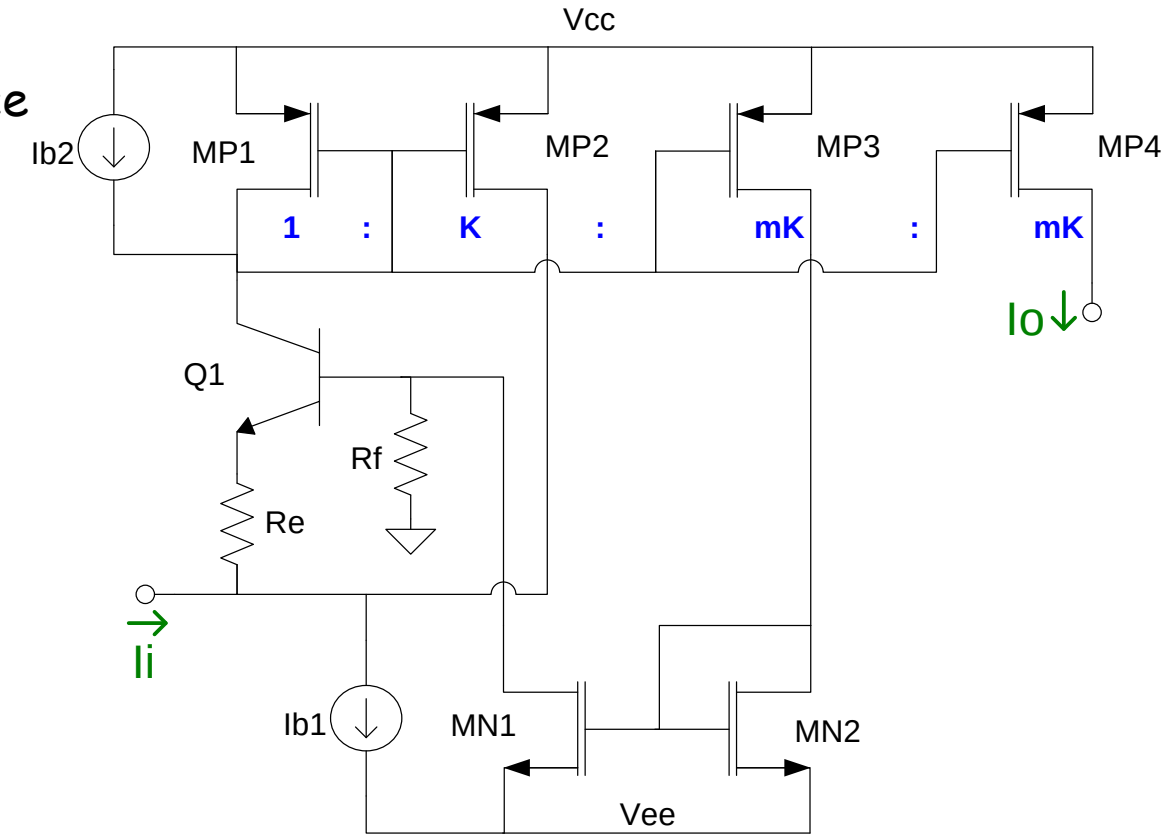


III. Key components: amplifier: current output / current feedback

- Current mode feedback:
  - Inner loop: lower input impedance
    - Current feedback (gain): mirror: K
  - Outer loop: control input impedance
    - Current feedback: mirror: m
- Current gain: m
- Input impedance

$$Z_i \approx \frac{1/g_{m1} + \mathrm{Re}}{1+K} + \frac{K}{1+K} m R_f$$

- Current mode feedback
  - Optical comunications
  - SiPM readout
- Better in terms of ESD:
  - No input pad connected to any transistor gate or base



III. Key components: low noise amplifier

- First simulations of current amplifiers are promising but:
  - Z_{in}=50 Ω for full dynamic and BW=100 MHz
  - Noise: 400 μV rms after integration and pedestal subtraction
  - Linearity of the current mirrors must be better than 1 %
    - Trade off: linearity / BW / noise
- Test key issues of input amplifier:
- First estimate of the effect of mismatch
- Methods to compensate process variation to be included in next coming prototypes

III. Summary

- To be prototype in June's run:
  - Low noise current amplifier:
    - Basic schemes
  - Integrator:
    - High GBW fully differential OpAmp
      - See Edu's talk
      - Could be used in other stages

- To be tested in future runs:
  - Compensation of process variation of amplifier's input impedance
  - Track and hold (if needed)
  - Analogue multiplexer
  - ADC driver
    - ADC needs to be characterized
  - Common blocks:
    - Clock generation
    - Biasing (CMOS band gap already exists)