Laboratoire de l'Accélérateur Linéaire (IN2P3-CNRS) Orsay, France

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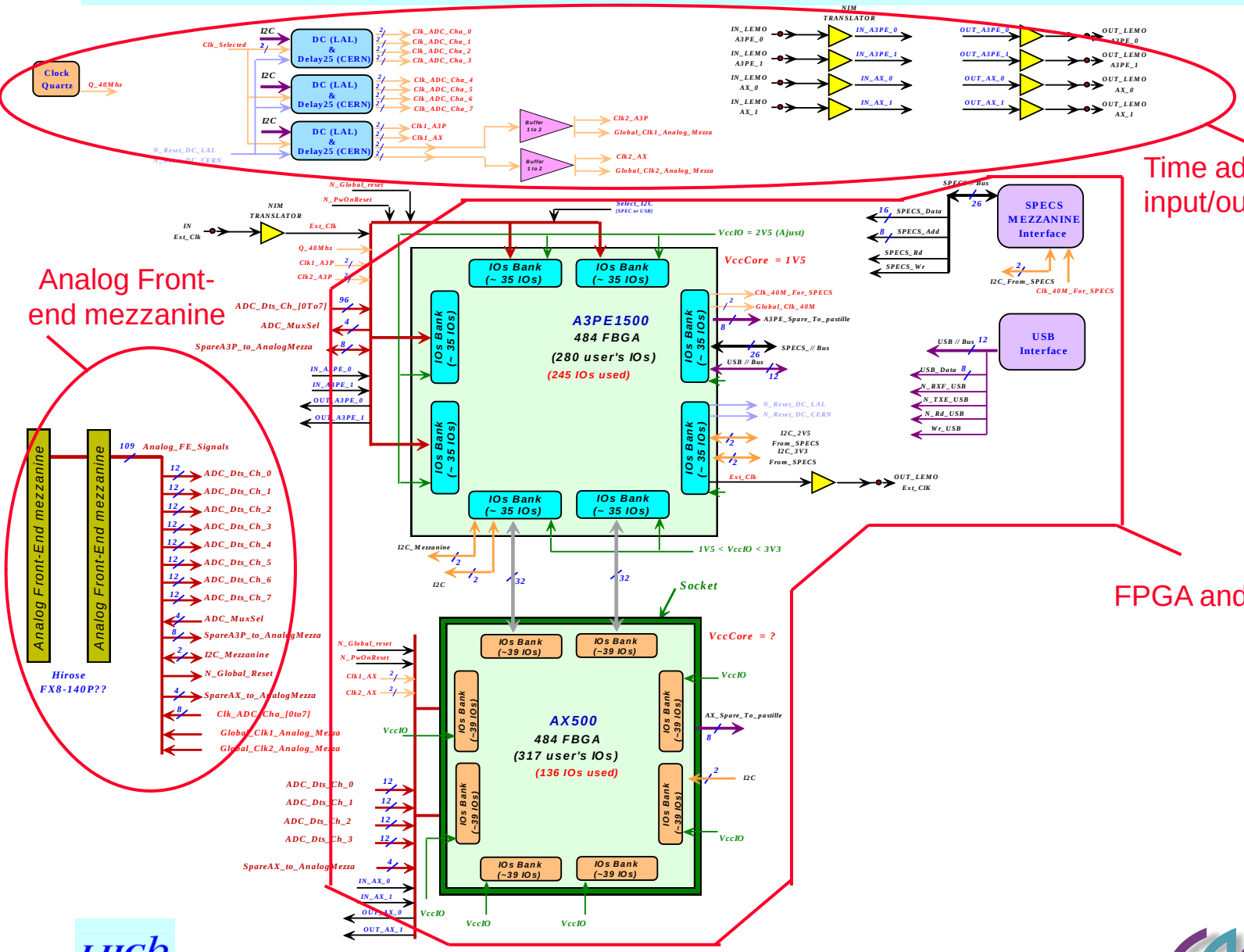
Tests Front-end card Status

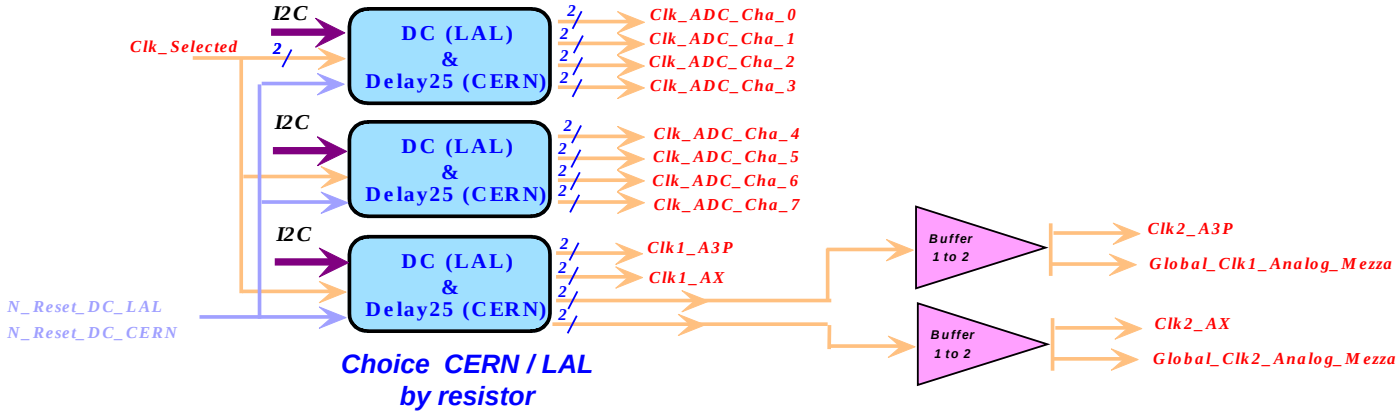
- **Recall of the architecture of the card**
  - Time adjustment , Analog Front-end mezzanine, FPGA and Interfaces, power supply, Clock Tree.
  - Layout of the board.
- **Recall of the firmware blocks**
  - USB interface module
  - Clock divider and L0 generator module for Lemo outputs
  - Processing ADC data
  - Trigger processing
  - Data storage
  - Test value injection RAM
- **Preliminary tests**
  - Power supply, download A3PE1500, Rd/wr by USB
- **Firmware status and tests schedule**

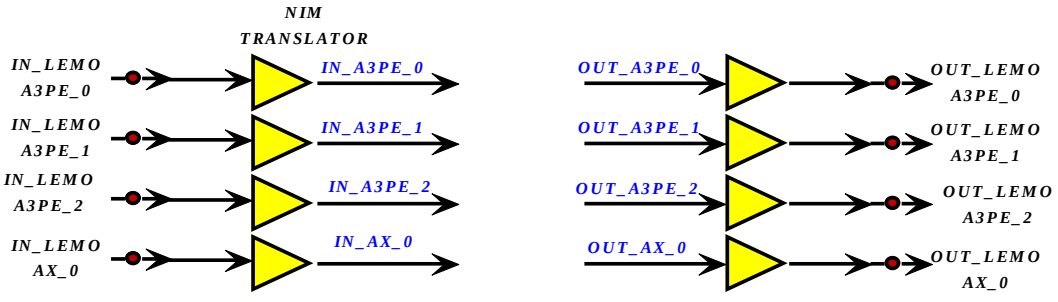
Tests board architecture



Time adjustment with delay chip and Input/Output (LEMO)

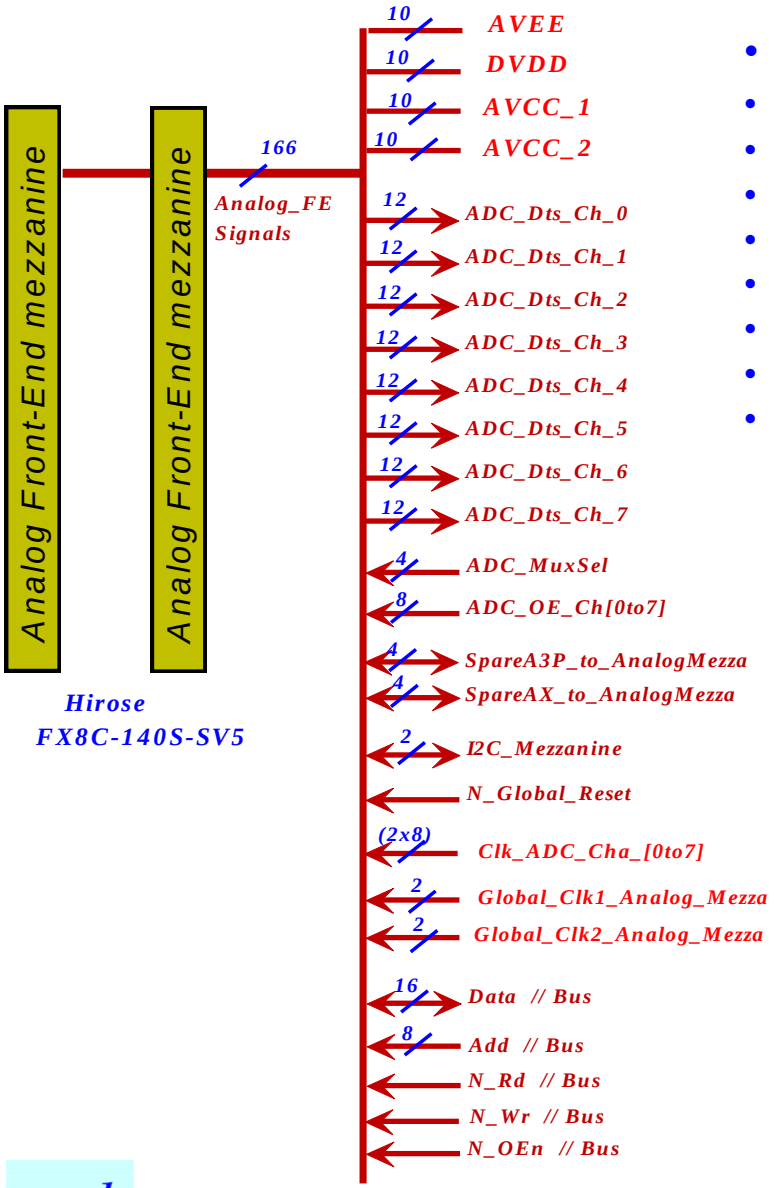
More information on the clock tree slide !



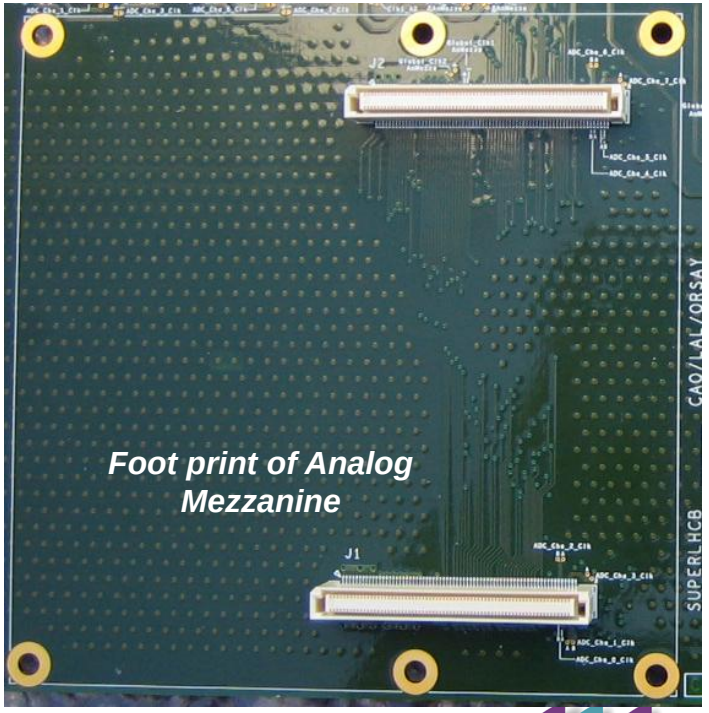


- 3 Inputs (NIM translator) for A3PE FPGA
- 3 Outputs (NIM translator) for A3PE FPGA
- 1 Input (NIM translator) for AX FPGA
- 1 Output (NIM translator) for AX FPGA
- 1 Input Ext_Clk (NIM translator) for A3PE
- 1 Output Ext_Clk (NIM translator) for A3PE

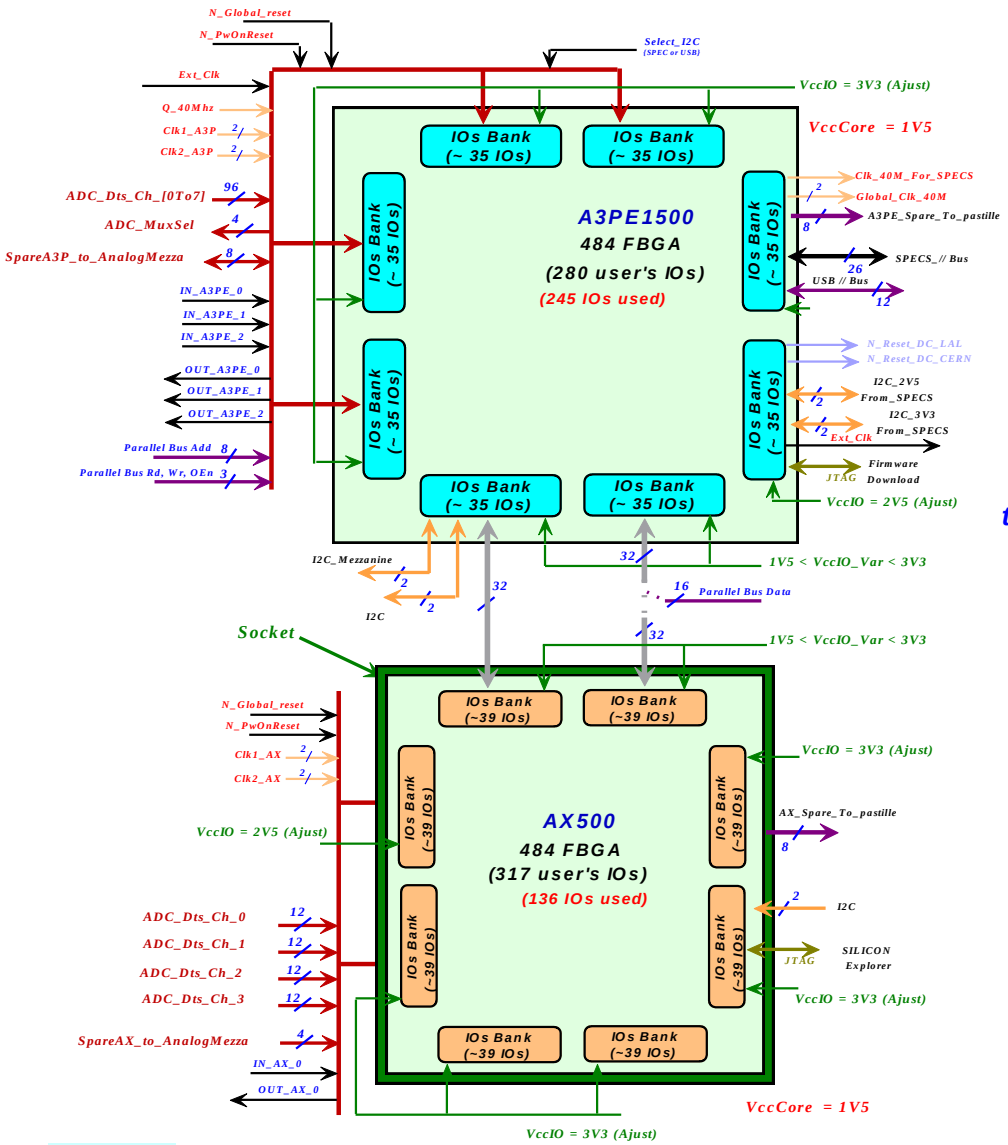
Analog Front-end mezzanine

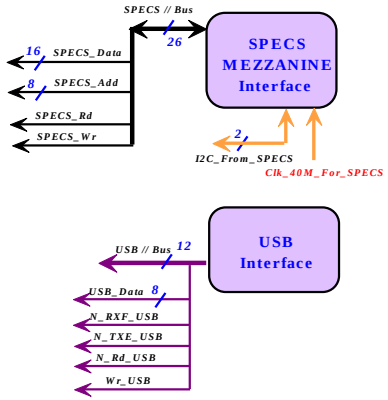


- 8 x {ADC_Data Channel (12b)}
- 8 x {Clk for ADC_Data Channel (LVDS)}
- 2 x Global Clk (LVDS)
- 4 Spare for A3PE
- 4 Spare for AX500
- I2C
- Reset
- Parallel Bus
- AVEE, DVDD, AVCC_1, AVCC_2



FPGA and Interfaces



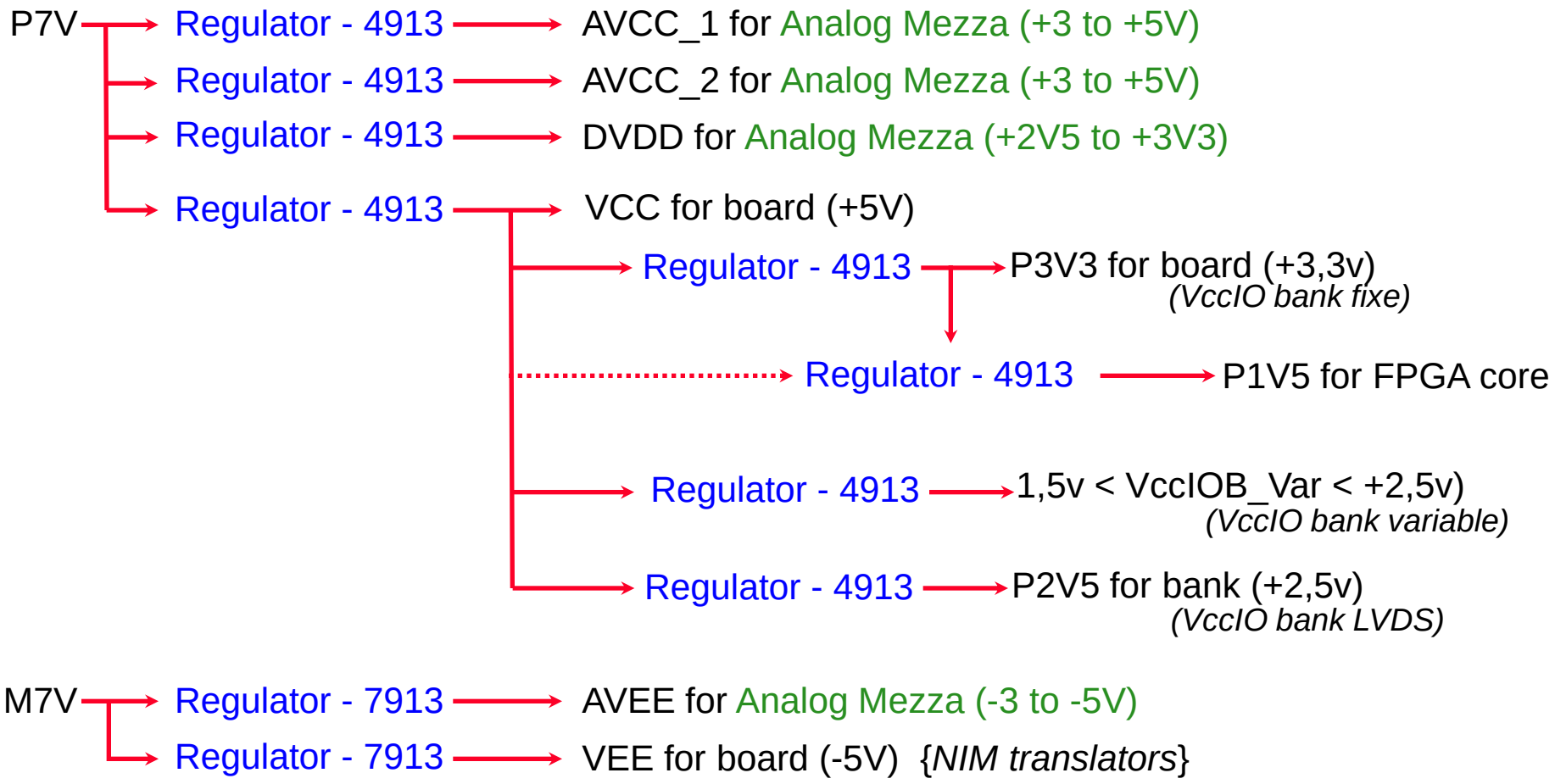


FPGA and Interfaces

Flash Pro 4 to be used to programming A3PE device

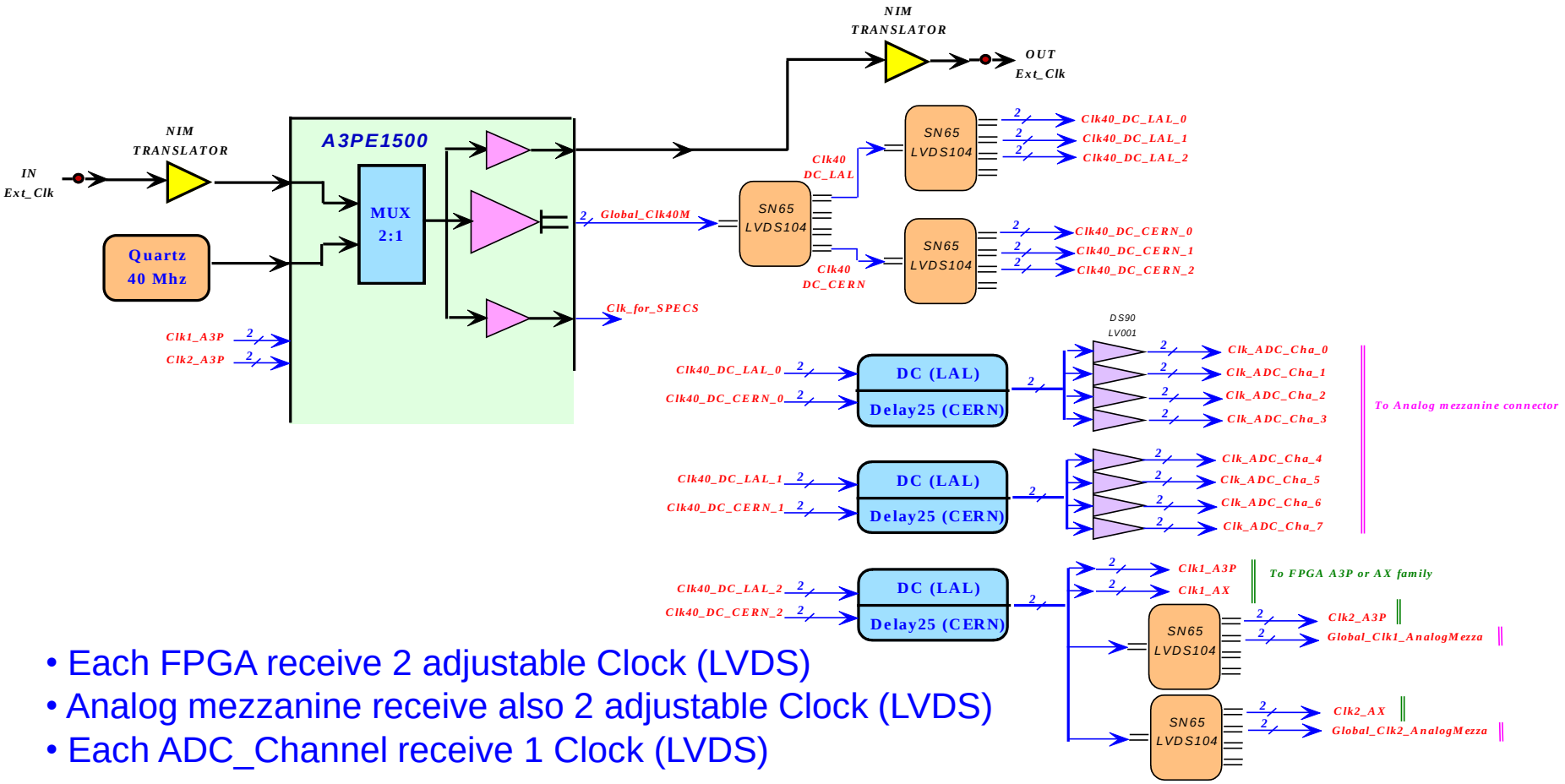
- A3PE1500
- AX500 (socket)
- SPECS and USB Interface through A3PE
- I2C Interface from A3PE to AX
- JTAG download for A3PE
- JTAG for AX : Silicon Explorer

Tests board power supply



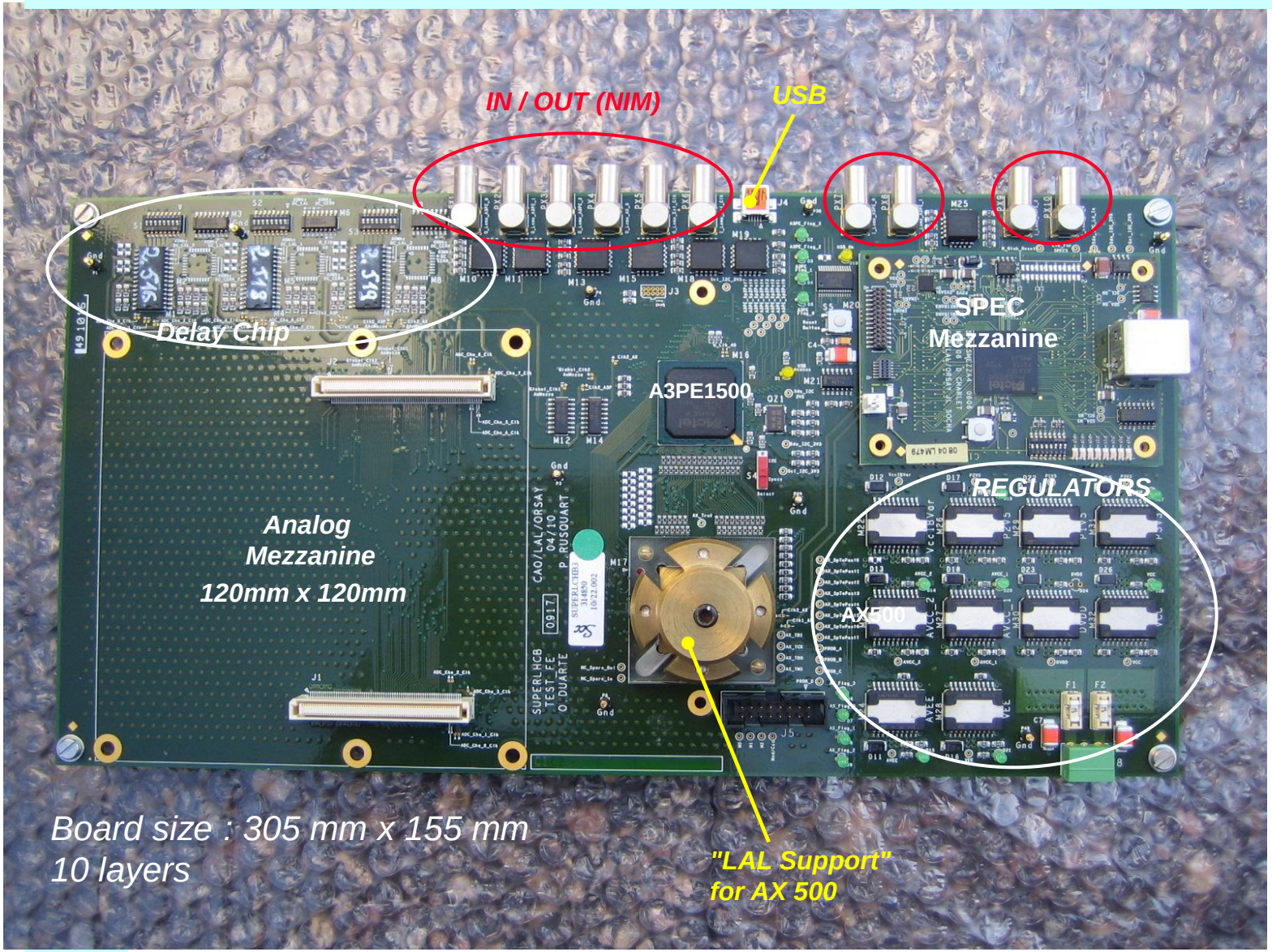
- ***Lab. Power Supply input (+/- 7V)***
- ***10 Radiation tolerance regulators ! !***

Tests board Clock Tree

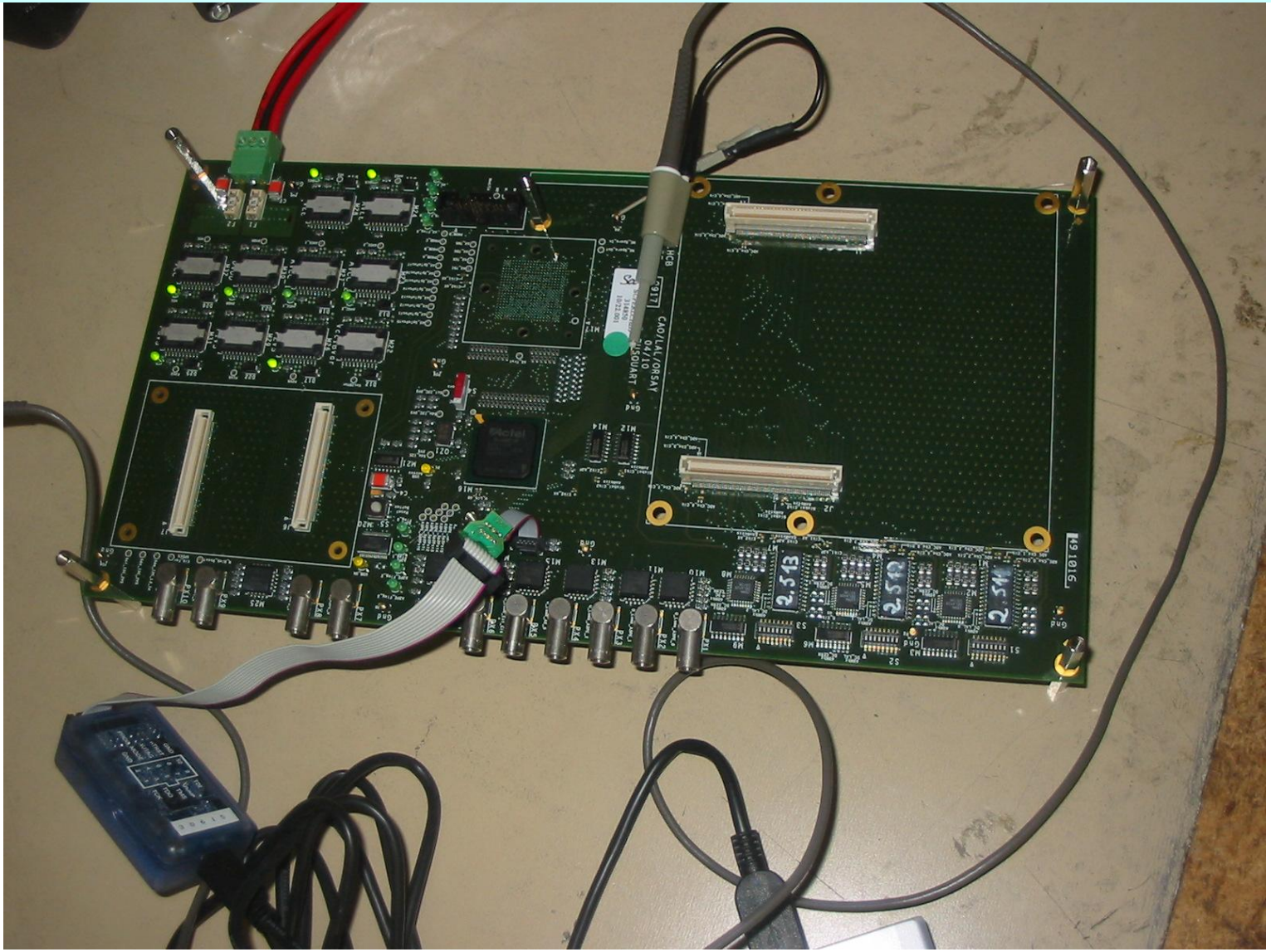


- Each FPGA receive 2 adjustable Clock (LVDS)
- Analog mezzanine receive also 2 adjustable Clock (LVDS)
- Each ADC_Channel receive 1 Clock (LVDS)

Layout of the board



Test FE Board



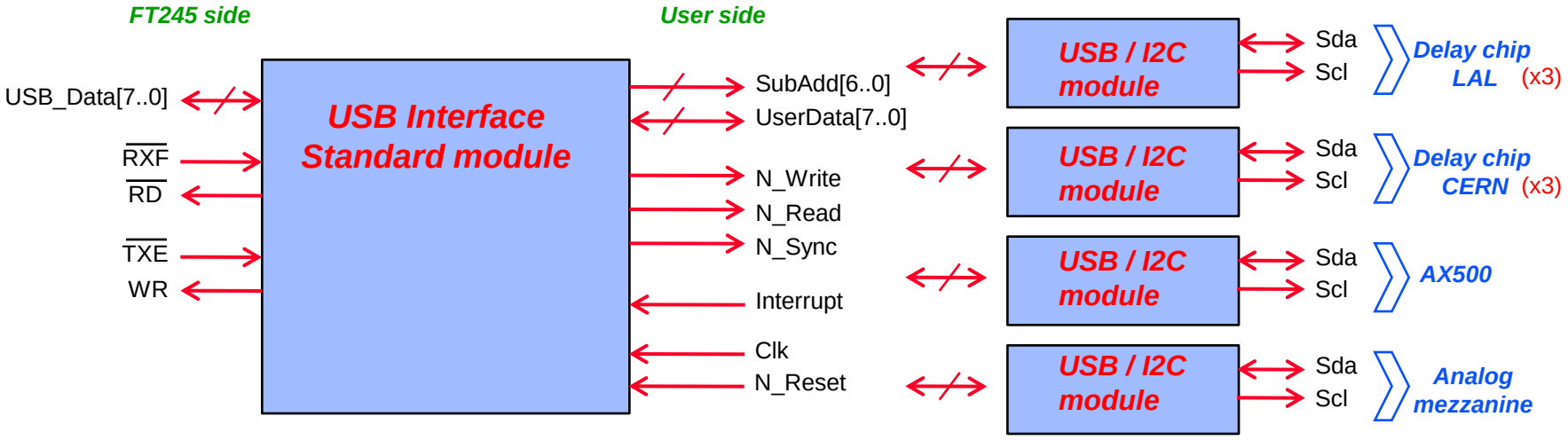
Recall of the firmware blocks

All Blocks inside A3PE1500 in Verilog language

- **USB interface module** *(Jihane's code)*
- **Clock divider and trigger generator module for Lemo outputs**
  (according Olivier's code APA300 for CROC)
- **Processing ADC data** *(according Christophe's code AX250)*
- ~~**Trigger processing**~~
- **Data storage**
- **Test value injection RAM**

A3PE firmware blocks : USB interface module

- **USB interface module**
  - **USB Interface standard module**
  - **I2C modules (x4)**

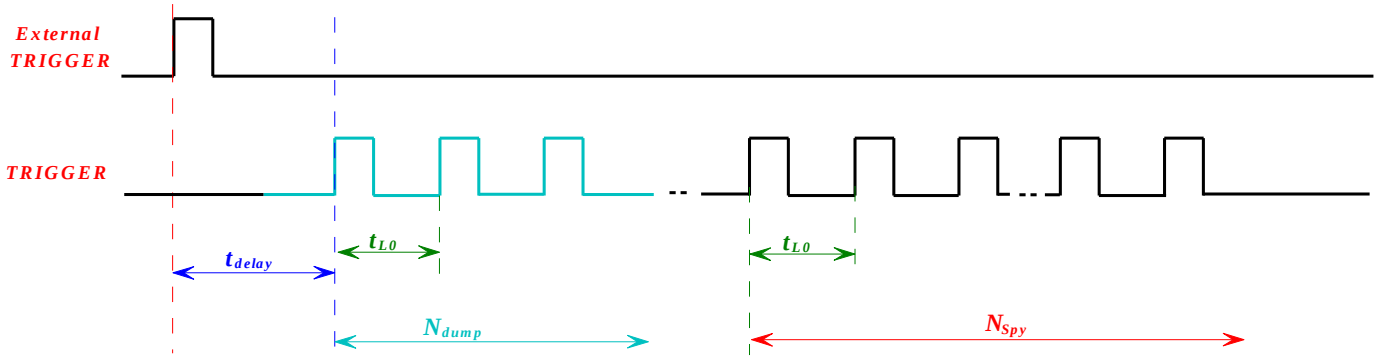


A3PE firmware blocks : Clock divider and trigger generator

- **Clock divider**
  - **50 ns to 0.4s (24 bits counter)**

- **Internal Trigger**

With this module we can produce trigger (external trigger or software command)



Registers loaded by USB or SPECS :
- Tdelay (8bits)
- TL0 (16 bits)

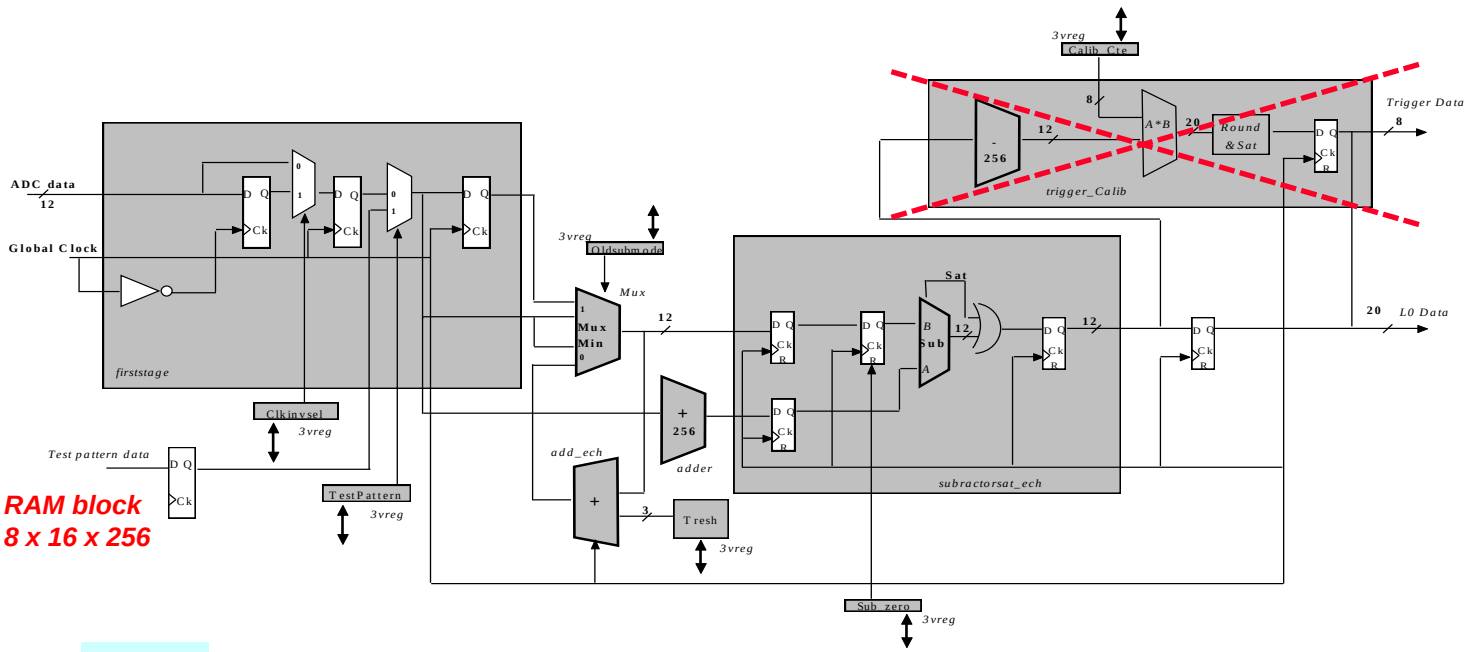
Registers loaded by USB or SPECS :
- Ndump (8bits)
- Nspy (8 bits)

A3PE firmware blocks : data processing

- **Processing ADC data**
  - **Re-synchronize ADC input**
  - **Dynamique pedestal subtraction**
    - **Suppression of low frequency noise**
- **Trigger processing**
  - **Convert ADC data to 8 bit**
  - **Sent towards the TRIG-PGA**

FE_Pga

L0 and trigger data processing part : Module Subtract
4 Clock cycles Input to Output



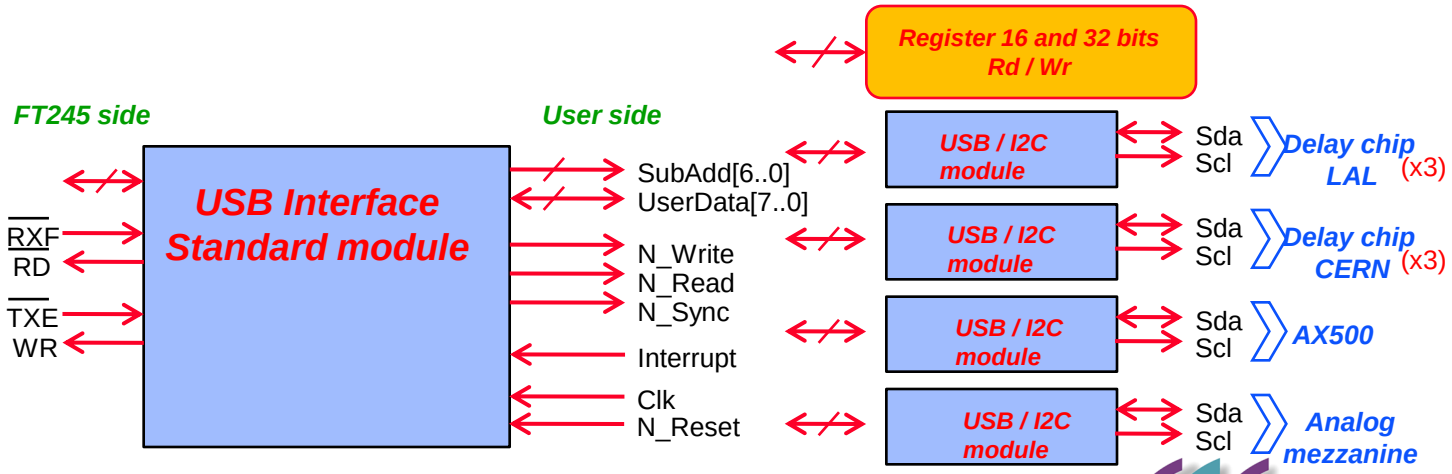
A3PE firmware blocks : RAM

- **Data storage (output buffer) before readout**
  - **8 x 16 (12 used) x 256**
  - **Read only by USB (first !)**
- **Test value injection RAM**
  - **8 x 16 (12 used) x 256**
  - **Use of the RAM test describ in LHCb ECAL/ HCAL Front-End card**

There exist different ways to use the RAM test:
- The standard one: the RAM address is increased every 25ns by the clock and the sequence of 256 addresses is initiated by the test-sequence signal, originating in the calibration command of the channel B and enabled by the corresponding status of an I2C register. The sequence ends up after 256 clock cycles.
- A variant with an enable loop bit loaded by I2C. In this case after the sequence initialisation the RAM address counter continues advancing and jumps automatically from address 255 to address 0.
- The L0 mode where the RAM address is incremented upon reception of each L0. The sequence can be terminated at 255 or looped as in case 2.
- Calibration mode where the RAM address is incremented upon reception of test sequence command. In this case by definition the system will loop after address 255.

Preliminary tests

- **Power supply** *ok*
  (AVcc_1, AVcc_2, AVee, ….)
- **Download A3PE1500**
  - **A3P family require FlashPro 3 or 4 (new product !)**
  - **Problem with FlashPro Consol** *debug in progress with Actel*
    (“failed to load the programming file” {stp files})
- **Rd / Wr register by USB inside A3P**
  - **USB interface Standard simulation** *ok*
  - **Used “test_245” by Chafik**
  - **Tests with 16 and 32 bits Rd/Wr register inside A3PE1500** *to do*

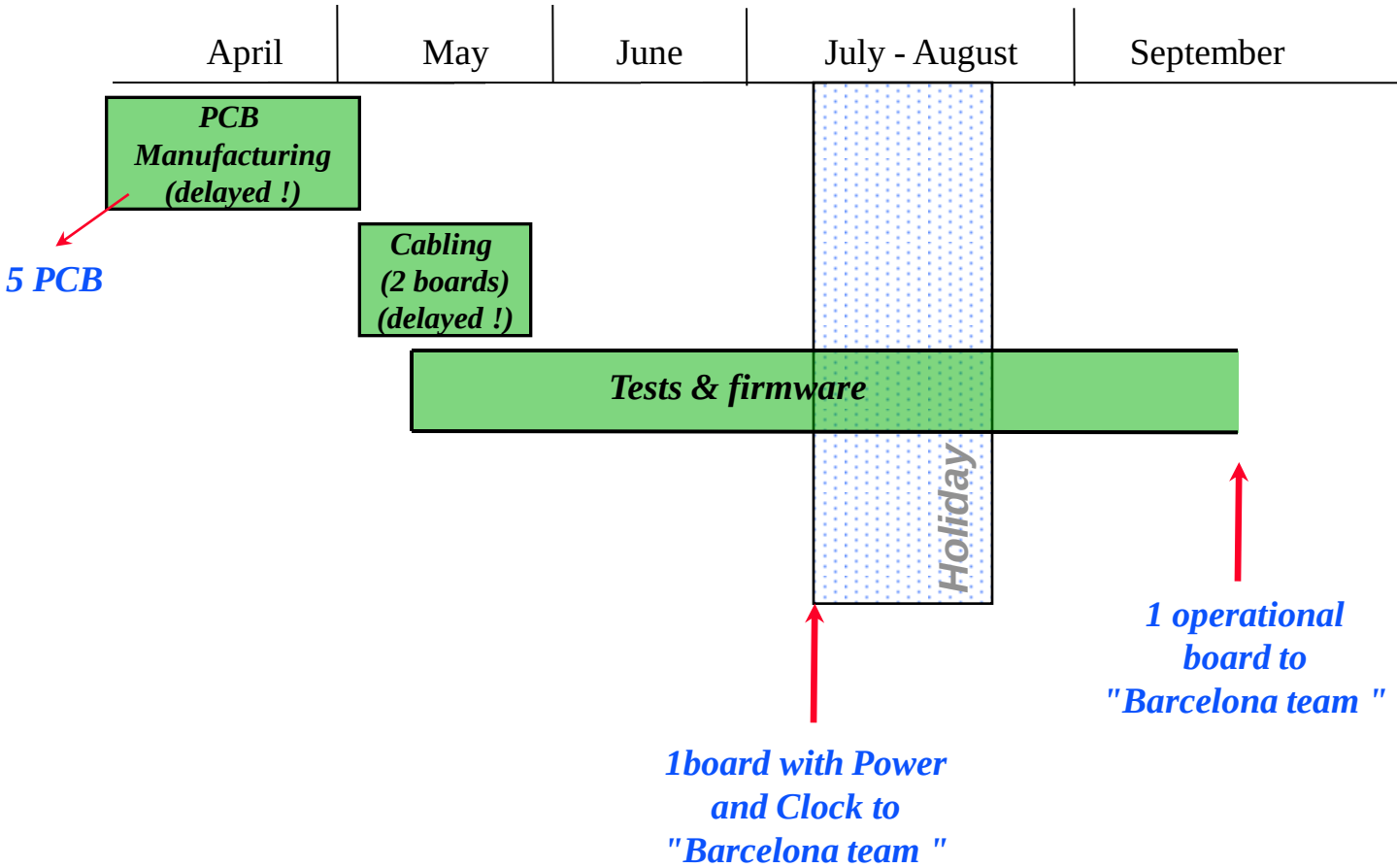


Status of the firmware blocks

- **USB interface module** *(in progress Jihane + Olivier)*
- **Clock divider and trigger generator module for Lemo outputs** *(to adapt from the CROC by Olivier)*
- **Processing ADC data** *(in progress by Christophe)*
- **Data storage** *(to do)*
- **Test value injection RAM** *(to do)*

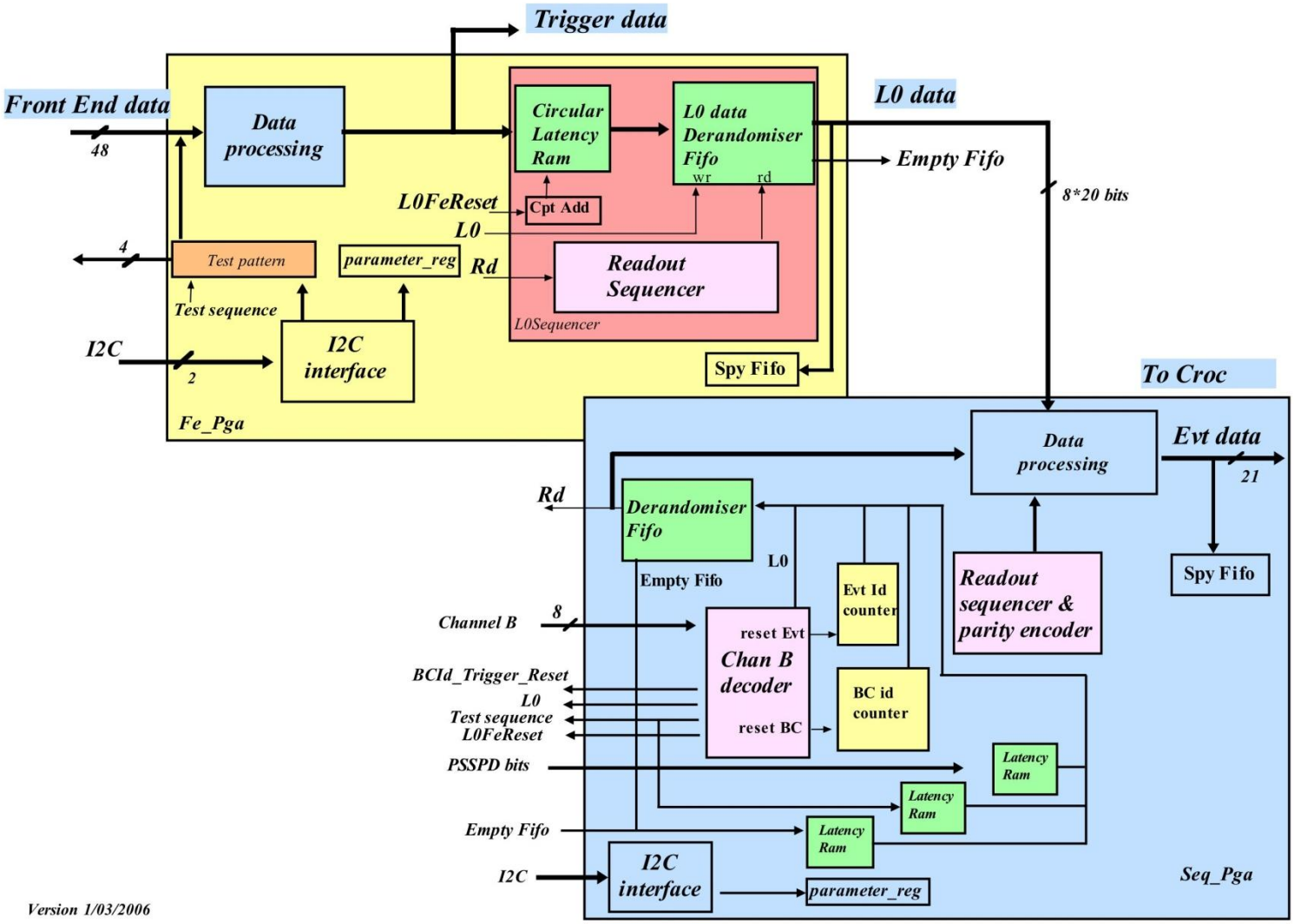
All Blocks inside A3PE1500 in Verilog language

Tests schedule (optimistic !)

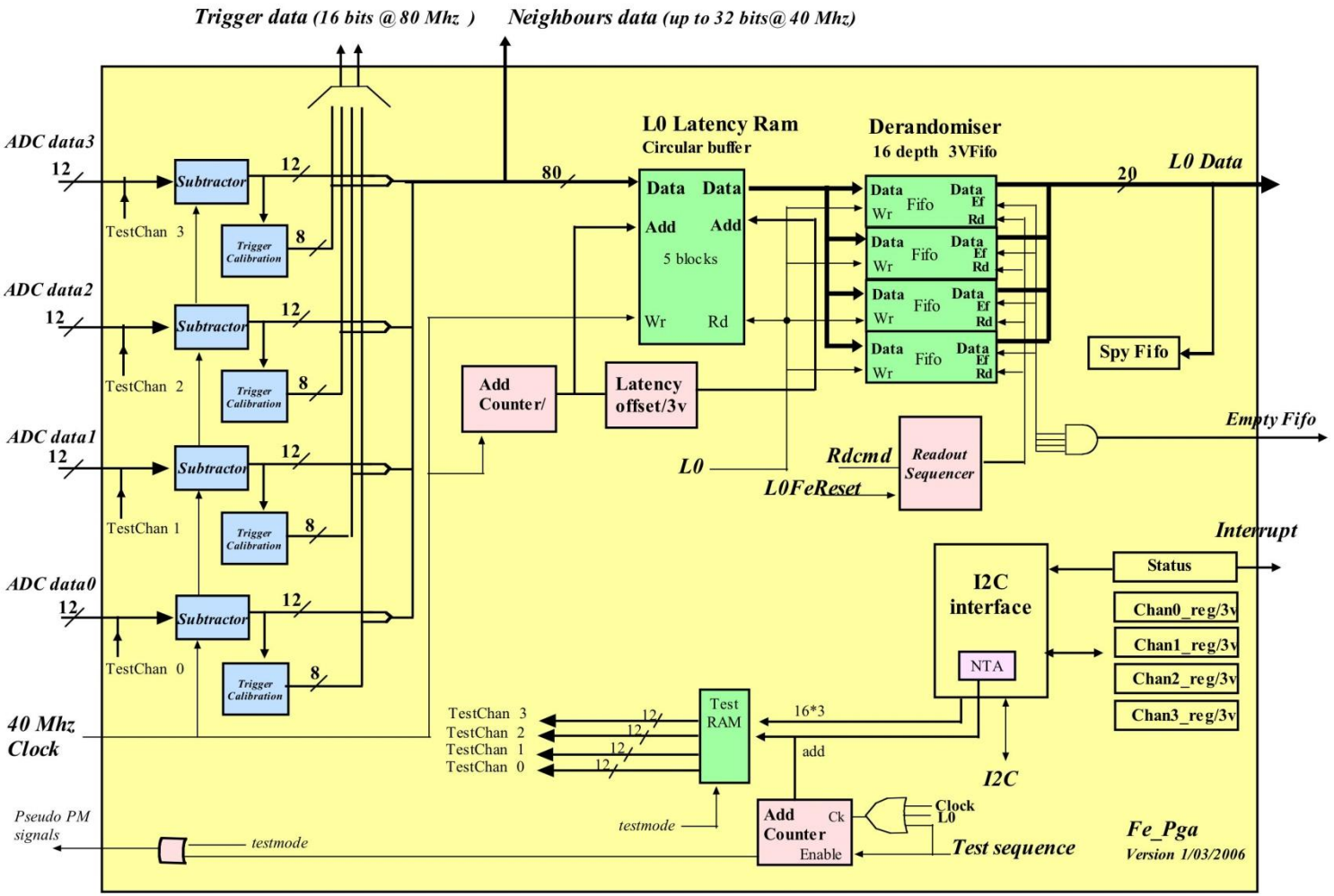


Nbre de PCB

SPARE


Trigger data
Front End data
48
Data processing
Circular Latency Ram
L0 data Derandomiser Fifo
wr
rd
L0 data
Empty Fifo
8*20 bits
L0FeReset
Cpt Add
L0
4
Test pattern
parameter_reg
Rd
Readout Sequencer
L0Sequencer
Test sequence
I2C
I2C interface
2
Spy Fifo
Fe_Pga
To Croc
Data processing
Evt data
21
Rd
Derandomiser Fifo
L0
Empty Fifo
Evt Id counter
Readout sequencer & parity encoder
Spy Fifo
Channel B
8
reset Evt
Chan B decoder
BCId_Trigger_Reset
L0
Test sequence
L0FeReset
reset BC
BC id counter
PSSPD bits
Latency Ram
Latency Ram
Empty Fifo
Latency Ram
I2C
I2C interface
parameter_reg
Seq_Pga
Version 1/03/2006

SPARE


Trigger data (16 bits @ 80 Mhz)
Neighbours data (up to 32 bits@ 40 Mhz)
ADC data3
ADC data2
ADC data1
ADC data0
12
Subtractor
TestChan 3
TestChan 2
TestChan 1
TestChan 0
Trigger Calibration
8
80
L0 Latency Ram
Circular buffer
Data
Add
5 blocks
Wr
Rd
Derandomiser
16 depth 3VFifo
Fifo
Ef
Rd
20
L0 Data
Spy Fifo
Add Counter/
Latency offset/3v
L0
L0FeReset
Rdcmd
Readout Sequencer
Empty Fifo
Interrupt
I2C interface
Status
Chan0_reg/3v
Chan1_reg/3v
Chan2_reg/3v
Chan3_reg/3v
NTA
16*3
add
I2C
Test RAM
testmode
Add Counter
Ck
Enable
Clock L0
Test sequence
40 Mhz Clock
Pseudo PM signals
Fe_Pga
Version 1/03/2006

SPARE

FE_Pga

L0 and trigger data processing part : Module Subtract

4 Clock cycles Input to Output