Calorimeter Upgrade Meeting

Analog Electronics
COTS design

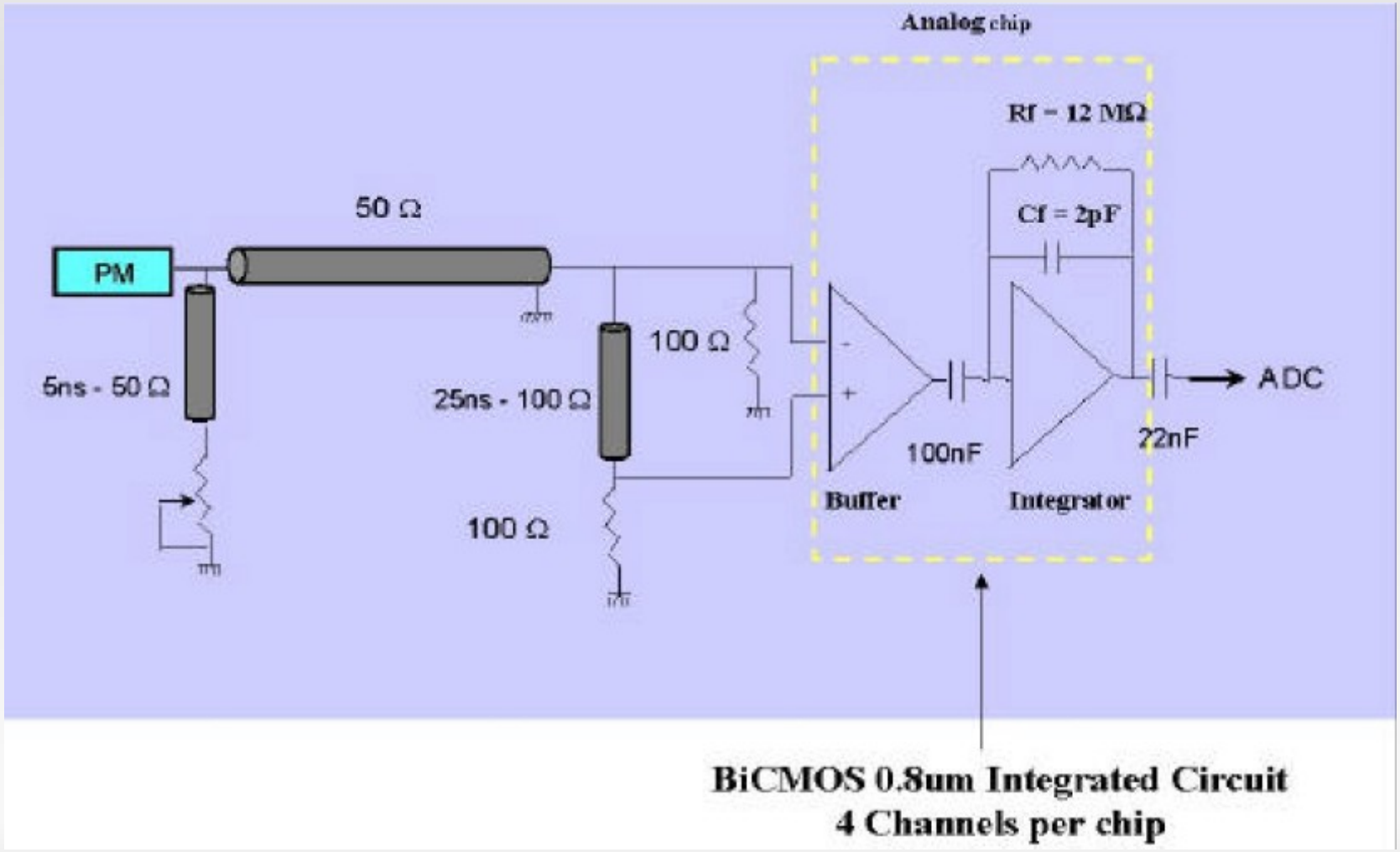
22/jun/2010

Main ideas of COTS

- Commercial Off The Shelf
  - Intended to be cheaper than ASIC
  - Easy to find
  - Commercially tested, no risk of mistakes in chip design
  - Much faster and easyer design and test
  - Not the same integration level
  - Not the same flexibility
  - Not the same performance

Current CALO reminder

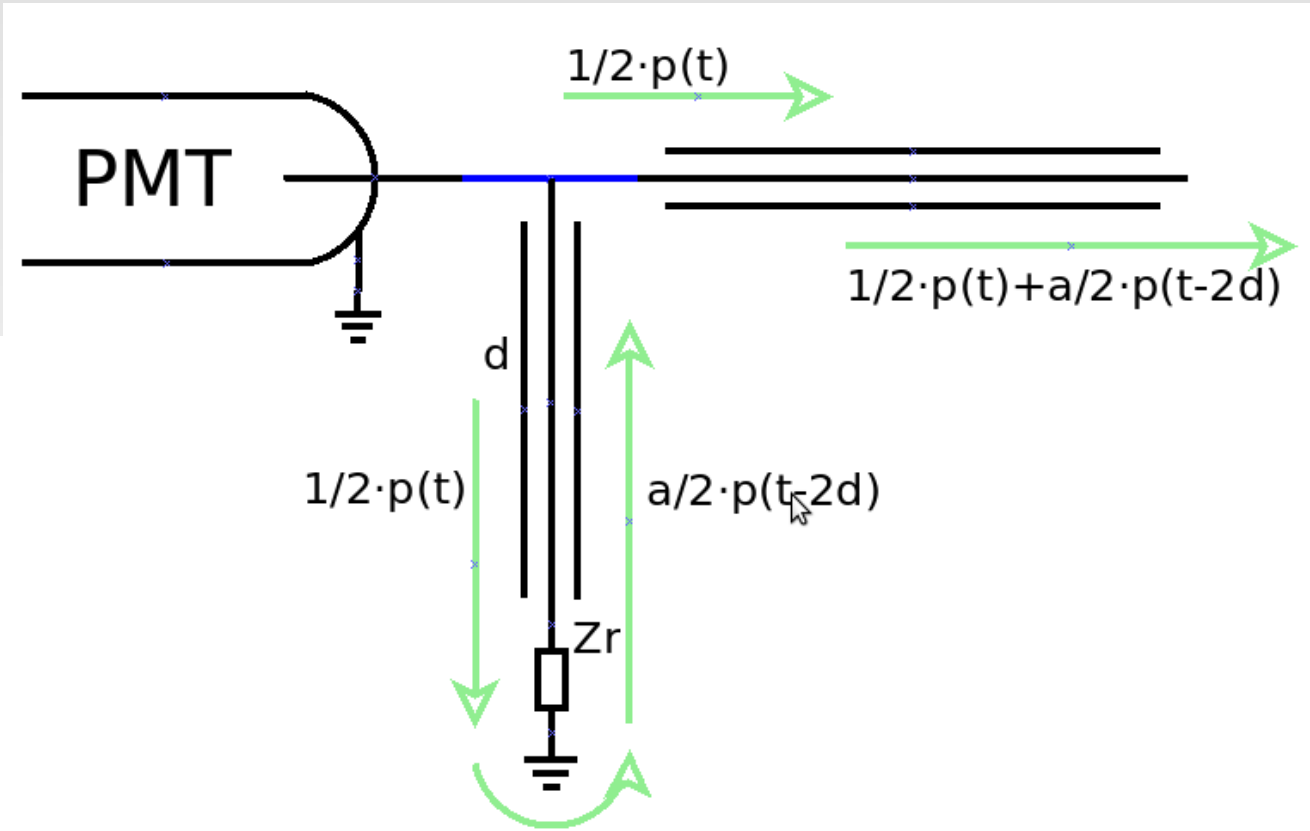
- Current CALO scheme [1]

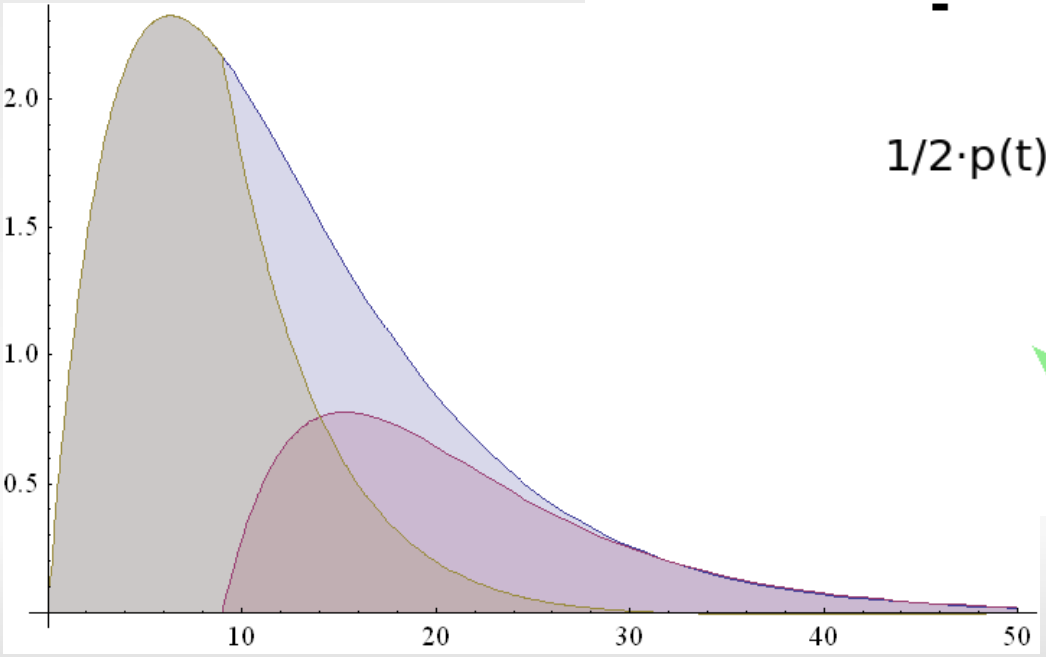


[1] LHCb Calorimeter TDR (CERN-LHCC-2000-036)

Current CALO reminder

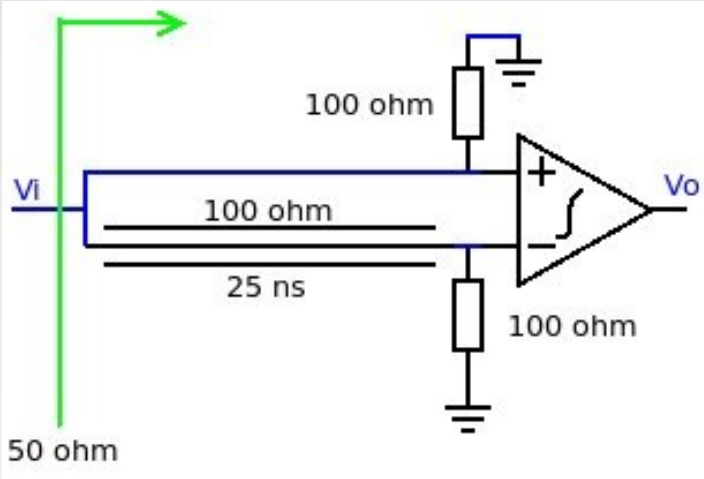
- Clipping with delay lines
  - In the PMT Base

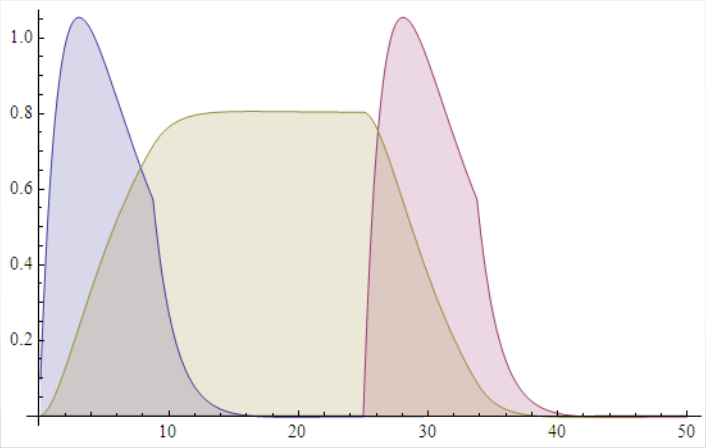


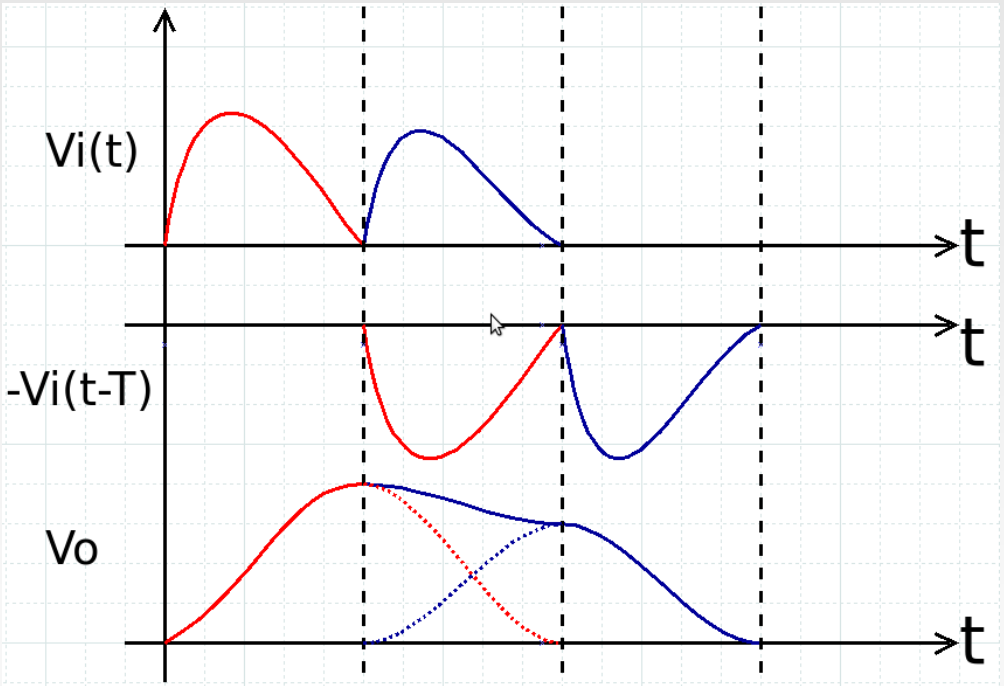


Current CALO reminder

- Integration
  - Delayed Lines Integrator



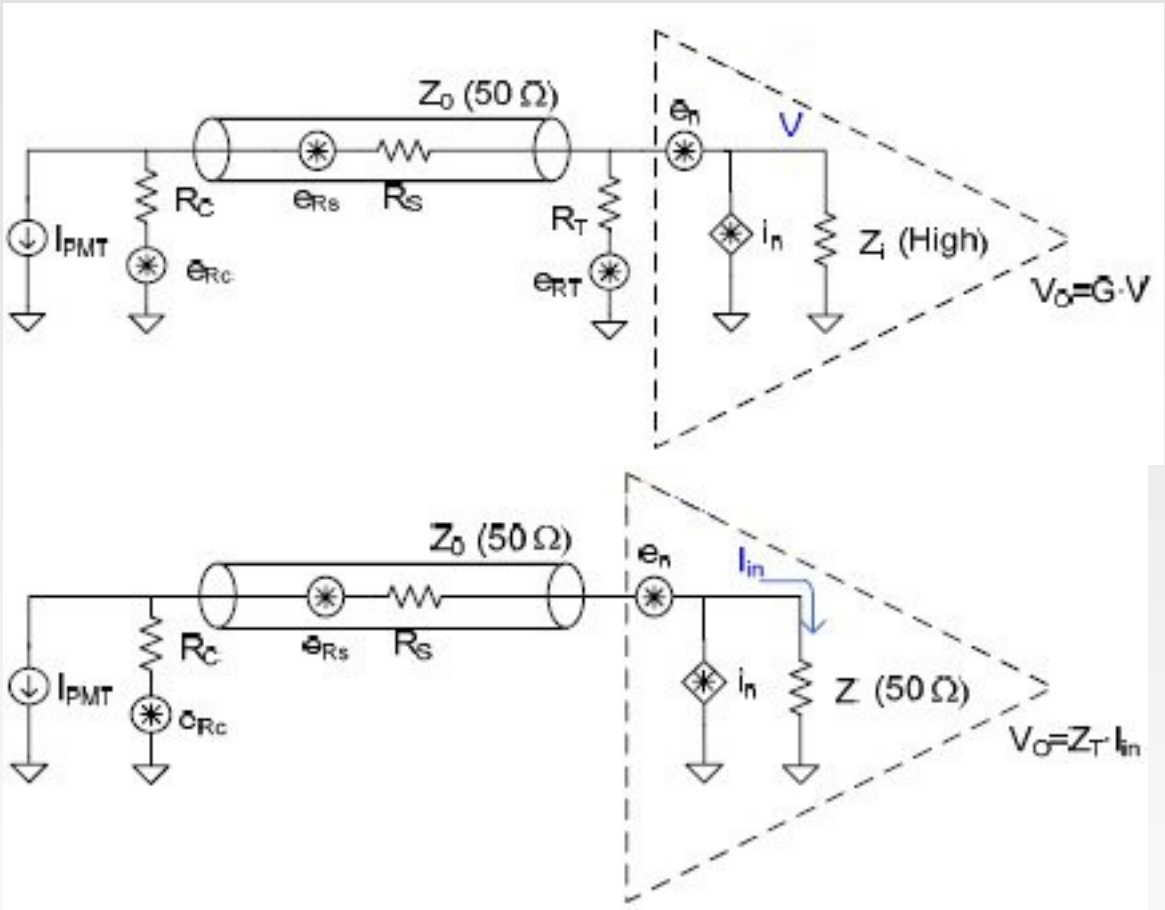




Noise Problematic

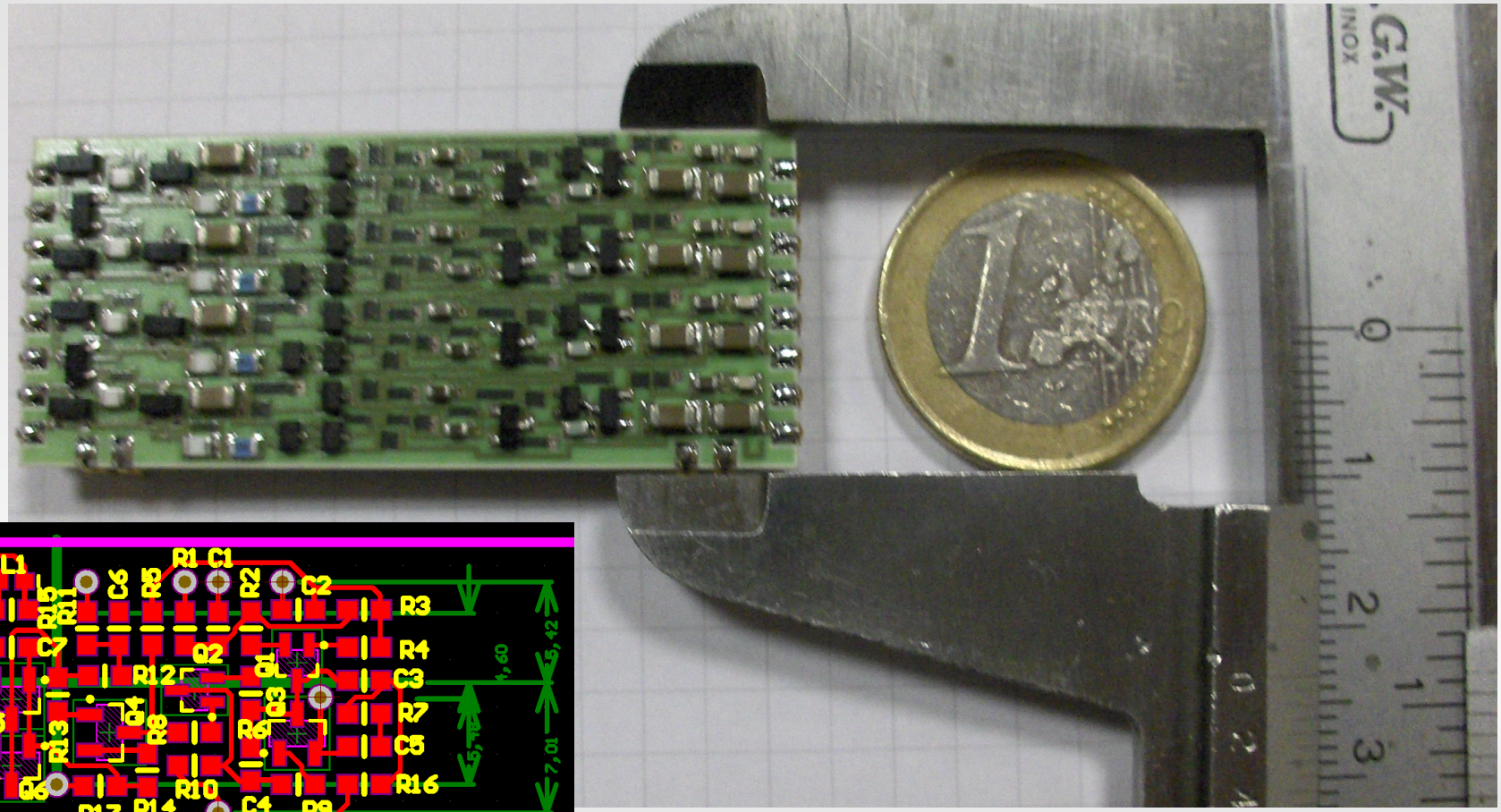
- Reducing the gain in the PMTs → less signal and same noise!
- Low noise needed
- Difficult with COTS
- Noise in the

  PMT base



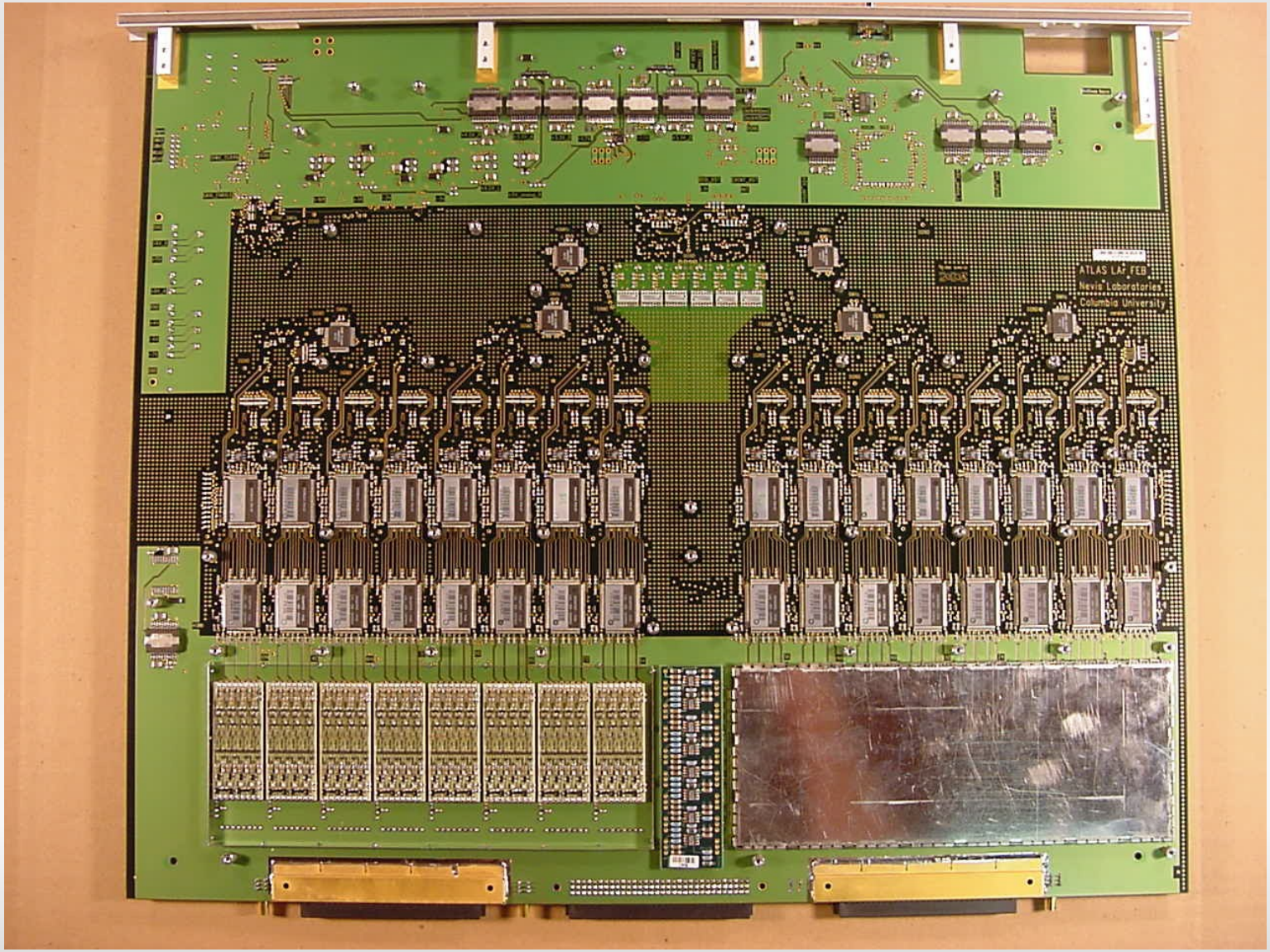
Possible Solutions with COTS

- Super Common Based Amplifier
- ATLAS LAr CALO uses one of those (4 chan)



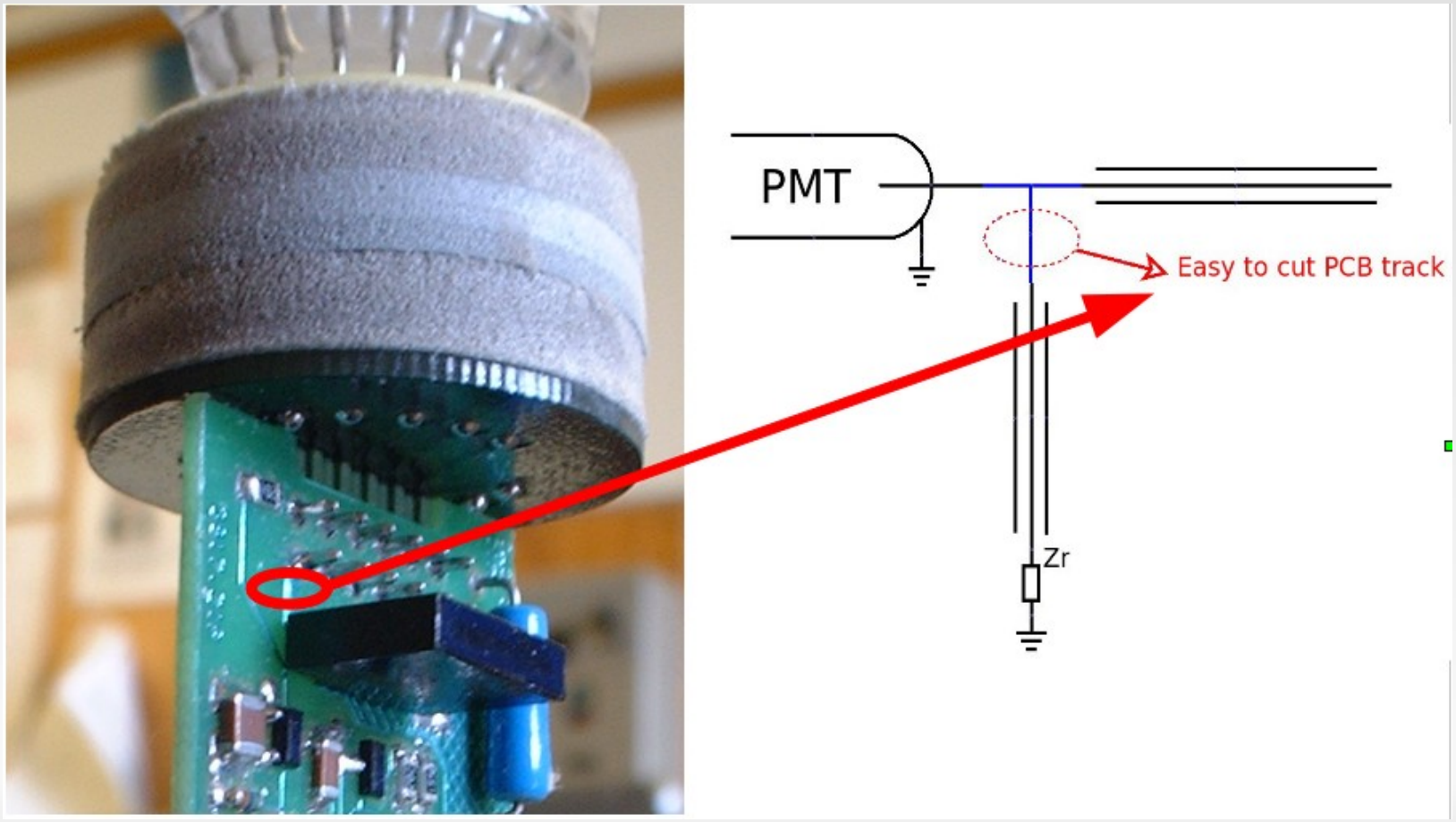
Possible Solutions with COTS

- Space is not an issue (LAr Calo Board)



Possible Solutions with COTS

- Manipulate the PMT's base to reduce noise

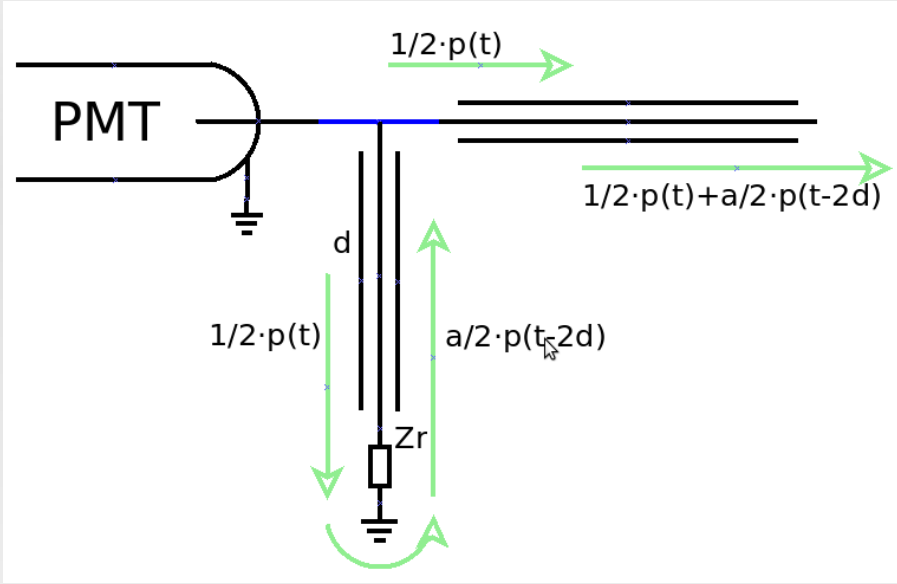


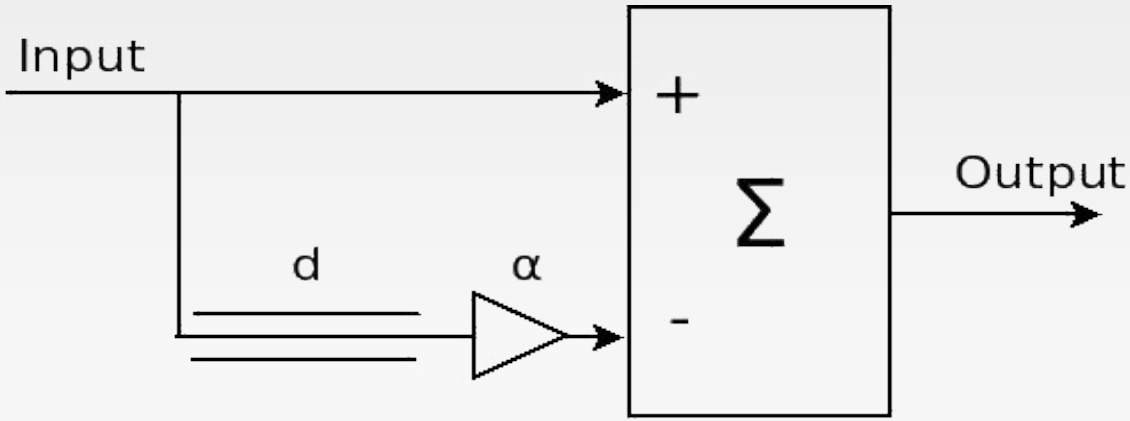
Possible Solutions with COTS

- Manipulate the PMT's base to reduce noise and relax system specifications
  - The resistor in the PMT's base has some contribution to noise, we could get rid of it.
  - Clipping in the base reduces useful signal, we would remove it.
  - With greater signal the signal/noise ratio would increase.

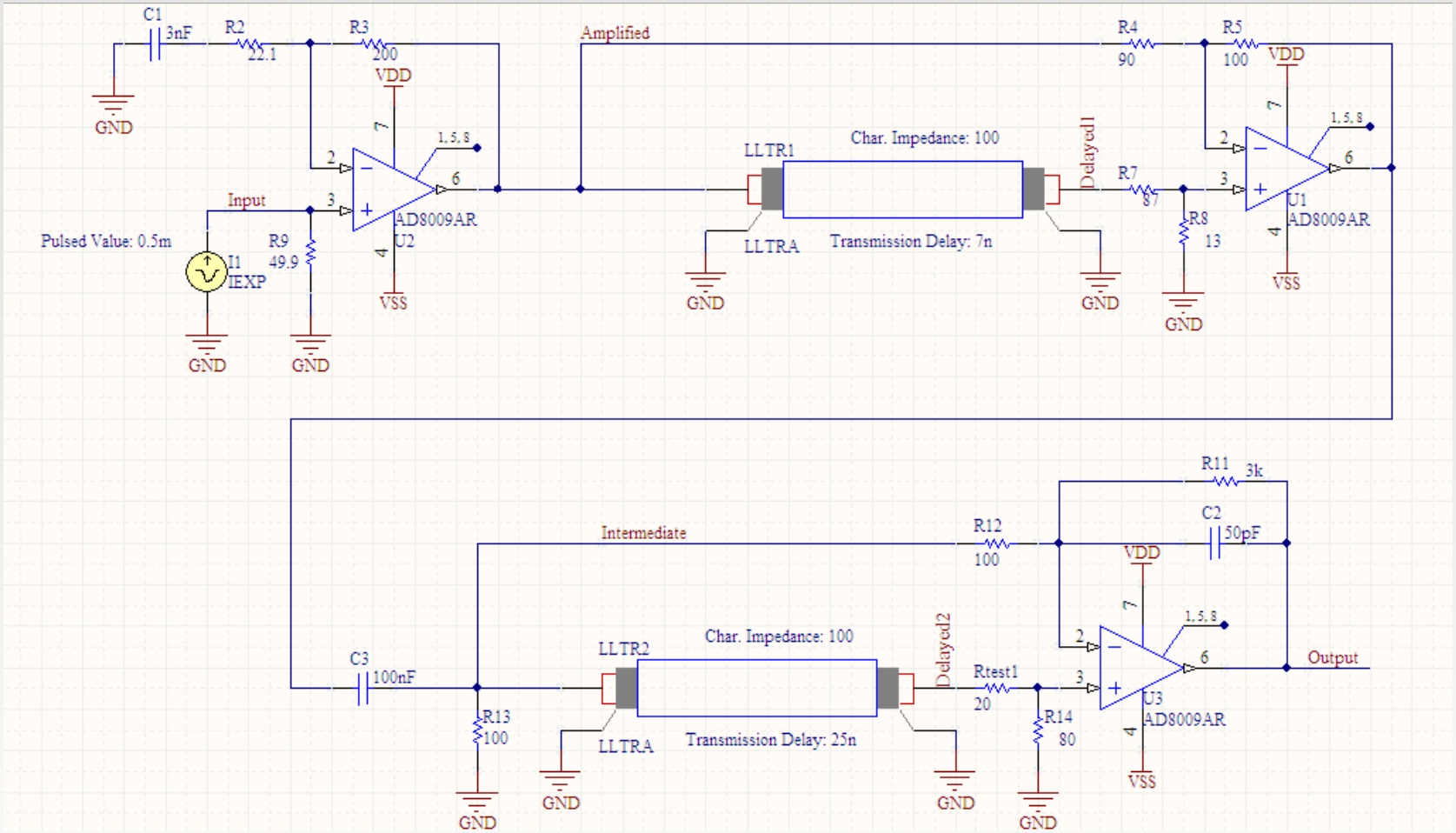
Different Clipping Approach

- Clipping after amplifying → Impedance problem...
- Equivalent system found, same impulse response but no impedance problems.





Studied Architectures (I)



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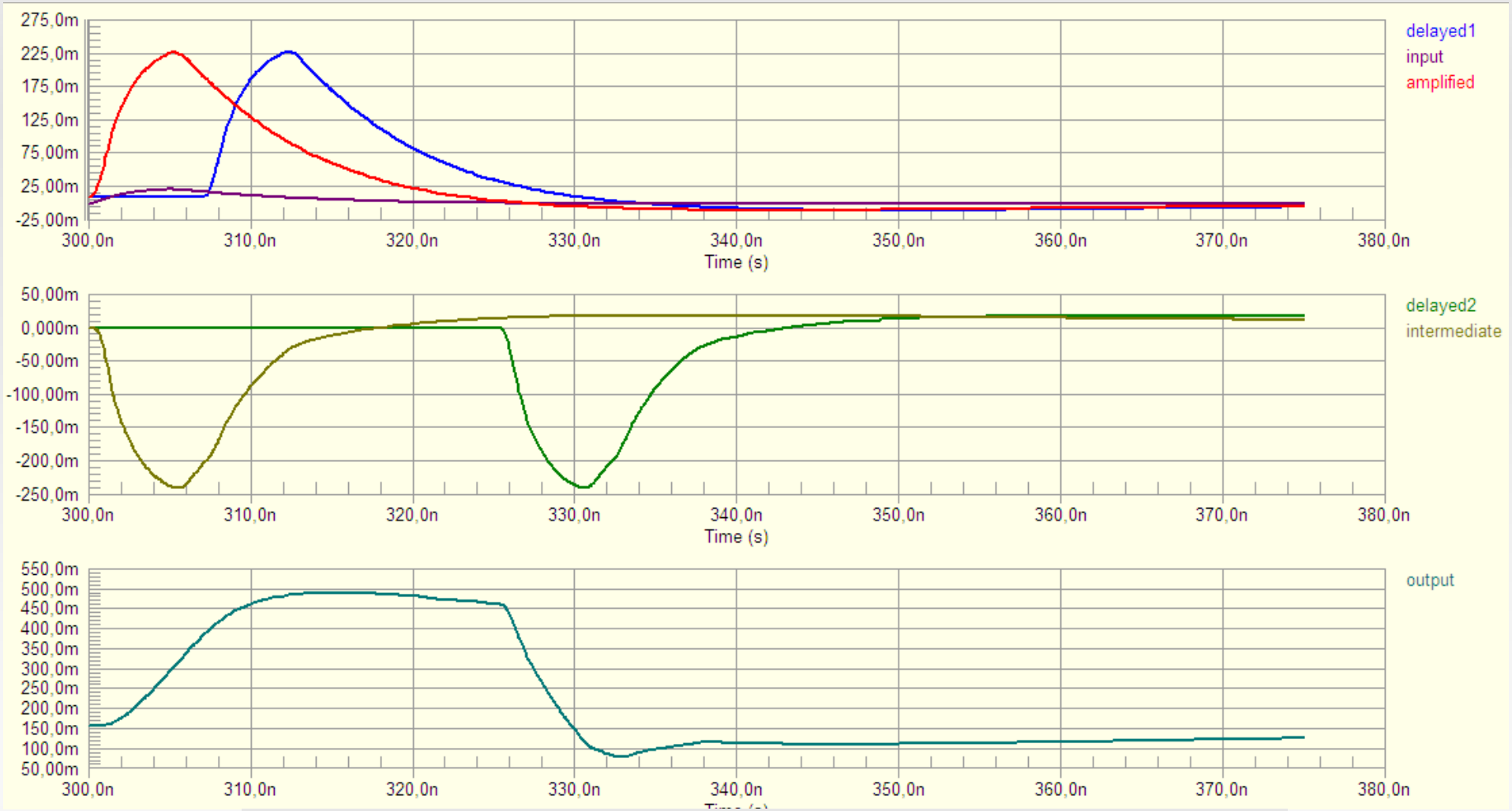
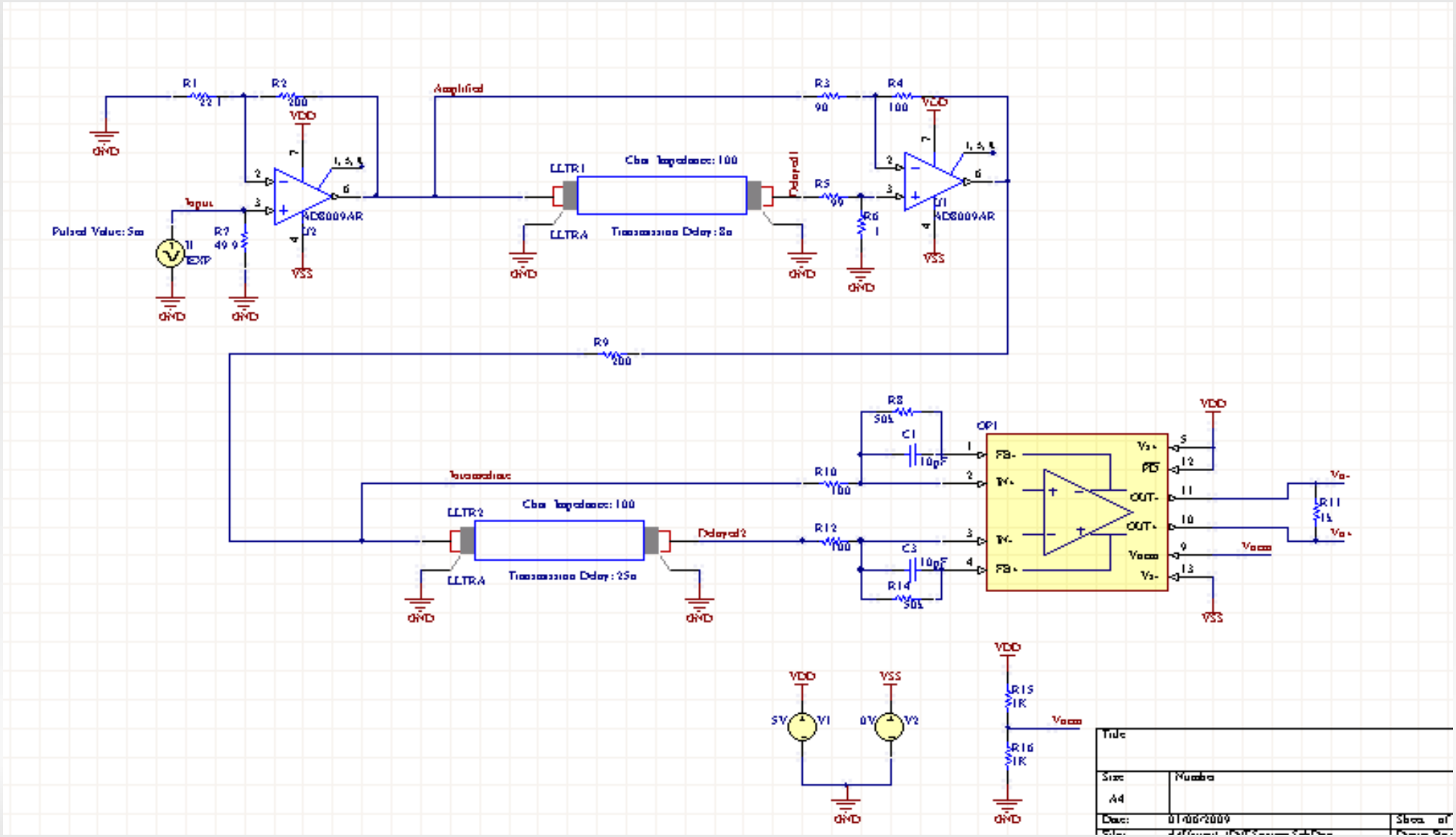


$$Output = \frac{1}{\tau}\int (Intermediate - Delayed2)\,dt + Delayed2$$

Studied Architectures (II)

- Scheme with Differential operational amplifier



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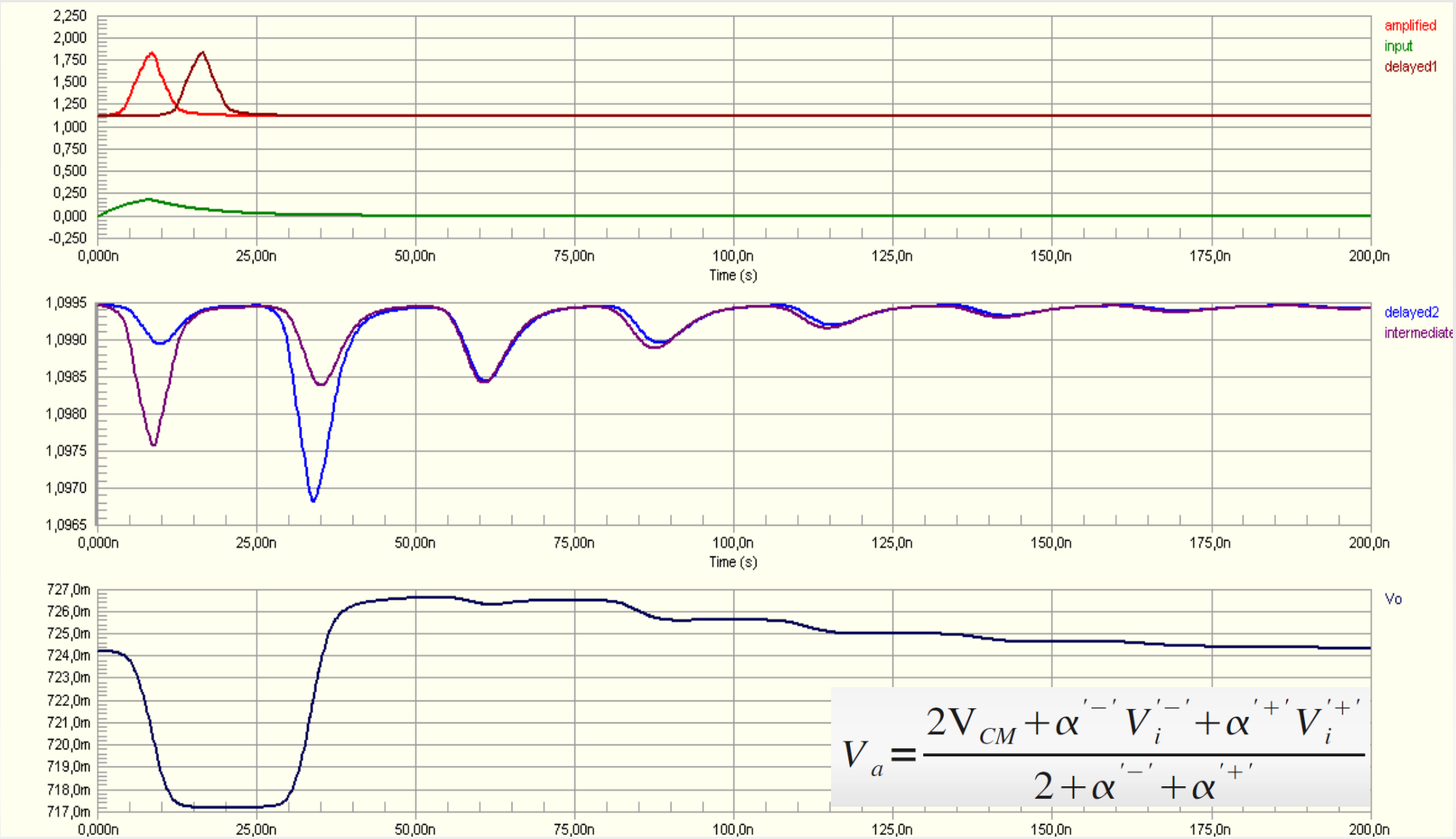
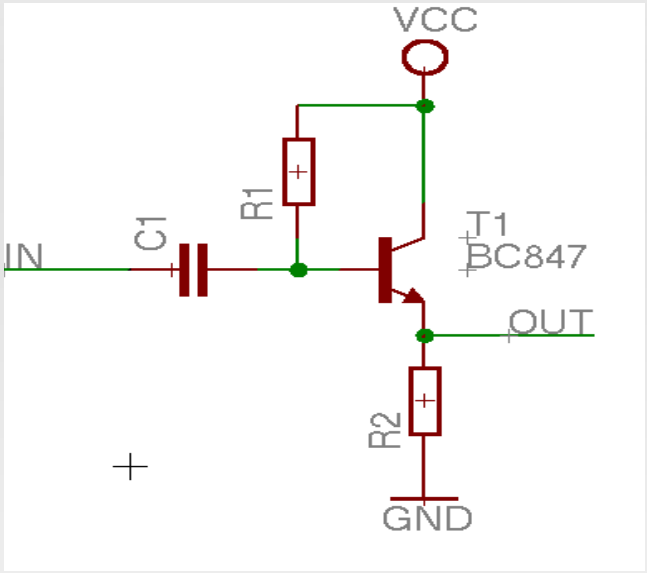
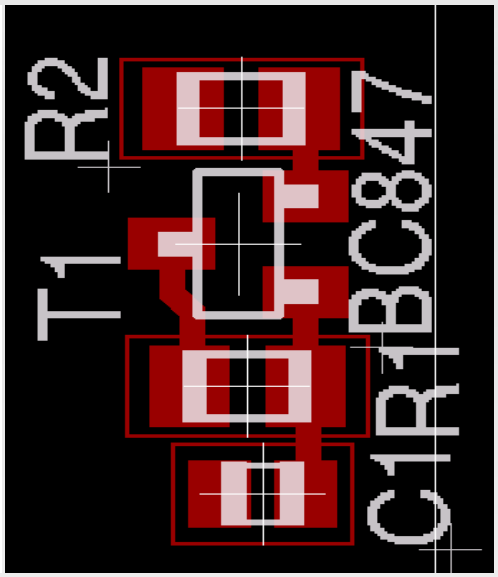


Studied Architectures (II)

- Schematic of the adaptation system





- Equations of the system

$$Z_B = R_B \| (r_d + R_L)(hfe + 1)$$

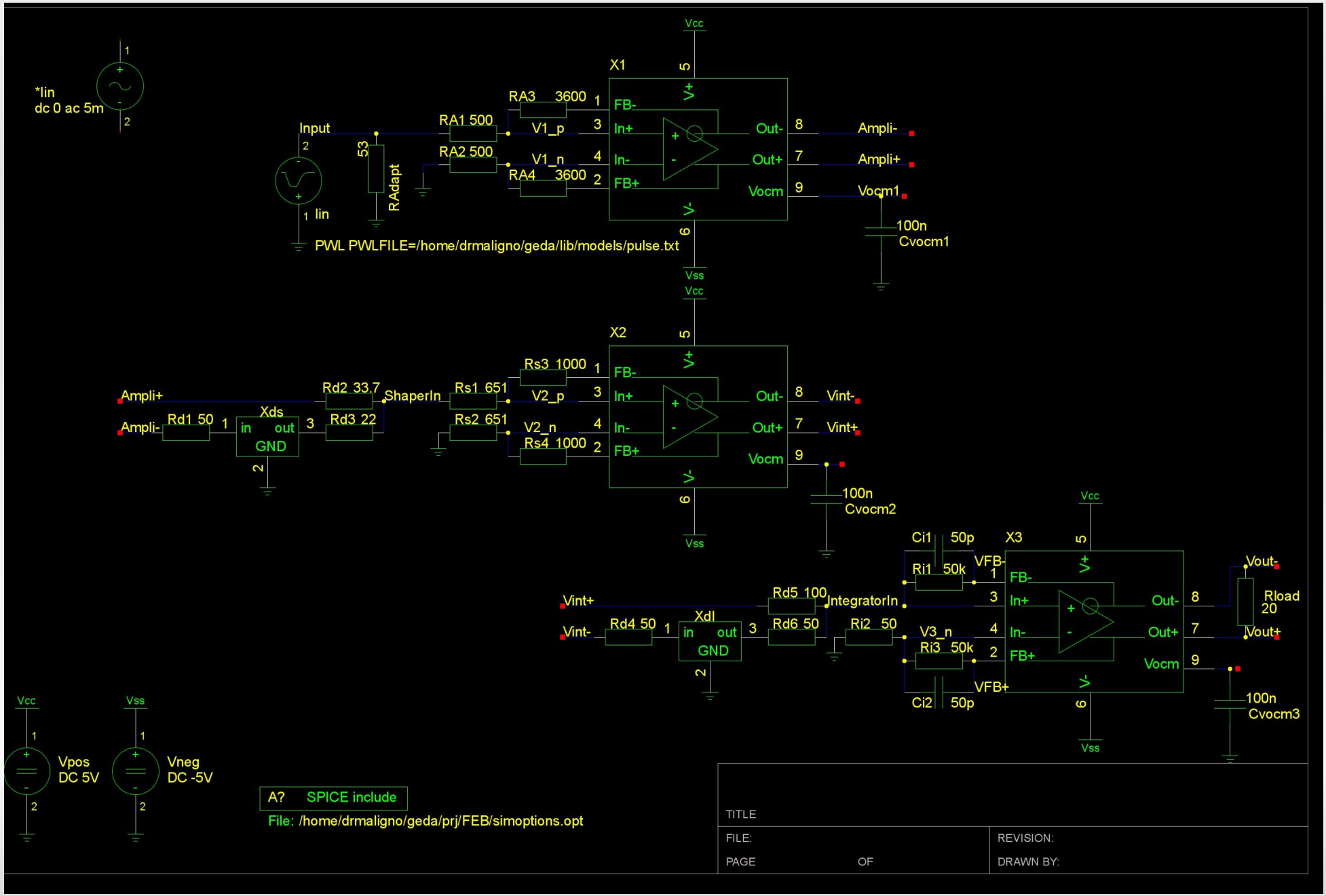
$$Z_{OUT} = R_L \| r_d + \frac{Z_0 \| R_B}{hfe + 1}$$

$$r_d = \frac{hie}{hfe + 1}$$

$hie \approx 100$
$hfe \approx 500$
$r_d \approx 0.2$
$R_L \approx 1\text{K}5$
$R_B \approx 416\text{K}$

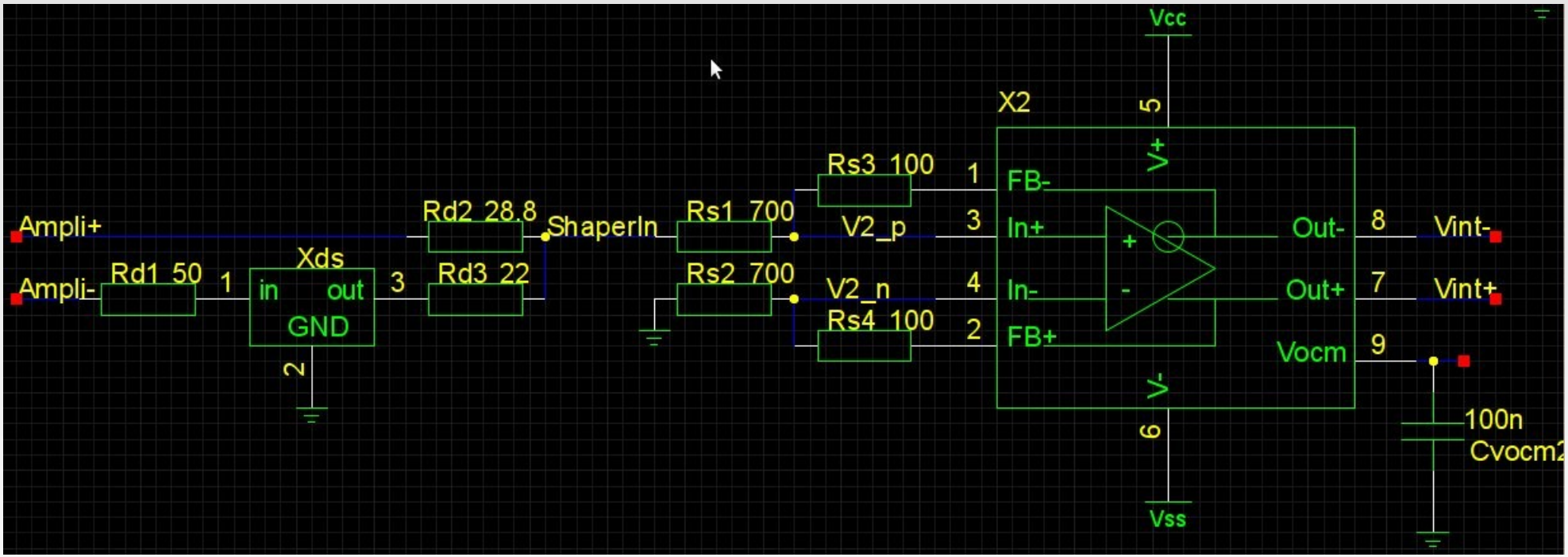
$Z_B \approx 230\text{K}$
$Z_{OUT} \approx 2$
$Gain \approx 1$
$C \approx some\ nF$
$Power\ Consumption \approx 3\text{mW}$

Studied Architectures (III)



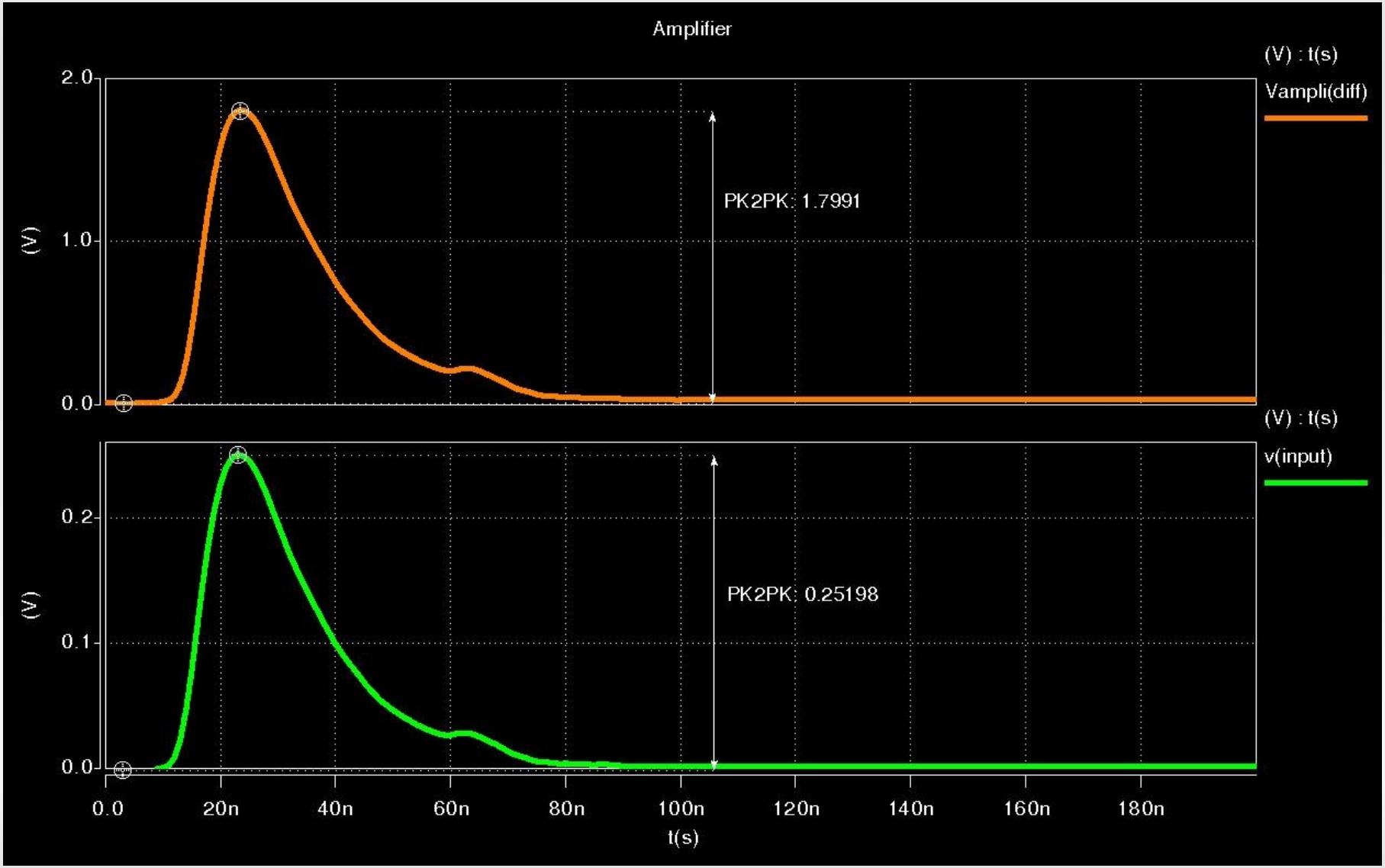
Studied Architectures (III)

- Different approach to same idea, no loop



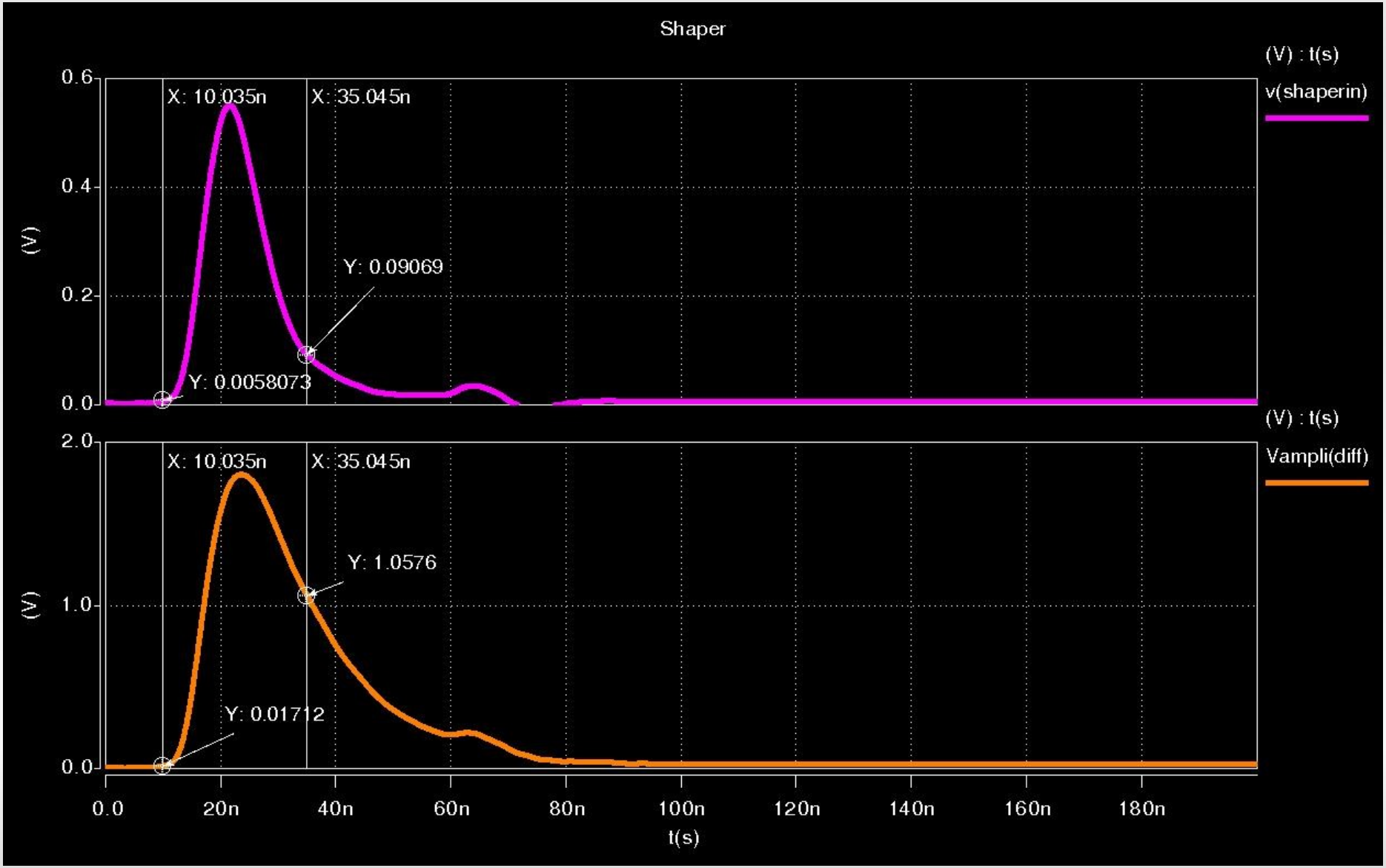
Studied Architectures (III)

- Amplifying Stage



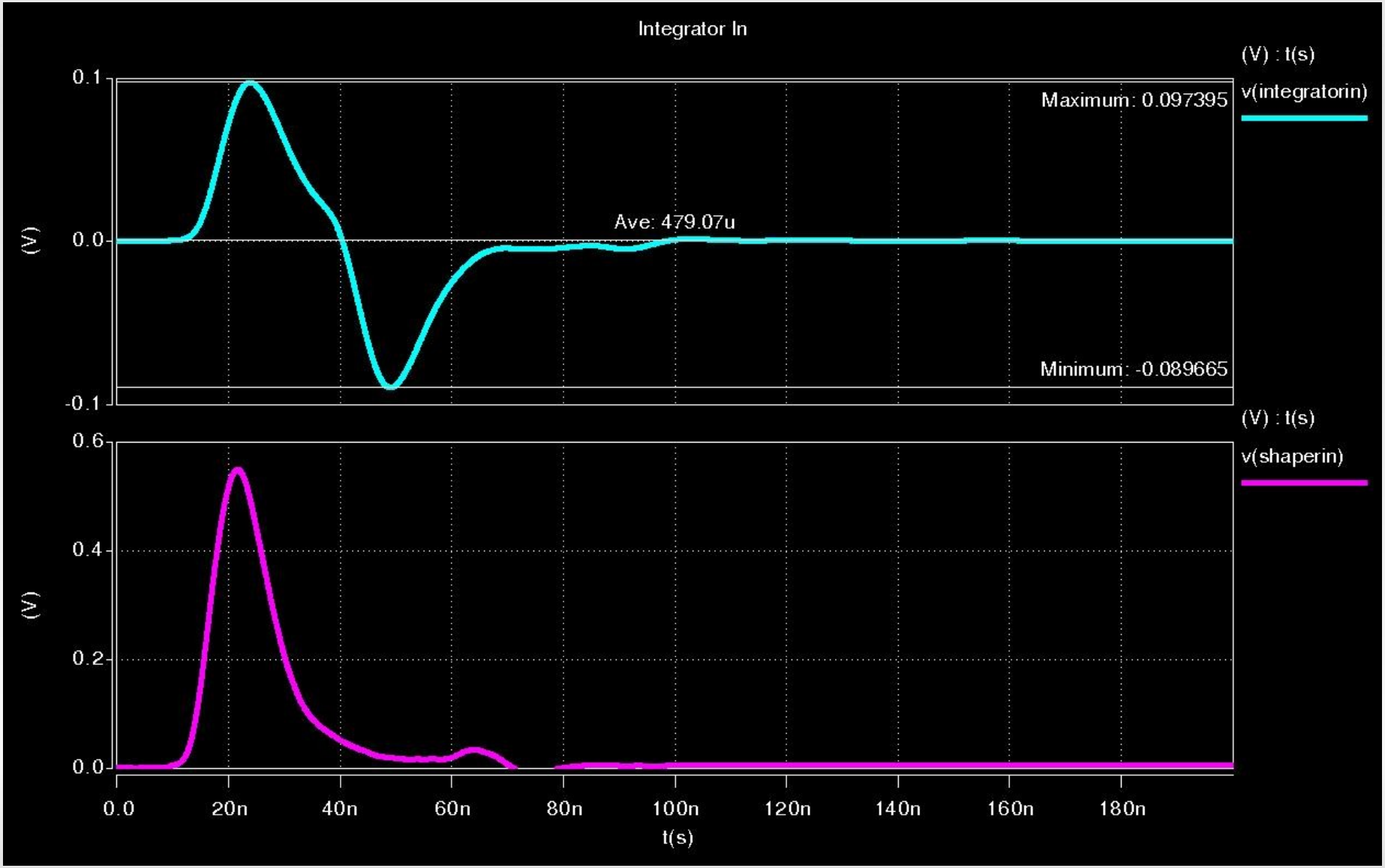
Studied Architectures (III)

- Clipping Stage



Studied Architectures (III)

- Integrator Input



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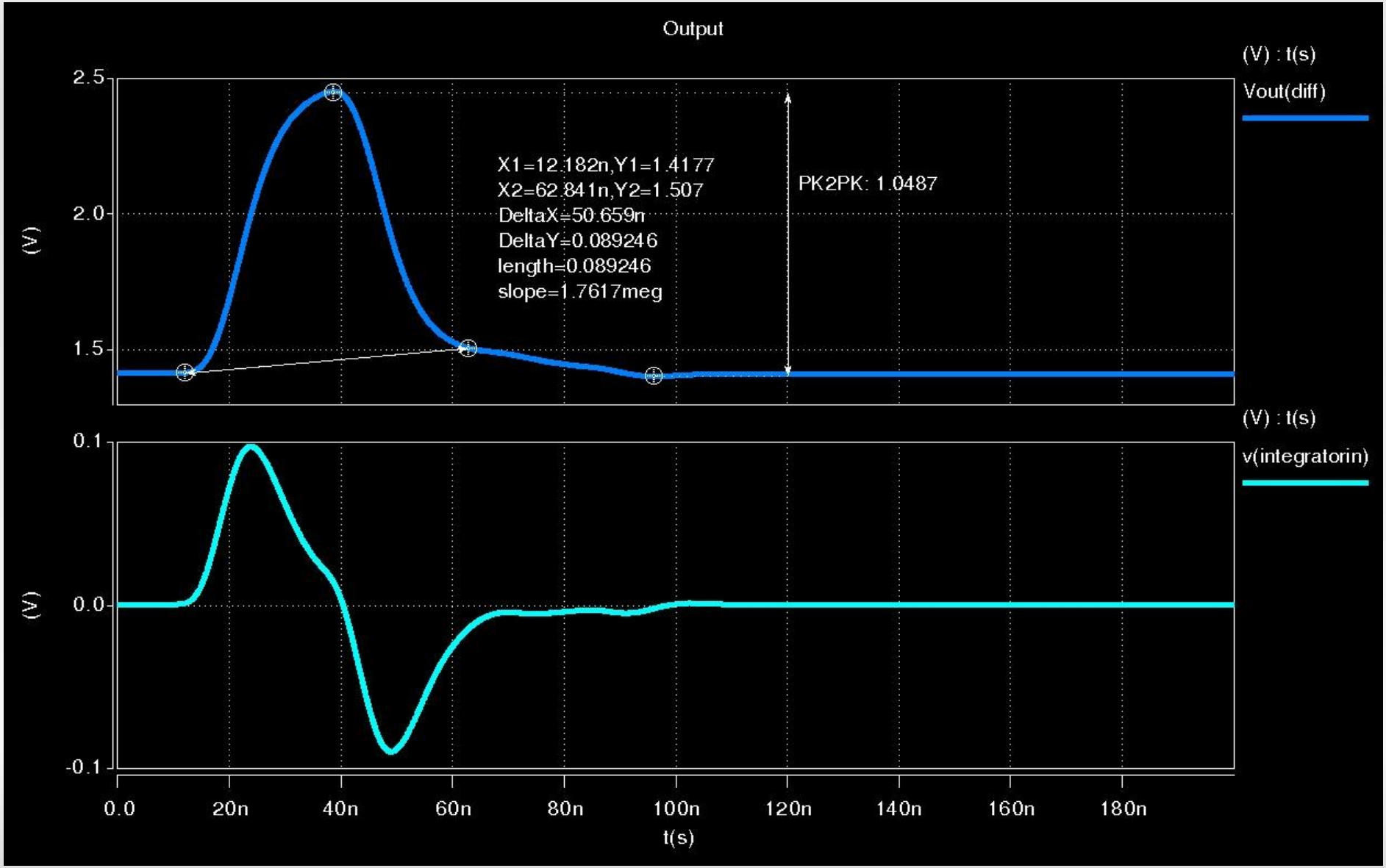
- Integrator Output

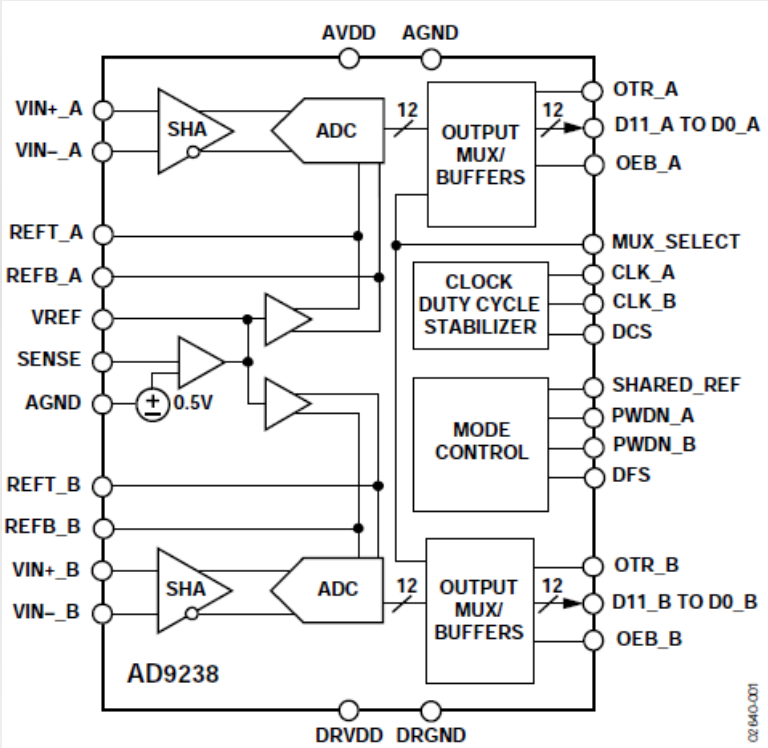


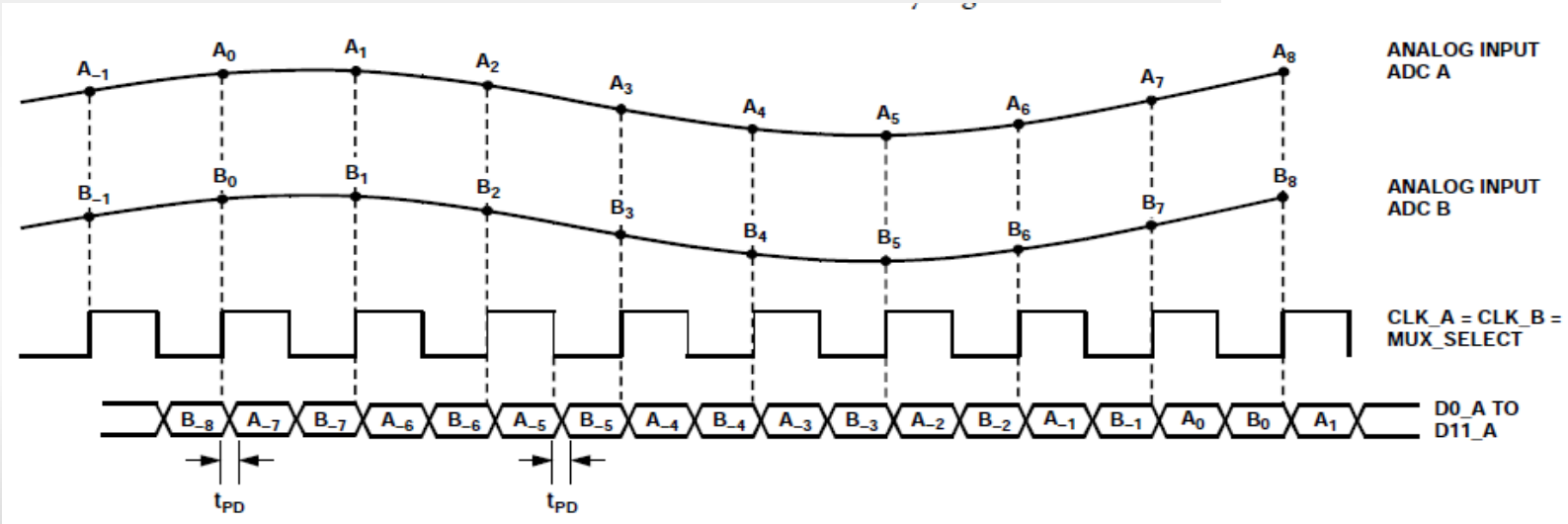
ADC Selection

- In order to make the proper interface between the analogical part and the ADC it is necessary to have it previously selected.
- Our ADC needed 12 bits resolution, at least 40MHz conversion frequency and it was also desirable a small package due to space restrictions.
- The more suitable components for our application where:
  - Texas Instruments ADS6122
    - 1 ADC/Chip but 5x5mm only, LVDS, DDR!
  - Texas Instruments ADS6222
    - 2 ADC/Chip, LVDS, DDR!
  - Analog Devices AD9238
    - 2 ADC/Chip, LVTTL.

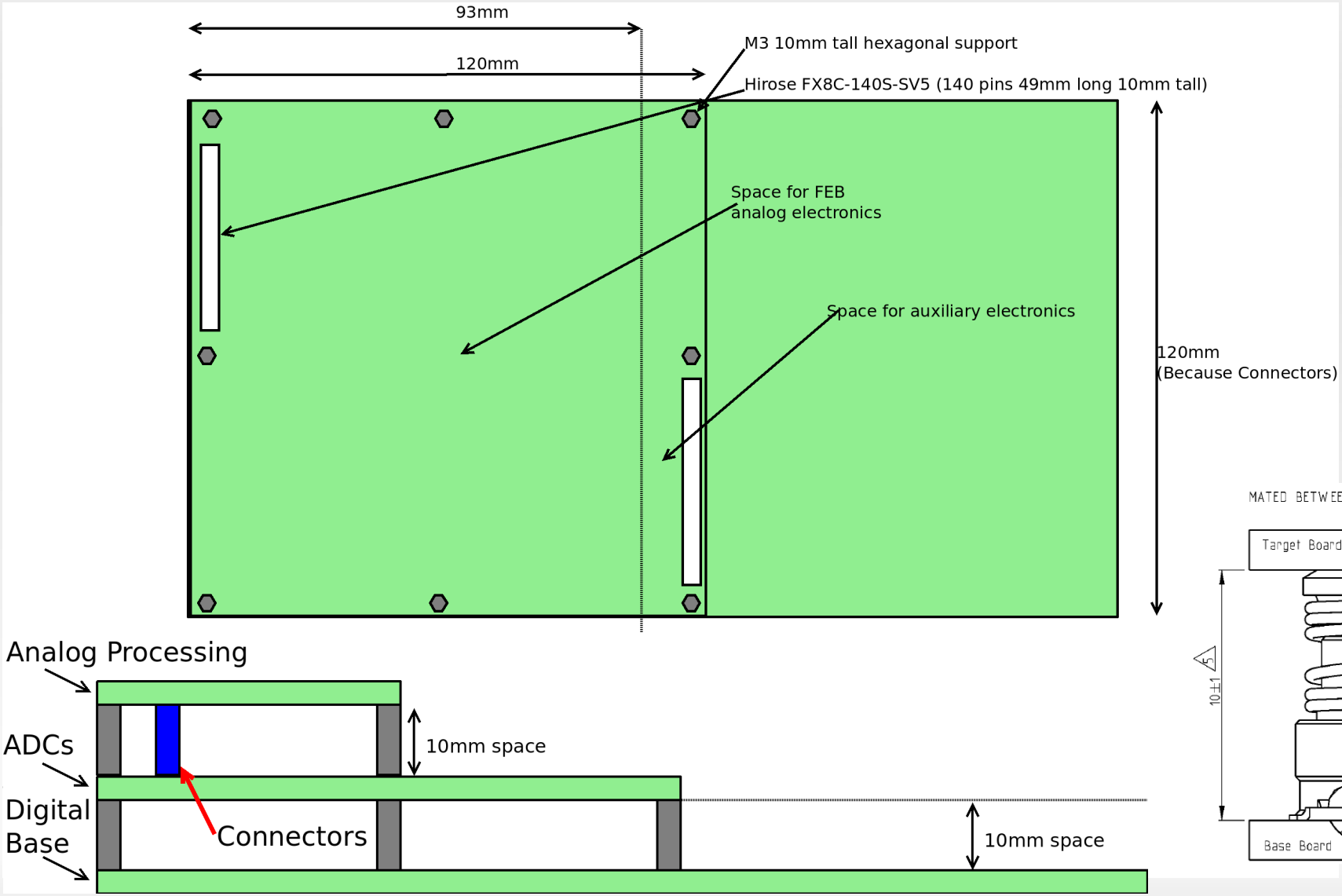
ADC Selection

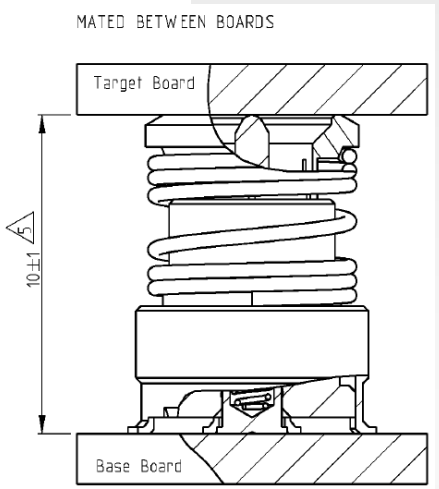
- Analog Devices AD9238
  - One sampling clock per channel
  - Optional multiplexing
  - No RAM configuration





First Set of Prototypes





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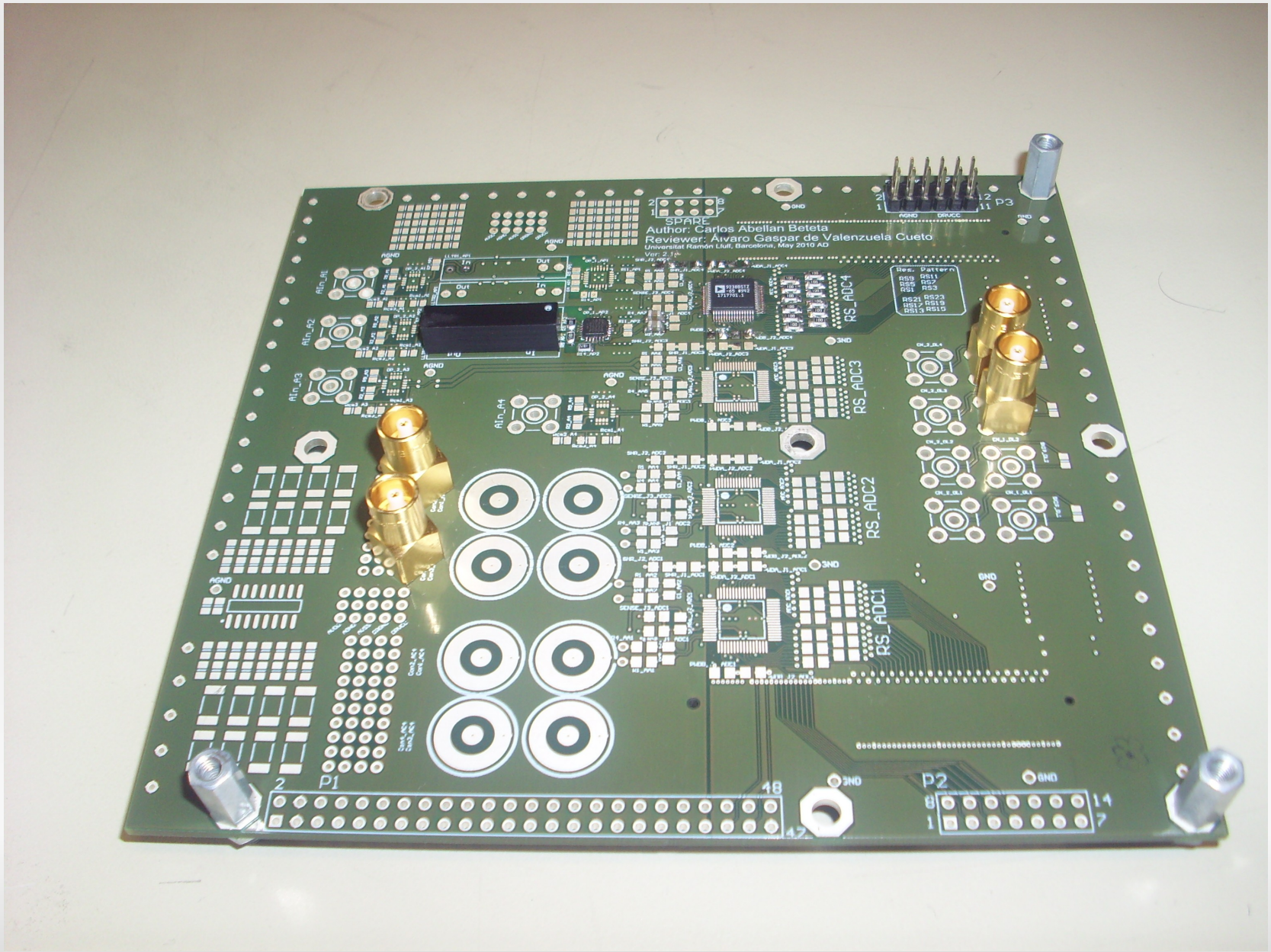

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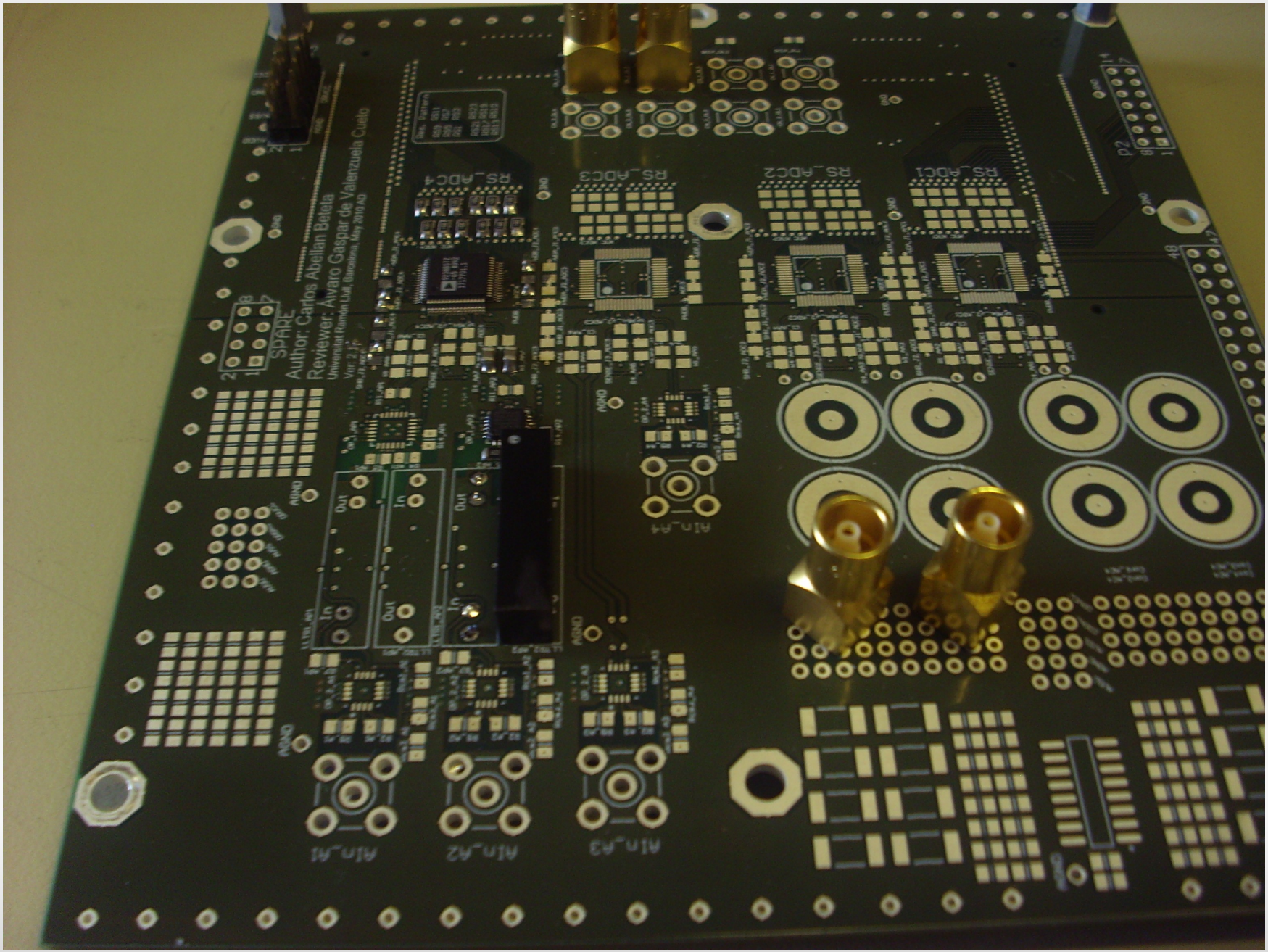


Further Steps

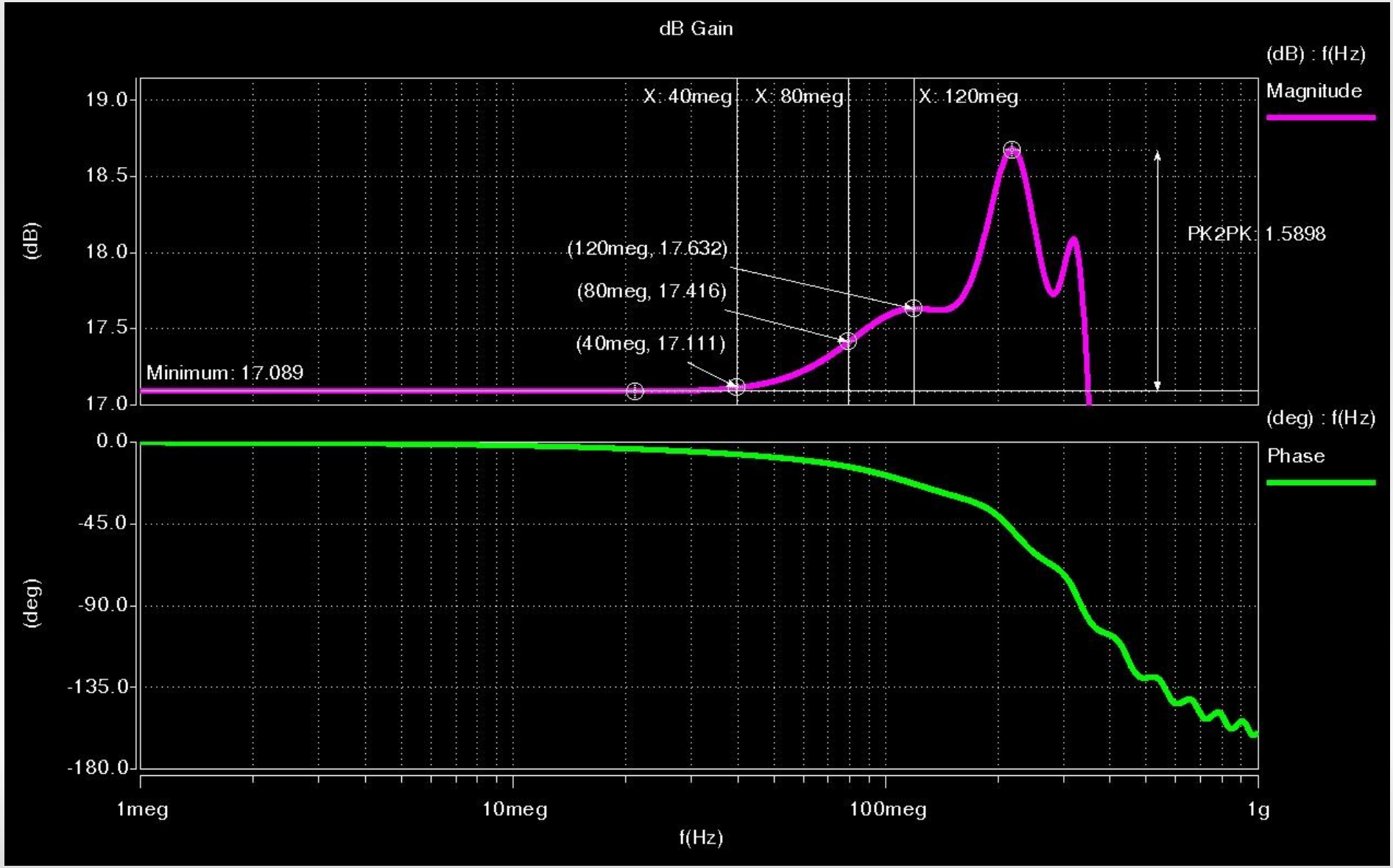
- Finish the prototype and measure all the real life effects
- Perform noise measurements and tradeoff with reflection coefficient
- Fine tune shaping method
- Measure ADC response
- Tests with digital part

Backup Slides

- If more information needed...

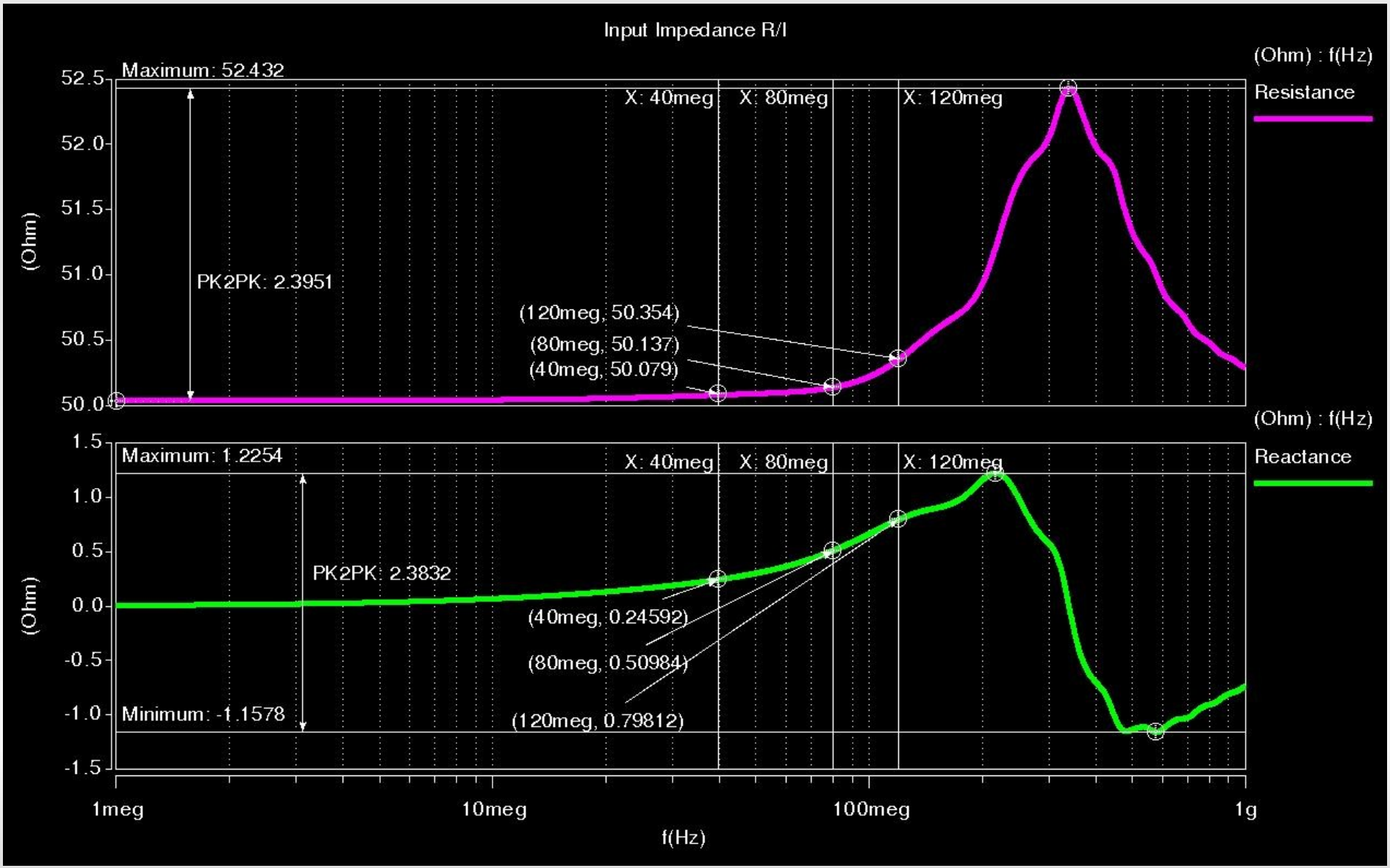
Backup Slides

- Input Stage Gain



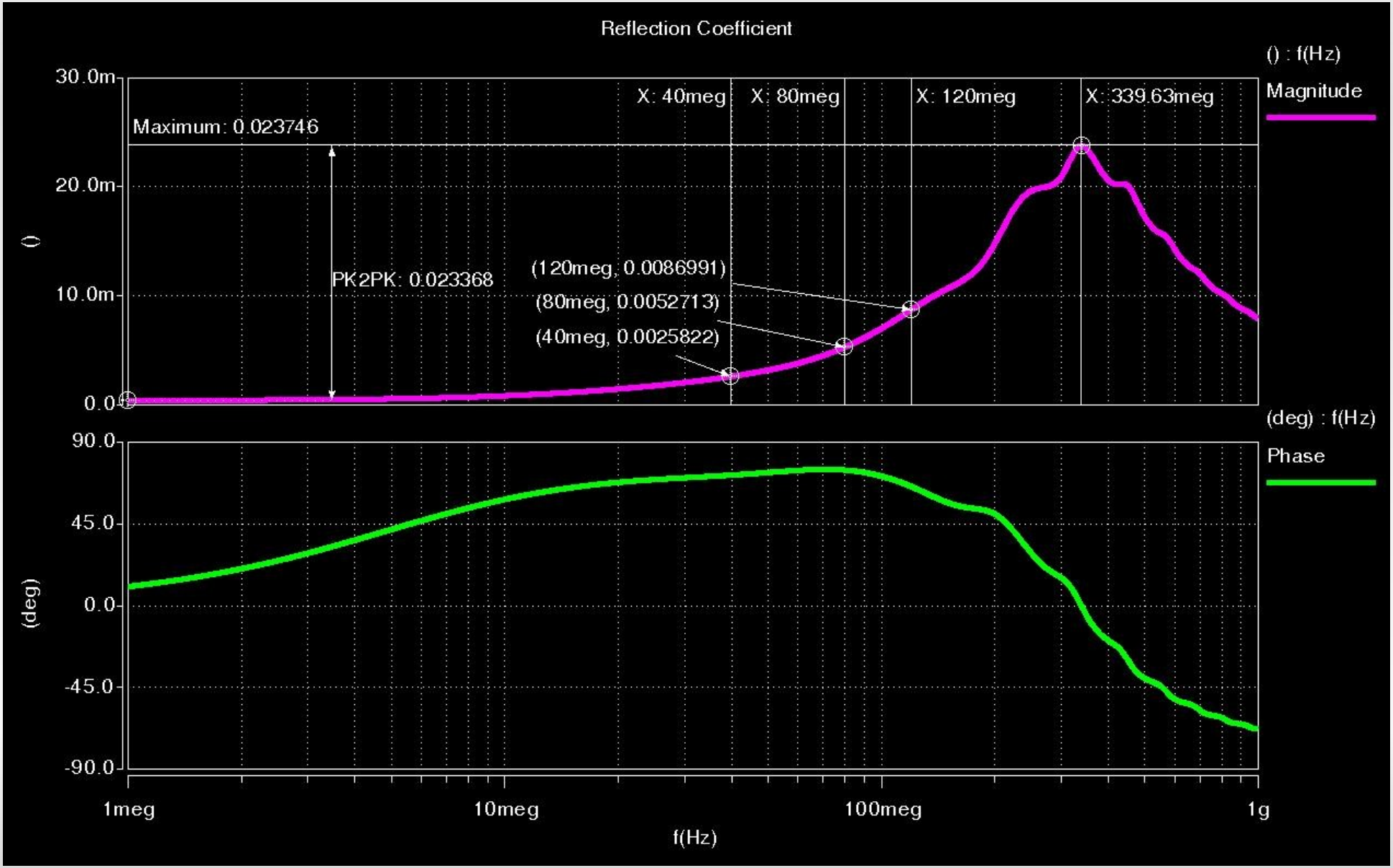
Backup Slides

- Input Stage Impedance



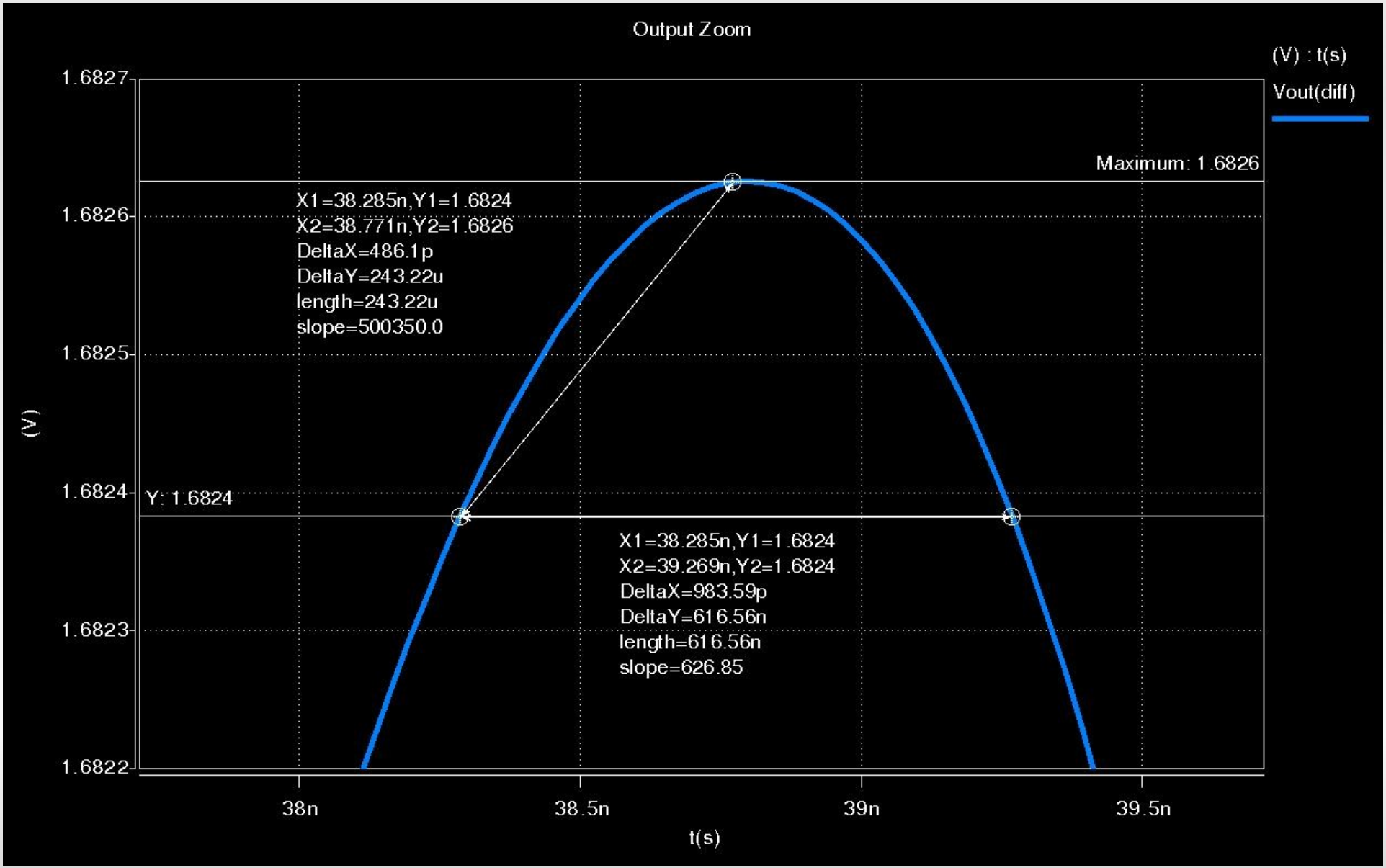
Backup Slides

- Input Stage Reflection Coefficient



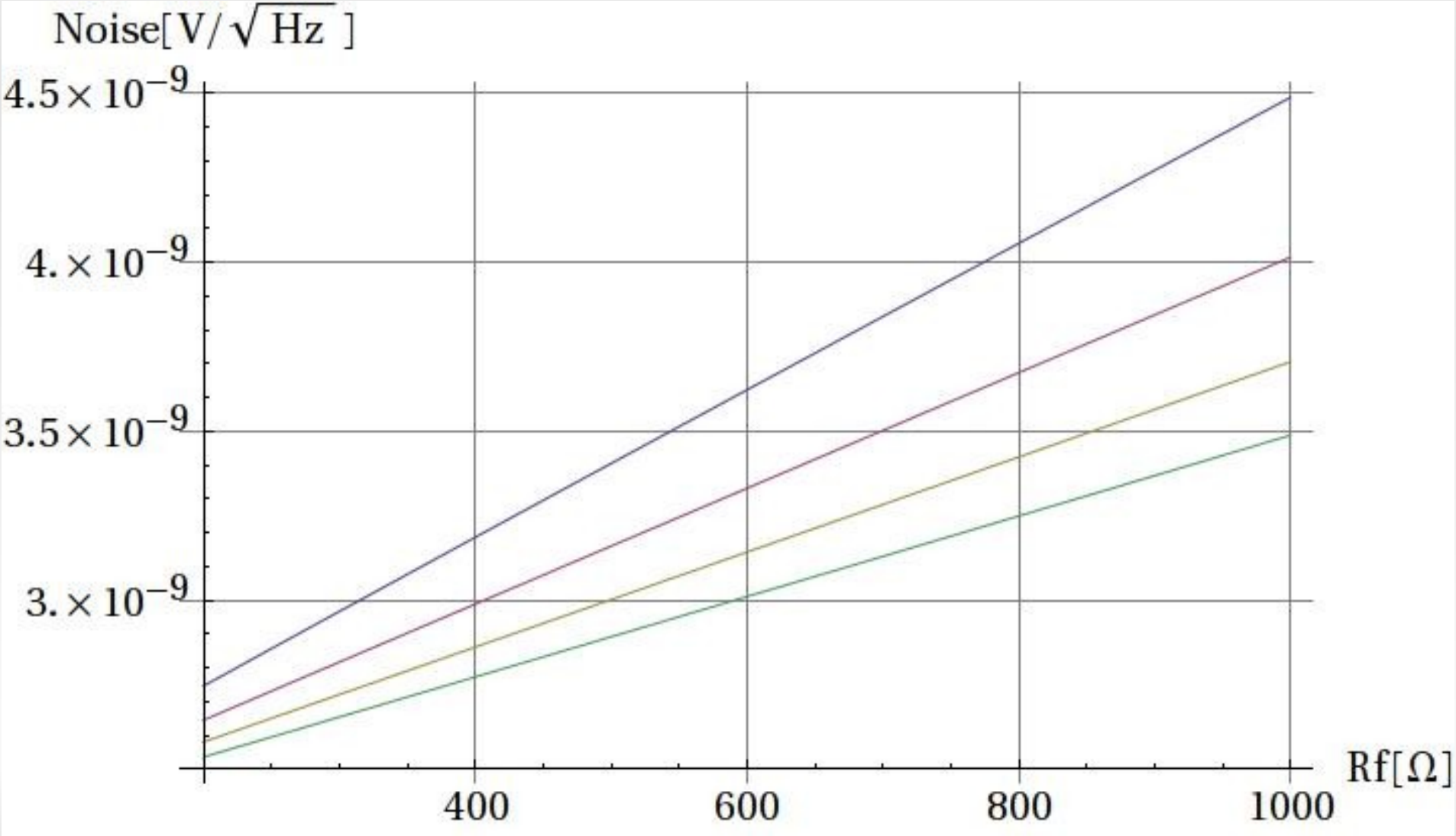
Backup Slides

- Output Zoom



Backup Slides

- Theoretical Noise vs Rf



Backup Slides

- Linearity
  - Definition: Charge/Voltage [C/V]
  - Simulated Linearity Error dependin on input pulse amplitude