RF voltage and frequency interlocks

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RF voltage interlock

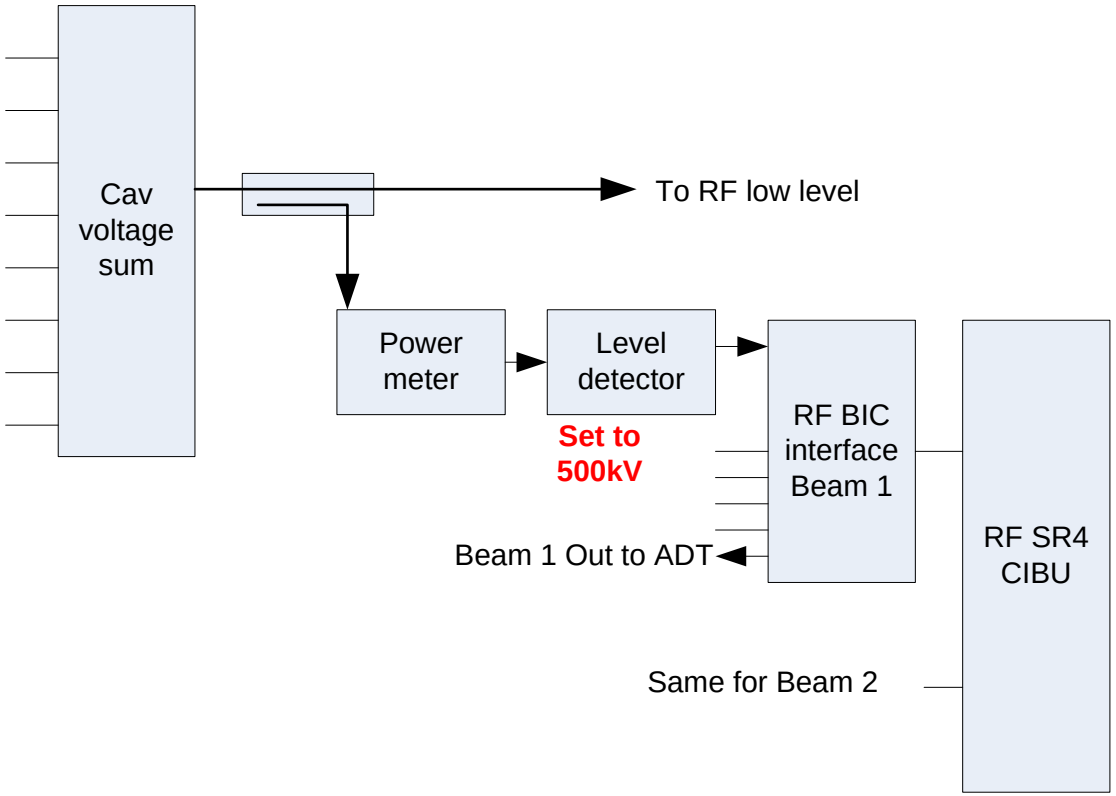
- Motivation: avoid debunching & abort gap population in the event of a total RF trip

- An interlock based on a measurement of the RF total voltage (vector sum) has been installed in SR4

RF Voltage interlock in SR4

Hardware set-up

- The cavity sum signal is fed to a RF standard power meter board.
- The detected signal is compared to a reference with a level detector.
- The output goes to one of the 8 inputs of the SR4 RF BIC interface.
- The output of the RF BIC interface is applied to the CIBU input for Beam 1 and 2 independently.



Status

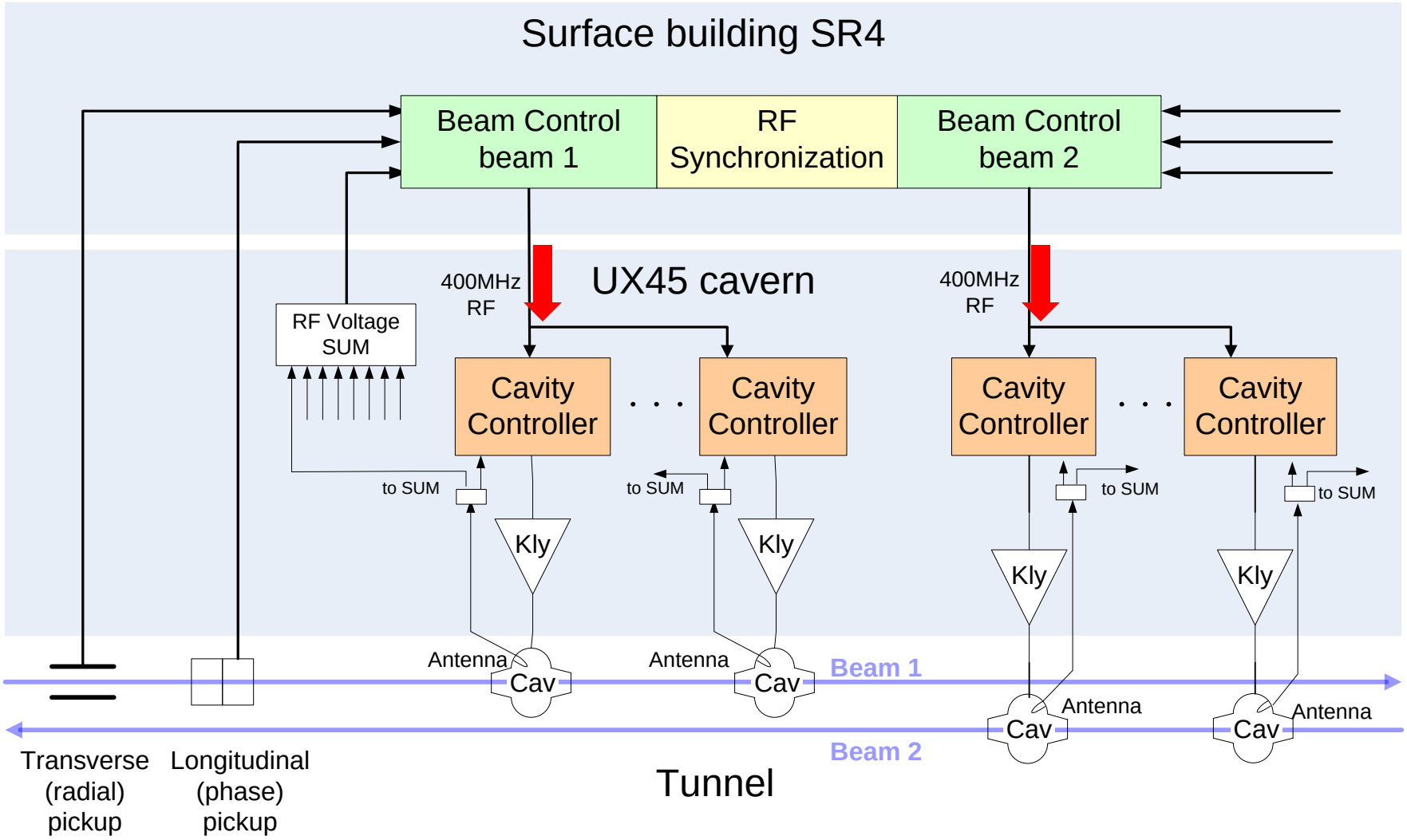
- Connected and tested up to CIBU input for both beams.
- Next step activate input on BIC system (need access) and perform validation test.

L. Arnaudon

RF frequency interlock

- Original motivation:
  - Maximum allowed 0.2% energy error in extraction channel due to RF
- Need to:
  - Measure RF frequency
  - compare with some allowed frequency range
  - generate interlock if outside
- Frequency range ~ central f_{RF} +- 200Hz
- Would like the measurement point as close as possible to the cavities
  - to detect cable inversion etc.

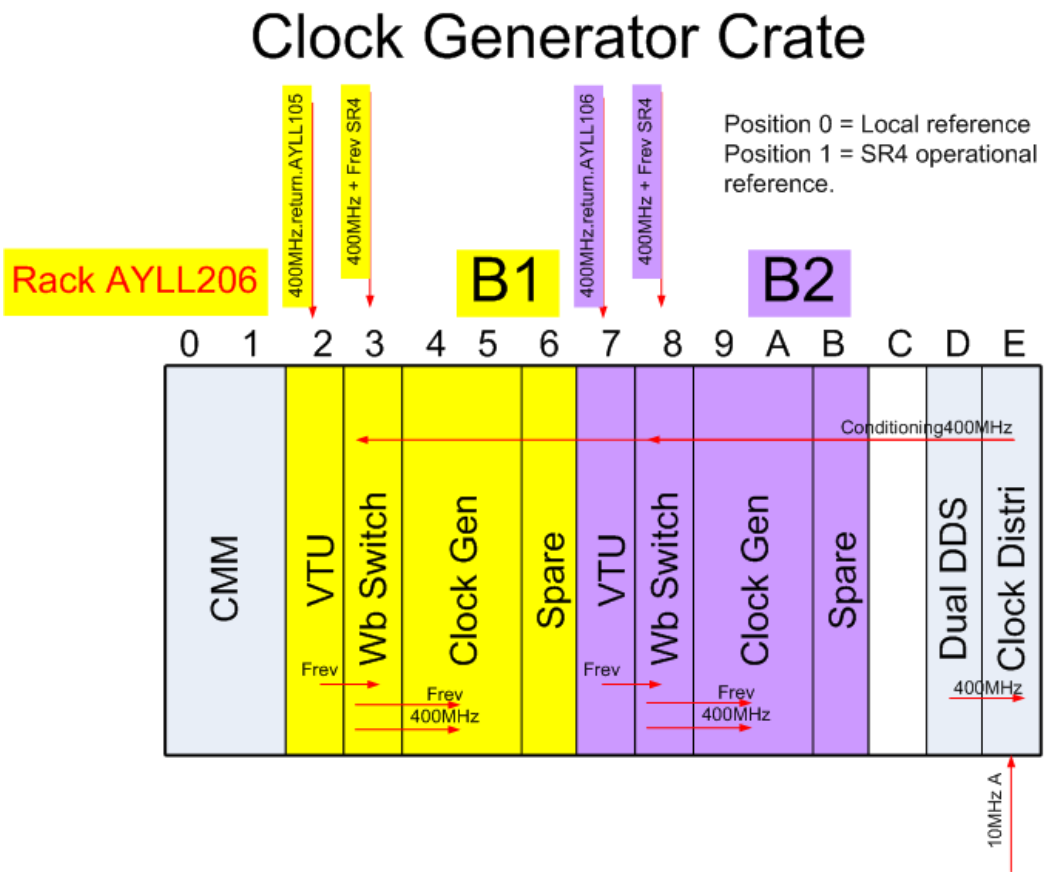
RF Low-Level system layout (simplified)

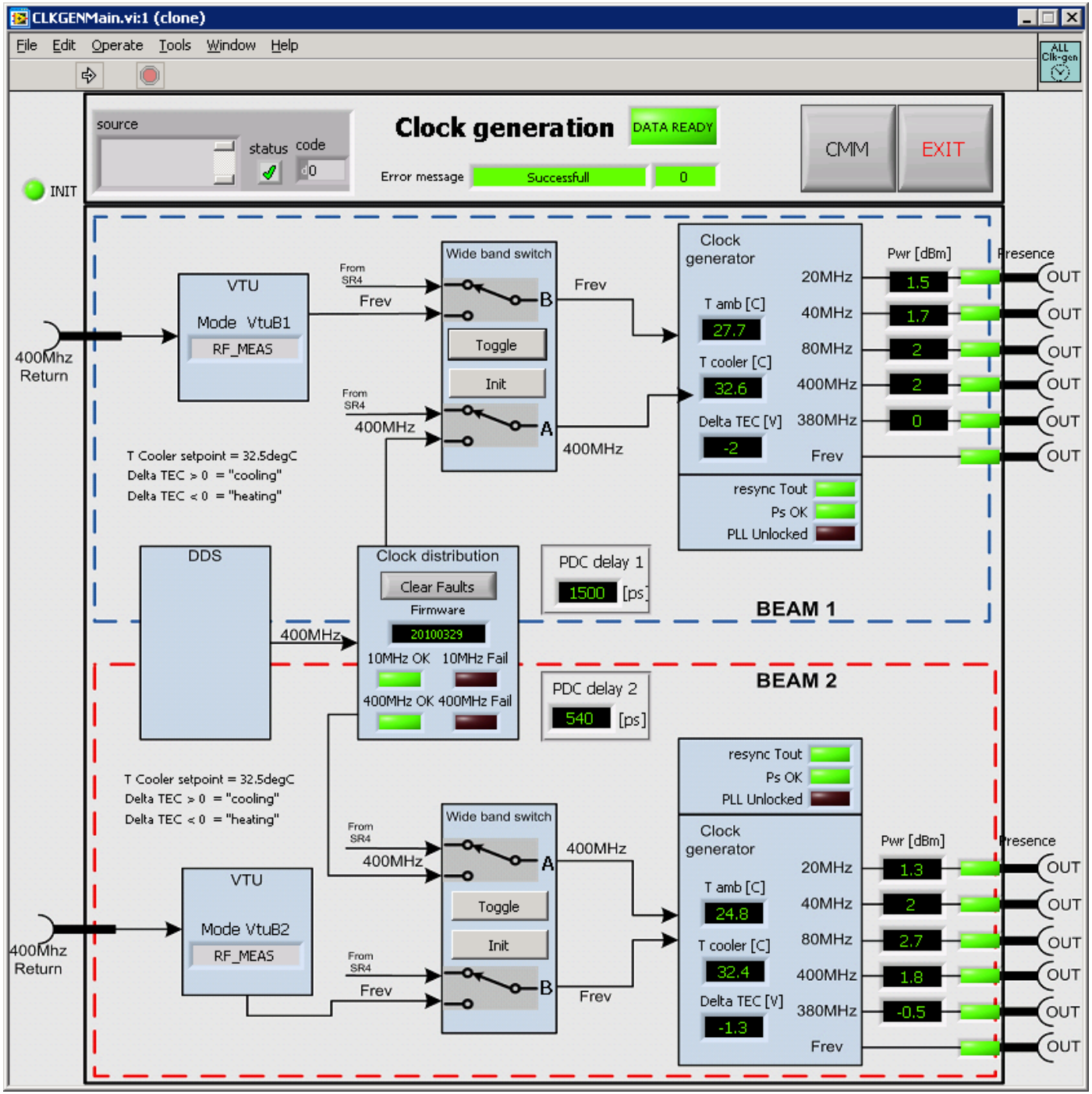


RF frequency interlock

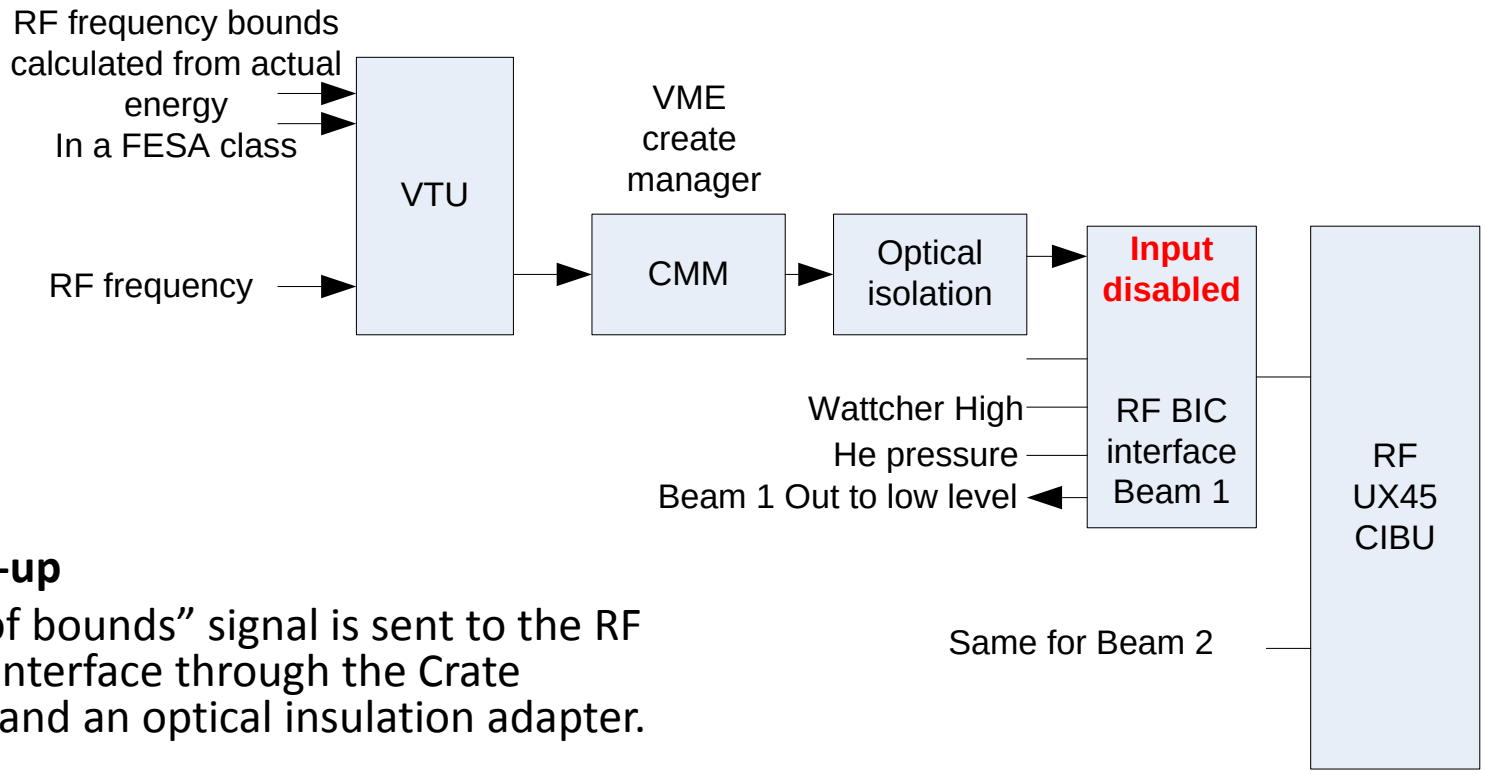
- f_{RF} measured using an RF counter module (VTU) in “RF measurement mode” in the Clock Generator VME crate in the UX45 Faraday cage

- Central f_{RF} calculated from SMP energy in a FESA class running




CLKGENMain.vi:1 (clone)
File Edit Operate Tools Window Help
ALL Clk-gen
source
status
code
d0
Clock generation
DATA READY
Error message
Successfull
0
CMM
EXIT
INIT
400Mhz Return
VTU
Mode VtuB1
RF_MEAS
From SR4
Frev
Wide band switch
B
Toggle
Init
A
400MHz
Frev
Clock generator
T amb [C]
27.7
T cooler [C]
32.6
Delta TEC [V]
-2
20MHz
40MHz
80MHz
400MHz
380MHz
Frev
Pwr [dBm]
1.5
1.7
2
2
0
Presence
OUT
resync Tout
Ps OK
PLL Unlocked
T Cooler setpoint = 32.5degC
Delta TEC > 0 = "cooling"
Delta TEC < 0 = "heating"
DDS
Clock distribution
Clear Faults
Firmware
20100329
10MHz OK
10MHz Fail
400MHz OK
400MHz Fail
PDC delay 1
1500
[ps]
BEAM 1
PDC delay 2
540
[ps]
BEAM 2
VTU
Mode VtuB2
RF_MEAS
T amb [C]
24.8
T cooler [C]
32.4
Delta TEC [V]
-1.3
1.3
2
2.7
1.8
-0.5

RF frequency interlock in UX45



Hardware set-up

- The “out of bounds” signal is sent to the RF UX45 BIC interface through the Crate Manager and an optical insulation adapter.

Status

- Fully cabled and tested for both beams. The RF BIC interface was enabled for a test by the CCC operator.
- The signal is currently disabled.
- The action of enabling/disabling is accessible only by RF specialist application.

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RF frequency interlock issues

- Relies on FESA class updating frequency bounds continuously
- Fail-safe operation: foresee a “watchdog”
  - will generate a beam interlock if FESA task crashes
  - it has been known to crash...
- Run without watchdog?
  - if FESA task crashes at flat bottom, frequency will be in bounds until we start to ramp

  →beam dump... RF very unpopular
- Compromise: sequencer task to check FESA task status before start of ramp?
  - status of VTU Fesa task available in crate master class