# Control and Low Level RF System of the SOLEIL Synchrotron

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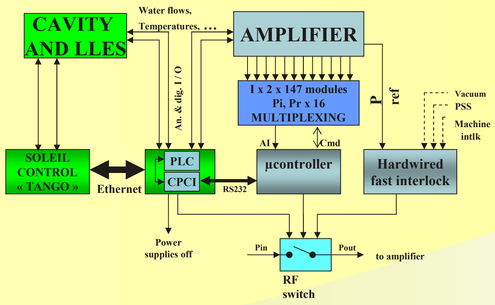
## ABSTRACT

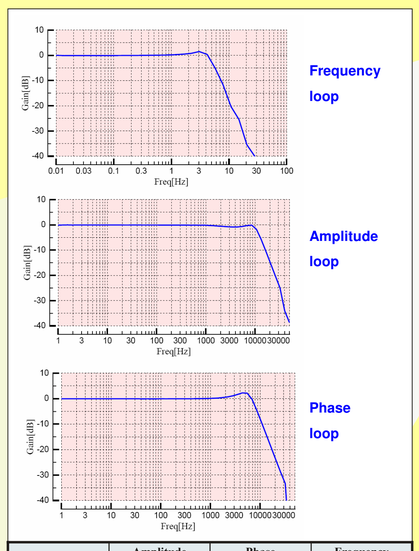
In the SOLEIL storage ring, two cryomodules, each containing a pair of 352 MHz superconducting cavities, will provide the maximum power of 600 kW, required at the nominal energy of 2.75 GeV with the full beam current of 500 mA and all the insertion devices. They will be supplied with liquid helium from a single cryogenic plant and each of the four cavities will be powered with a 190 kW solid state amplifier consisting in a combination of 315 W elementary modules (about 700 modules per amplifier). The low level electronic system that will be used in the first phase consists in “slow” amplitude, phase and frequency loops, complemented with a direct RF feedback. A fast digital, FPGA-based, I/Q feedback is currently under development, that should be implemented later on. The control of the whole system is insured by several PLCs and a µcontroller, which monitors the amplifier parameters through a multiplexing system. The PLCs are linked to the SOLEIL TANGO framework via Ethernet. The control and low level RF system is described and the first operational/experimental results are reported in this paper.

## RF Control & Low Level for the Booster

### GENERAL CONTROL ARCHITECTURE

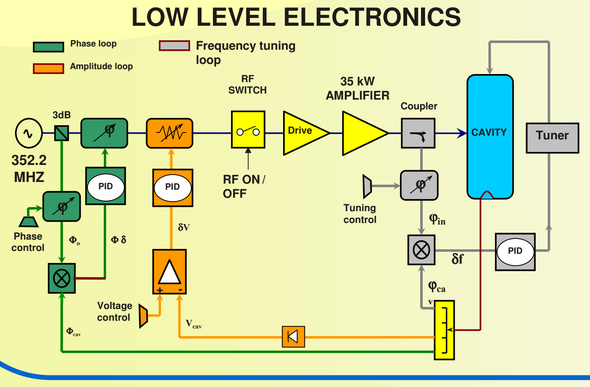



### CHARARISTICS OF THE LOOPS



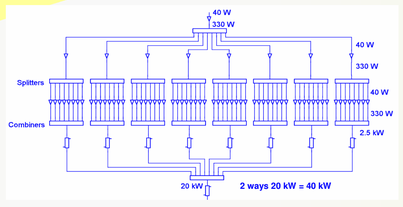

| | Amplitude | Phase | Frequency |
|---|---|---|---|
| Accuracy | ± 0.25 % | ± 0.4° | ± 30 Hz |
| 3 dB BW | 12 kHz | 7 kHz | 5 Hz |

### LOW LEVEL ELECTRONICS

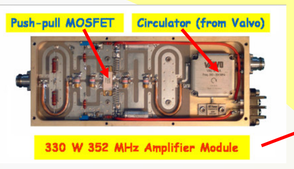



## RF Amplifier & Cavity for the Booster

### Booster Amplifier Principle

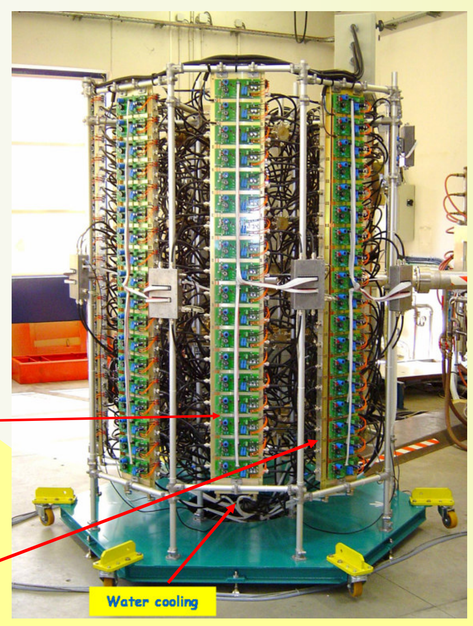



600 W, 300 Vdc / 30 Vdc converter

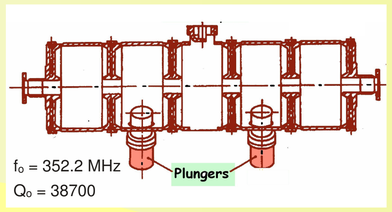



330 W 352 MHz Amplifier Module

### 35 kW Solid State Amplifier

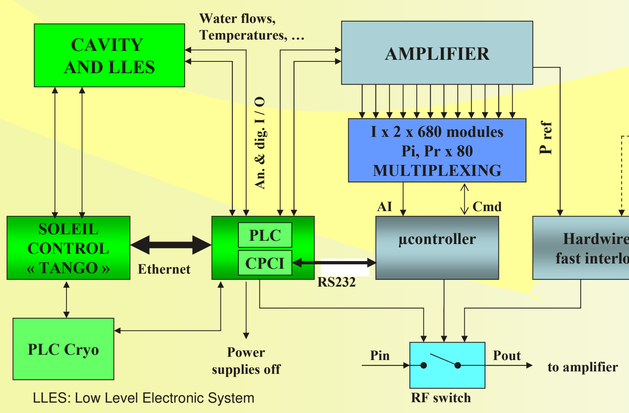



### 5-cell Cu cavity ( CERN–LEP type )

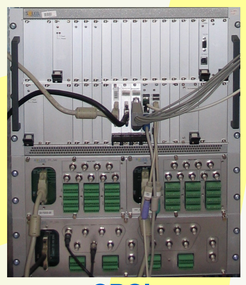



## Control & Low level for the RF Storage Ring

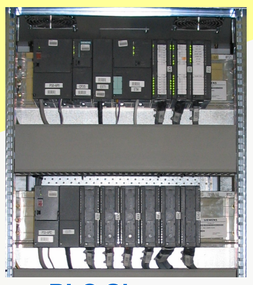
### DIAGRAM OF THE RF SYSTEM




LLES: Low Level Electronic System

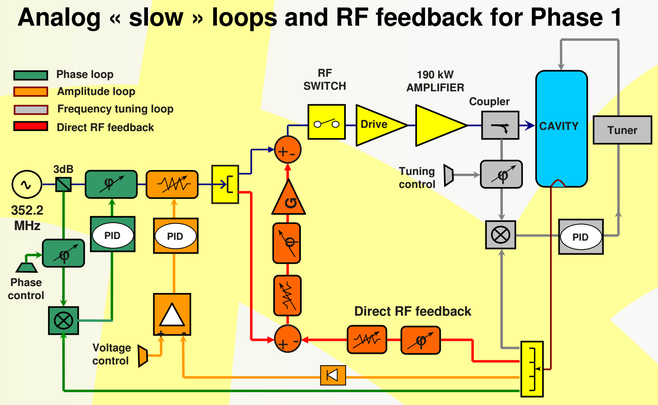


CPCI hardware



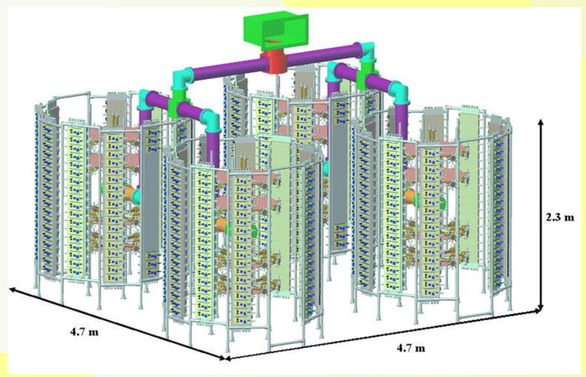
PLC Siemens S7-300

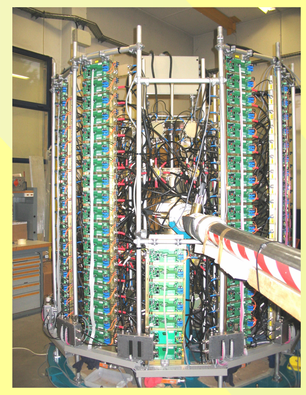
### Analog « slow » loops and RF feedback for Phase 1




## RF Amplifier & Cavities for the Storage Ring

### 190 kW Solid State Amplifier

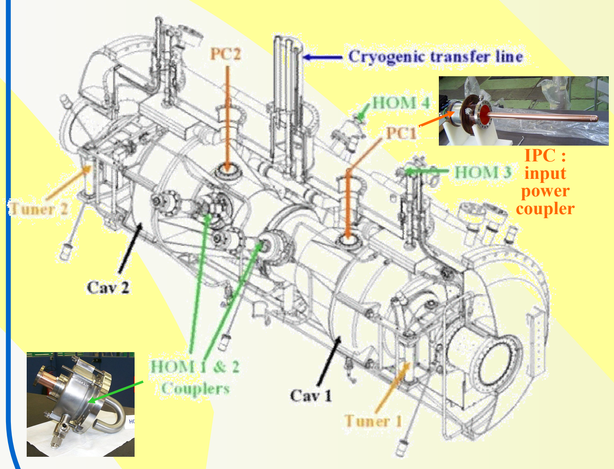


Use of 2 cryomodules, each of them containing a pair of cavities
Each of the 4 cavities powered with a 190 kW solid state amplifier
Same principle as for the BO one, extended to 4 x 50 kW
( → 724 modules of which 42 in « stand-by »)

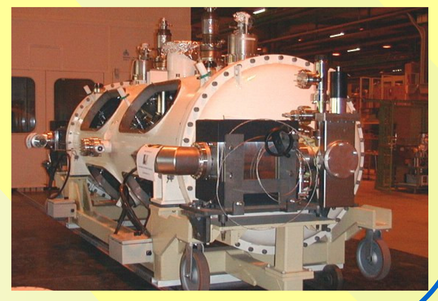
The first SR “50 kW Tower” under test

### Cryomodule with 2 Nb/Cu cavities

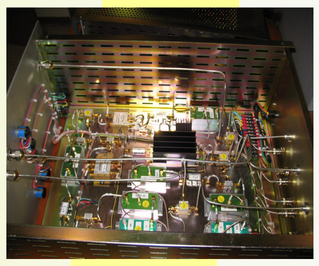




“50 kW tower” control display
( transistor currents, Pi & Pr )



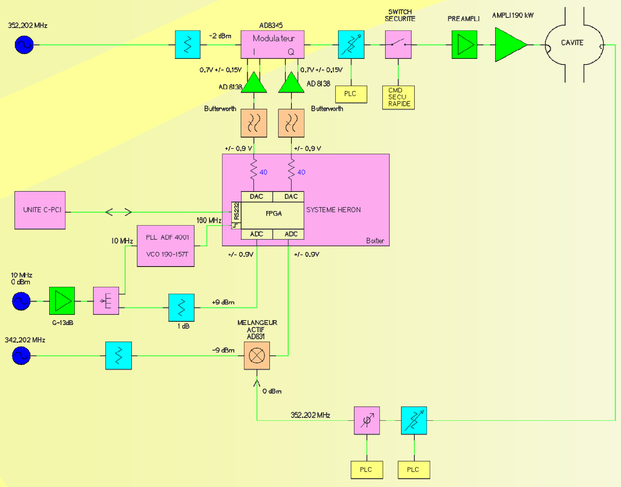
### Low Level RF components



### Micro-controller & Analog feedback

### Diagram of the Fast Digital Feedback for Phase 2

**A fast digital FPGA-based feedback with IQ modulator and demodulator is under development (collaboration with the CEA)**




### Digital IQ Control Loop

The HERON IO2 module has been selected for our application. The main reason of this choice is the short latency time between the input and output signals, due to the Virtex II performance. The architecture and main component characteristics of this module are described in figure 1. It works in stand-alone mode.
In order to study the behaviour of the program with time constraints, ISE (Integrated Software Environment) tools are used to simulate our application. The loading of the FPGA (Field - Programmable Gate Array ) boot program into the PROM is quite fast and easy.

Module Architecture

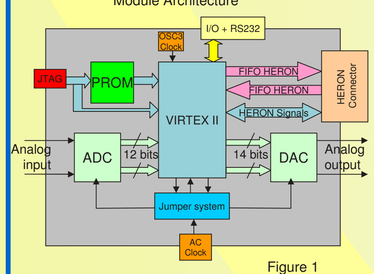



Figure 1

Heron IO2V2 board

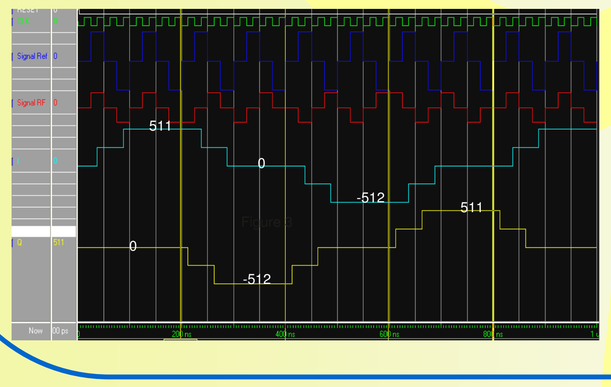
**HERON-IO2 FPGA module with 2 channels of 12bit 125Mhz A/D and 2 channels of 14bit 125Mhz D/A**
**• HERON-IO2V has Xilinx Virtex II FPGA with 1M gates HERON-IO2S**
**• FPGA configuration downloaded using the HERON Serial Bus.**
**• Choice of clocking options**
**• Two 125MSPS 12 bit A/Ds connected to the FPGA**
**• Two 125MSPS 14 bit D/As connected to the FPGA**
**• High analog signal bandwidth of 500Mhz in and 145Mhz out.**
**• 8 uncommitted digital I/Os**
**• Several serial I/O options possible -- configured by the FPGA.**
**• Connects to all of the HERON FIFOs, UMI and module ID signals**

### Digital IQ demodulator

Four samples of the reference and RF signals, over one period, are used to calculate I and Q.

I1 = Vref(0)*VRF(0)+Vref(1)*VRF(1)  Q1 = Vref(0)*VRF(1)-Vref(1)*VRF(0)
I2 = Vref(2)*VRF(2)+Vref(3)*VRF(3)  Q2 = Vref(2)*VRF(3)-Vref(3)*VRF(2)

I = (I1+I2)/(2*V0)  Q = (Q1+Q2)/(2*V0)




### FPGA Architecture Design

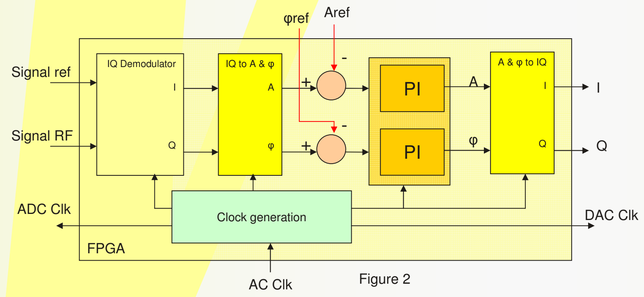



Figure 2

The IQ demodulator and the clock generator with DCM (Digital Clock Manager) have already been tested. The PI (Proportional - Integrate) are realised with a FIR (Finite Impulse Response) filter, provided by XILINX (Intellectual Property). The results of simulations are illustrated in figures 3 to 5.

***Currently under tests*** :
• The “ IQ to A & φ " function transforms from polar to cartesian coordinates.
• The phase and amplitude reference signals are input through RS232, the IP of which is provided with the module.

Low Pass FIR Filter Simulation (Fc = 5MHz)

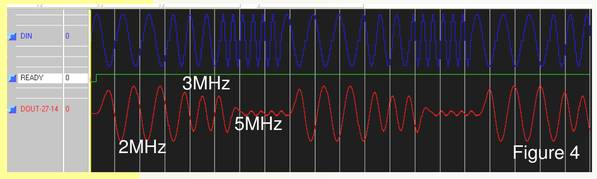



Figure 4

DCM (Digital Clock Manager)

The FPGA, ADCs and DACs must be synchronized with the machine clock.

The DCM does not introduce any delay and it provides synchronized clock signals to those components. Once the DCM is locked, the output clocks are extremely accurate.

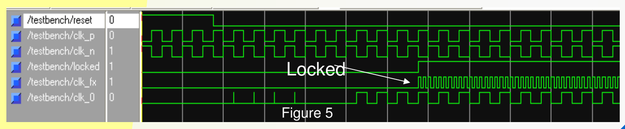



Figure 5

## Summary and Conclusions

The RF plant of the Booster, a 5-cell Cu cavity powered by a 35 kW solid state amplifier with the associated Control and Low Level RF (“slow” analogue amplitude, phase & frequency loops), is fully operational and currently in use for the Booster commissioning.

In the Storage Ring, the power is transferred to the beam by means of two cryomodules, each containing a pair of superconducting cavities; the four cavities are individually powered with a 190 kW solid state amplifier.
For starting, the control and LLRF of each plant will be basically the same as the Booster one, but complemented with a fast direct feedback for insuring the stability up to the full beam current of 500 mA.
In parallel, we are developing in collaboration with CEA, a fast digital FPGA-based feedback with IQ modulator and demodulator. Later on, it will replace the initial fully analog version.
Results of simulation show that both, the direct feedback and digital IQ systems, allow to operate with a comfortable stability margin up to the maximum beam loading conditions (“Modelling and Simulation of the RF System for SOLEIL Synchrotron”, poster presented at this conference).