The FE-I4 ATLAS Pixel Chip for Upgraded LHC Luminosities

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I. Introduction

A new ATLAS pixel chip FE-I4 has being developed for use in upgraded LHC luminosity environments. FE-I4 is designed in a 130nm technology, presenting advantages in terms of radiation tolerance and digital logic density. It is based on an array of 80 by 336 pixels, each 50×250µm², sheltering analog and digital sections. The analog pixel section is designed for low power consumption and compatibility to several sensor candidates. The digital architecture is based on a 4-pixel unit called Pixel Digital Region (PDR), which allows for a power-efficient, low recording inefficiency design, and gives some control over the problem of timewalk. The chip periphery consists of a control block, powering blocks, a command decoder, a data formatter, an asynchronous storage FIFO, an 8b10b coder and a clock multiplier unit to handle data transmission up to 160Mb/s. Increased power consumption in the inner layers of ATLAS translates into more material for cooling and power routing, which degrades the tracking and the b-tagging quality. The FE-I4 collaboration places hence severe constraints on the power consumption of all blocks.

II. The Analog Pixel

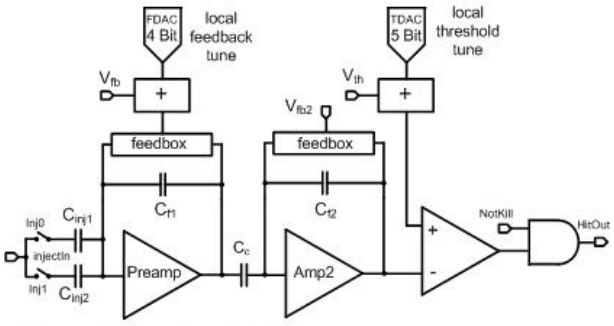

Figure 1: FEI4 analog pixel chain.

The FE-I4 analog pixel is based on the two-stage architecture sketched in Figure 1. The pre-amp is a straight regulated cascode with triple-well nmos input device, with feedback tuned by a 4-bit local DAC. It is AC-coupled to the second stage of amplification, implemented as a folded cascode with pmos input. With the two-stage architecture chosen, an additional gain factor is introduced by the ratio of the AC-coupling capacitance to the second stage feedback capacitance. This allows optimization of the pre-amp for high charge collection, fast rise time and low power consumption. The analog pixel contains a leakage current compensation differential pair. Together with the AC-coupling architecture chosen, this structure handles post-irradiation sensor leakage current up to 100nA/pixel. The analog section is completed by a discriminator, which can be adjusted locally through 5 configuration bits. The analog section has being prototyped and has shown excellent characteristics with respect to noise and threshold dispersions, both pre- and post-irradiation.

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III. The Digital Pixel and the Digital Architecture

The present ATLAS pixel IC FE-I3 uses a double-column hit drain mechanism, where every digital hit detected in the pixel array is transferred to a data pipeline sitting in the End-of-Column periphery, and waits until Level 1 Trigger (L1T) based confirmation or erasing. It could be shown that this architecture reaches its limits when going to increased hit rate due to unacceptable double-column data traffic. Taking advantage of the smaller feature size which allows including more digital functionalities at the level of the pixel, a new digital architecture was chosen. The new digital structure is based on local hit storage inside the 4-pixel unit PDR in a 5-deep data buffer. The PDR structure is well tuned to real physics data where hits come clustered: It is efficient from the point of view of power consumption and presents reduced data losses. Finally, the hit processing machinery after the discriminator output is designed to record small pixel hits without any timewalk, by taking advantage of the presence of a bigger hit signal in the vicinity. The PDR is the basic building block of the double-column. The readout of PDR data is organized double-column-wise by a token passing mechanism. Power distribution scheme, clock distribution and buffering strategy inside the double-column are now defined, as well as a strategy for noise isolation of the analog pixel from the digital activity.

IV. Periphery

The FE-I4 periphery contains a command decoder unit which needs to handle not only programming of the various DACs and registers but also L1T requests from ATLAS trigger system. The periphery also contains low drop-out regulators, as well as the circuitry needed to test new concepts of powering schemes (Serial Power or DC-DC conversion). The End of Chip Logic is the control block which organizes the data readout. To increase the transmission bandwidth and fit the data output protocol, data reformatting is provided. Data is then 8b10b encoded, before being serialized and sent out at 160Mb/s through pseudo-LVDS transmitters. For back compatibility with the current ATLAS pixel system, clock multiplication from the 40MHz clock (LHC bunch-crossing structure) is supplied to allow the higher bandwidth data transfer. An overview of FE-I4 is shown in Figure 2.

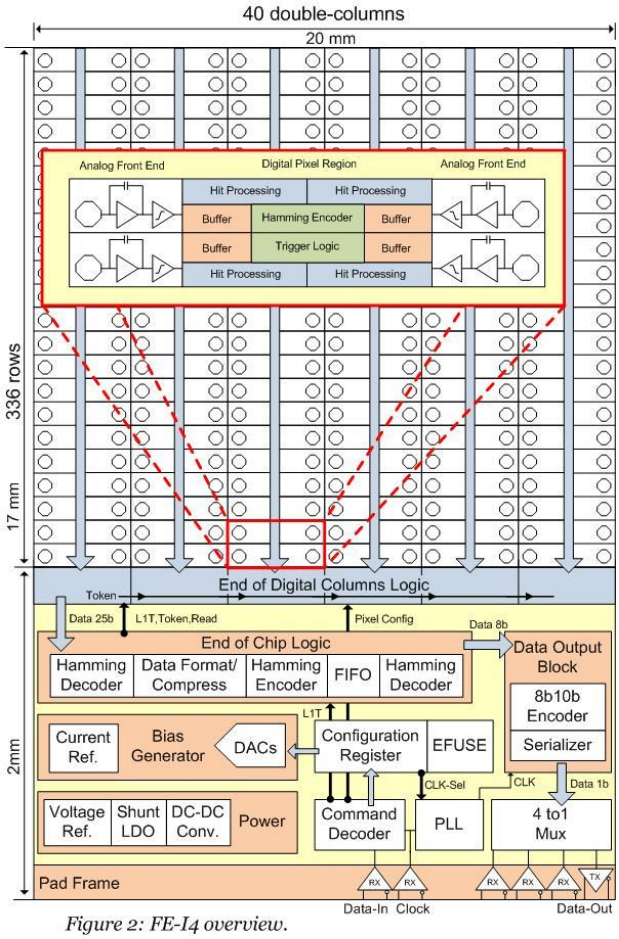

Figure 2: FE-I4 overview.

V. Schedule

FE-I4 will be submitted mid-2010, and the IC is expected back from the foundry in the summer. An extensive phase of testing is foreseen, with first focus on wafer level characterization, then detailed single-chip performance checks. First results are expected at fall 2010. Meanwhile batches of FE-I4 will be sent for bump-bonding to various sensor candidates (planar silicon, 3D silicon and diamond). A complex test system is being developed which will allow pursuing wafer level and single-chip tests, and will be available on this time scale.