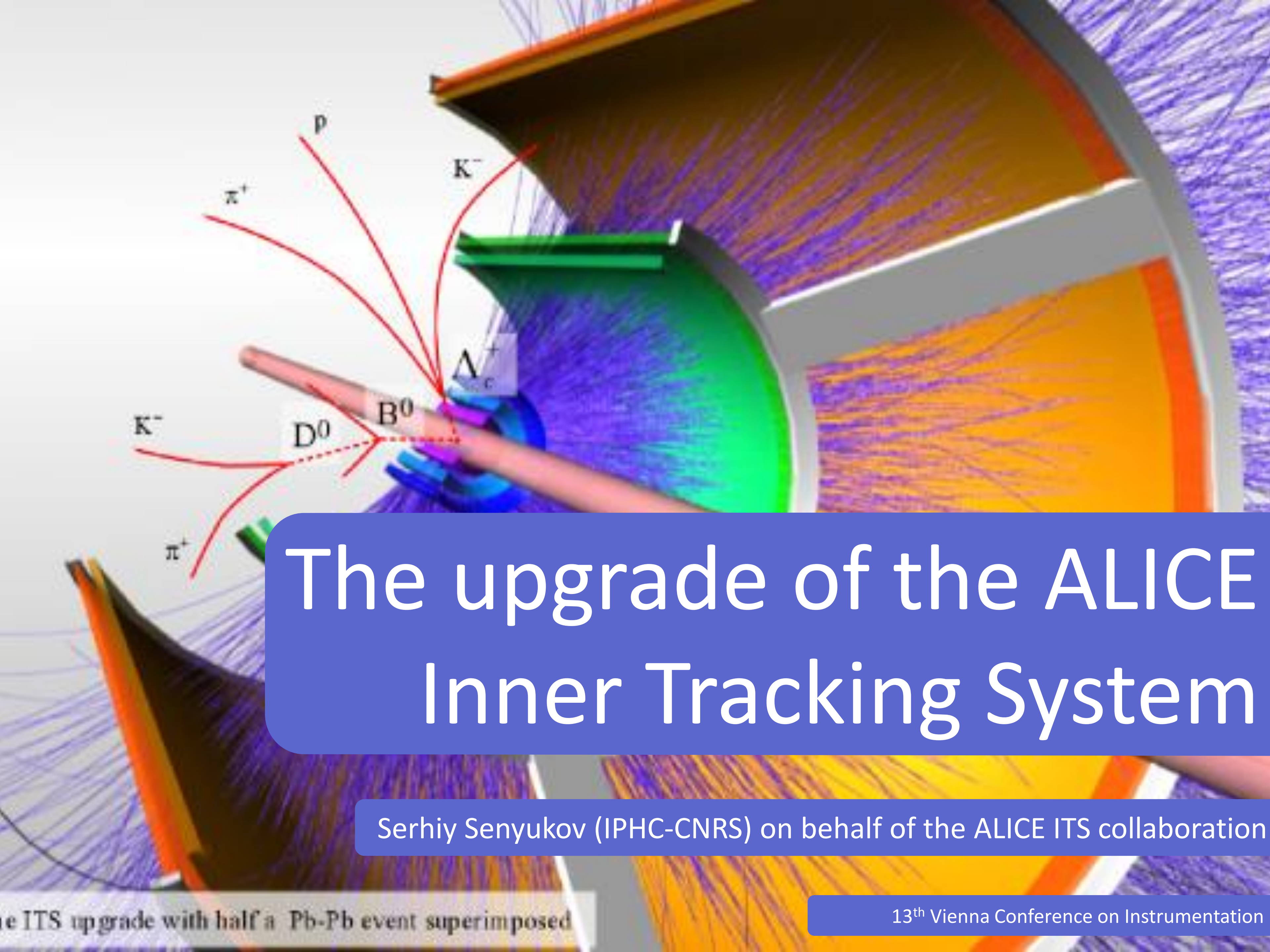
The upgrade of the ALICE Inner Tracking System



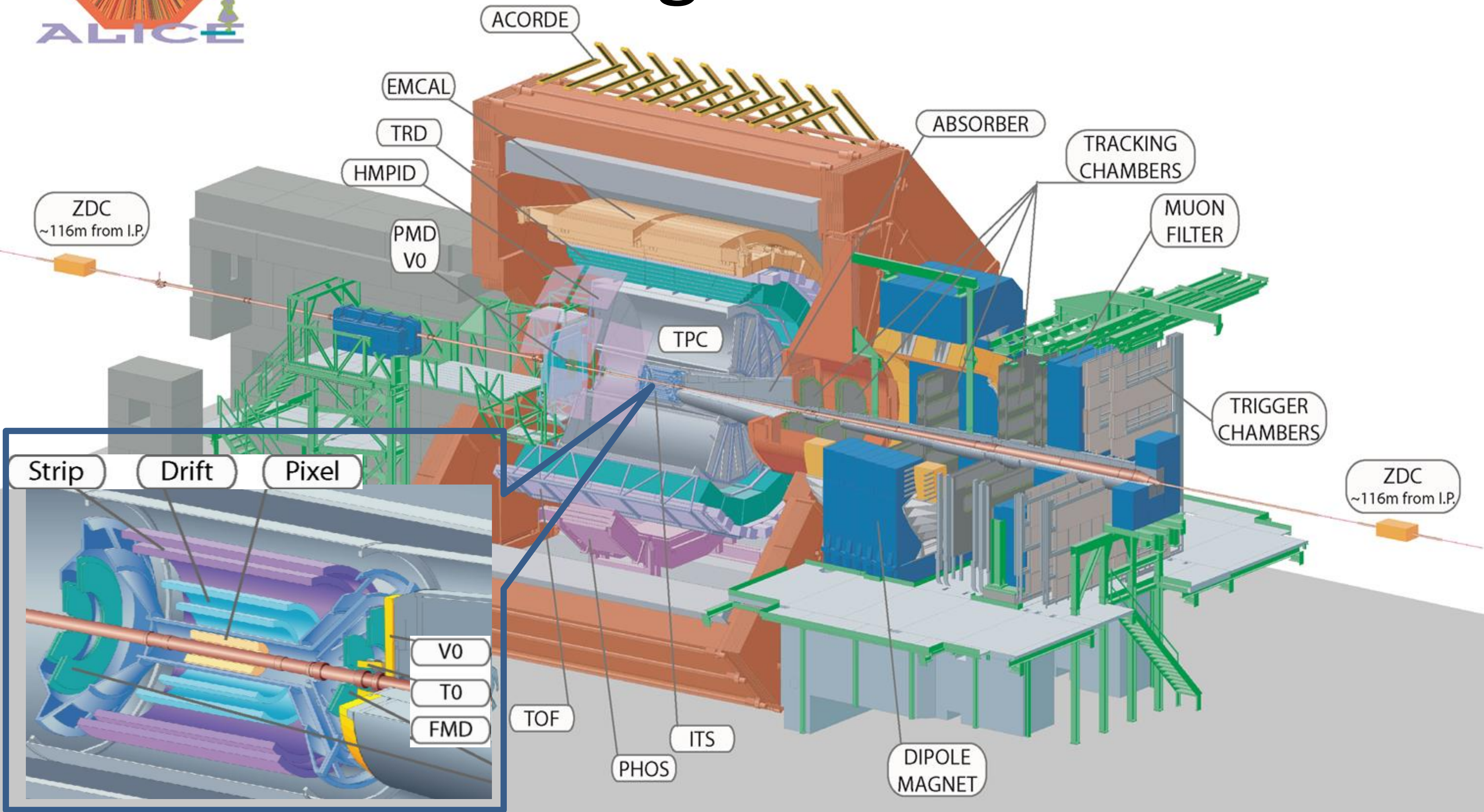
Serhiy Senyukov (IPHC-CNRS) on behalf of the ALICE ITS collaboration

13th Vienna Conference on Instrumentation

Outline

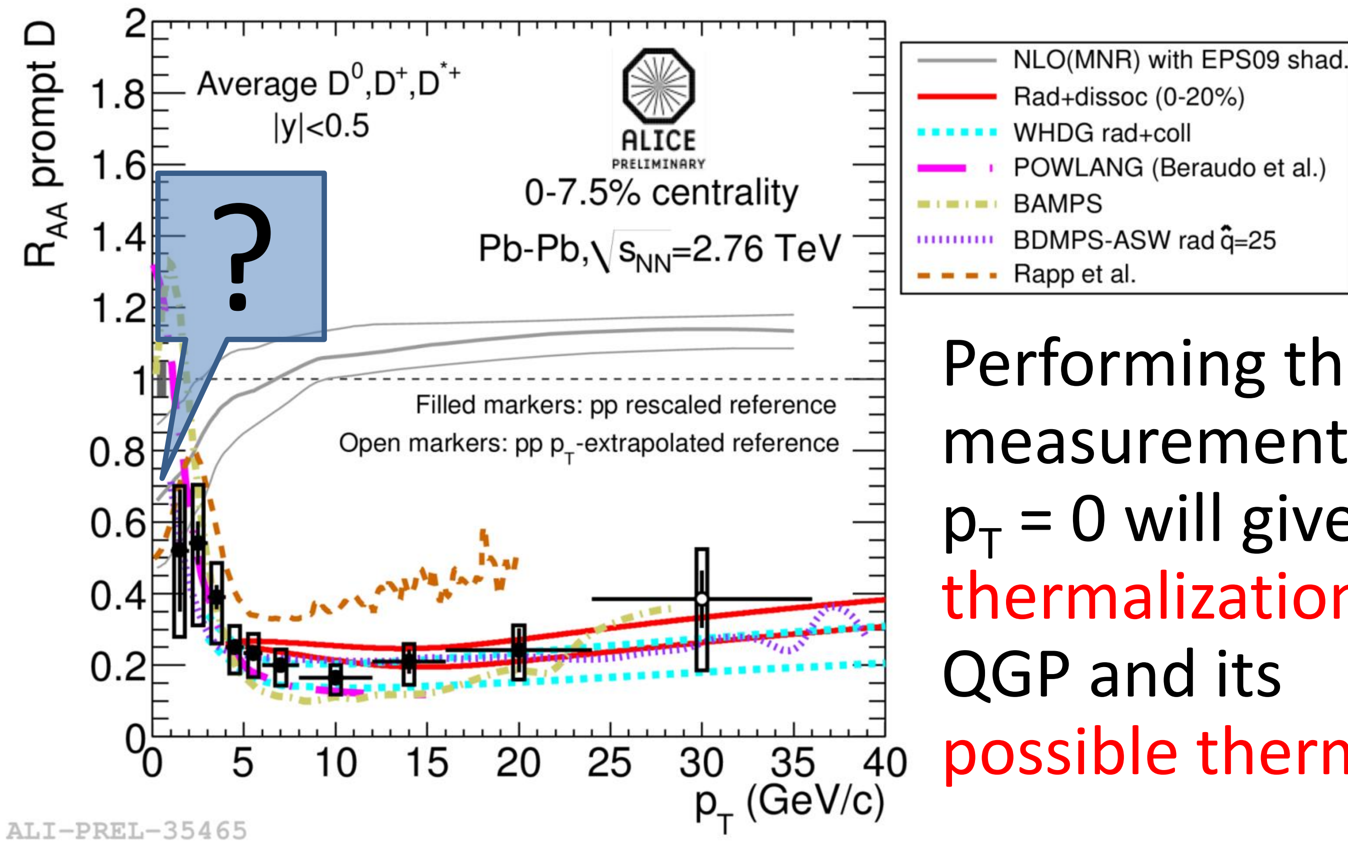
- Present ALICE detector and its physics results
- General ALICE upgrade in 2017-18
- New Inner Tracking System conceptual design
  - Expected detector performance
- From the concept to the final design:
  - Pixel chip developments
  - Mechanical integration
  - Cooling
- Conclusions

Present ALICE detector = = Tracking + Particle ID



ALICE physics results

Recently numerous measurements were performed including D mesons spectra in Pb-Pb and pp and their ratio R_{AA} giving information on charm energy loss inside Quark-Gluon Plasma

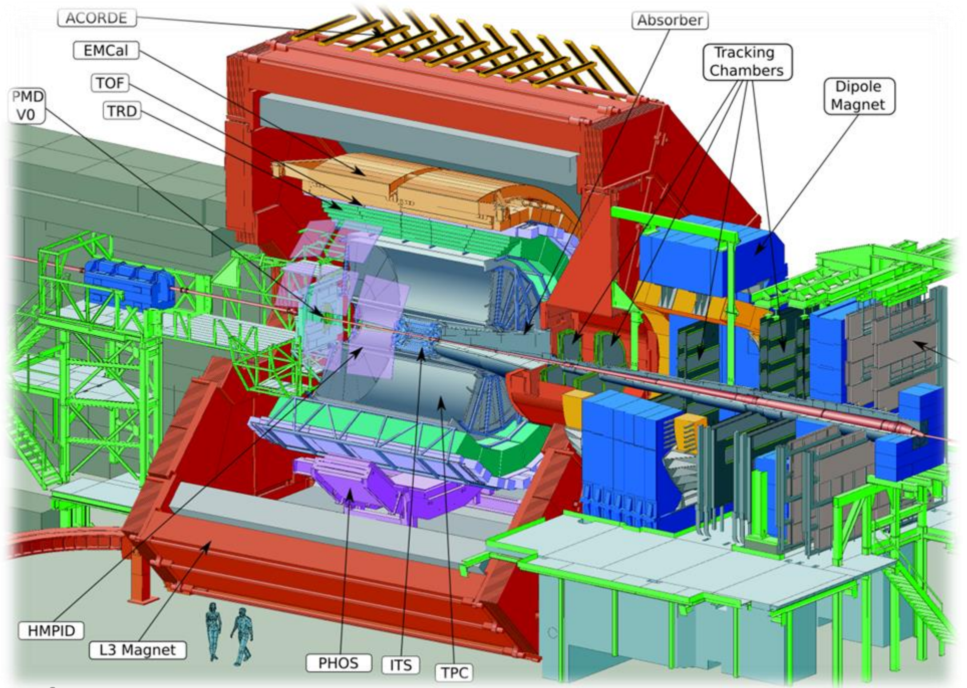


Performing these measurements down to $p_T = 0$ will give information on thermalization of charm in QGP and its possible thermal production.

General ALICE upgrade

- **Why:** improve the physics performance for:
  - Heavy flavor at low p_T
  - Quarkonia
  - Low-mass di-leptons
  - Heavy nuclear states
- **What:**
  - Smaller beam pipe: r_{out}=29.8 mm → 20 mm
  - <u>New highly-granular and low-mass ITS</u>
  - Continuous GEM readout of the TPC
  - New readout electronics of TOF, TRD, PHOS and Muon Spectrometer for high rate operation
  - New online and offline computing
- **When:** LHC LS2 (2017-18)

- **How:**
  - Better spatial resolution
  - Higher LHC luminosity: 6×10^{27} cm^{-2}s^{-1} → 50 kHz

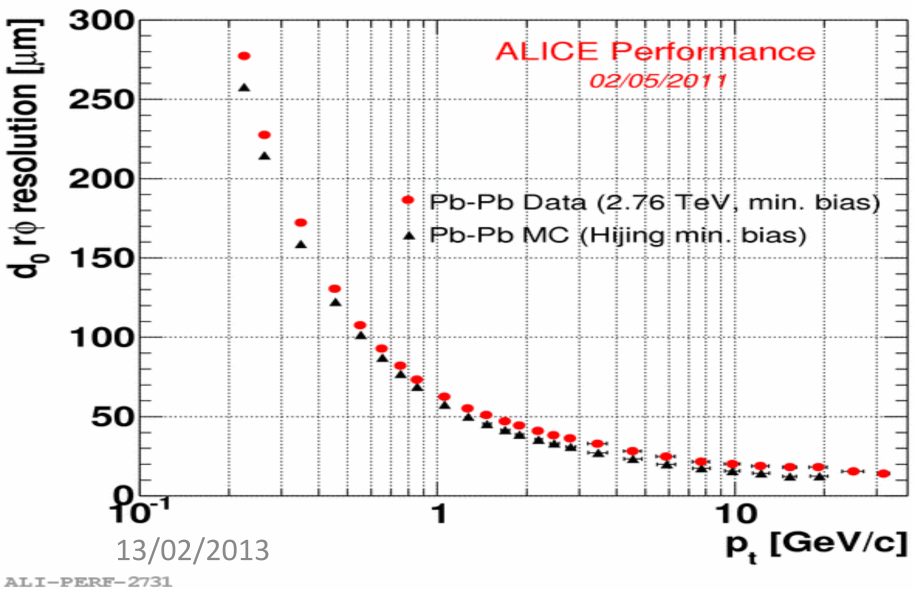


ITS upgrade

2007 → **2018**

- 6 layers: r_{min} = 39 mm
- Maximum readout rate (SDD) = 1 kHz

Type	$\sigma_{r\phi}$ [μm]	σ_z [μm]	X/X_0
2x pixel	12	100	1.14
2x drift	35	25	1.2
2x strips	20	830	0.83



- Better spatial resolution:
  - r_{min} = 22 mm
  - More layers
  - Smaller segmentation
  - Lower material budget
- Faster readout:
  - 1 kHz → 50 kHz in Pb-Pb
  - ~ 200 kHz in pp
- Radiation level:
  - 700 kRad + 10^{13} n_{eq} /cm^2 for the full integrated luminosity (innermost layer including a safety factor = 4)

Silicon particle detectors

- Hybrid pixels:
  - Mature technology
  - High radiation hardness
  - Pixel pitch: ~ 50 μm
  - Material budget: ~ 1 % X_0
    (100 + 50 μm total silicon thickness)
  - High production cost

- CMOS monolithic pixels:
  - Novel technology
  - Less radiation hard
  - Pixel pitch: ~ 20 μm
  - Material budget: ~ 0.3 % X_0
    (50 μm chip thickness)
  - Low production cost

- Silicon micro-strips:
  - Mature technology
  - Allows to measure dE/dx for the particle ID
  - Low resolution along beam direction
  - Suited only for the low track density (outermost layers)

Conceptual detector layouts:

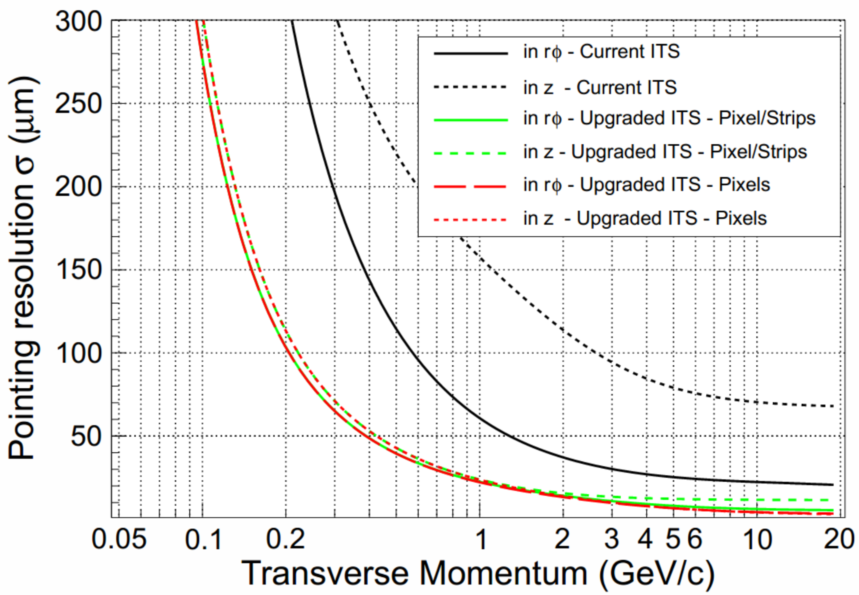
All pixels Pixels + Strips

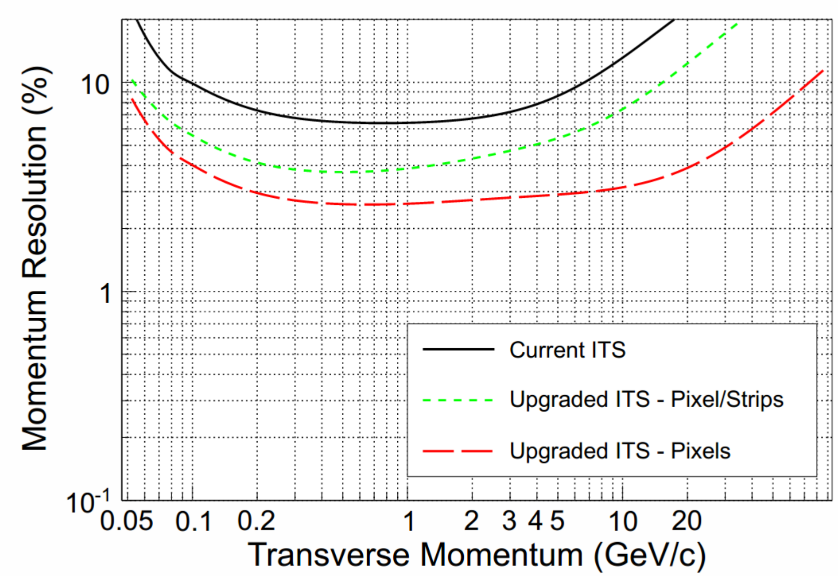
Layer	Type	R [cm]	±z [cm]	Intrinsic resolution [μm] rφ	Intrinsic resolution [μm] z	Material budget [% X_0]
	Beam pipe	2.0	-	-	-	0.22
1	Pixels	2.2	11.2	4	4	0.3
2	Pixels	2.8	12.1	4	4	0.3
3	Pixels	3.6	13.4	4	4	0.3
4	Pixels / Strips	20.0	39.0	4 / 20	4 / 830	0.3 / 0.83
5	Pixels / Strips	22.0	41.8	4 / 20	4 / 830	0.3 / 0.83
6	Pixels / Strips	41.0	71.2	4 / 20	4 / 830	0.3 / 0.83
7	Pixels / Strips	43.0	74.3	4 / 20	4 / 830	0.3 / 0.83

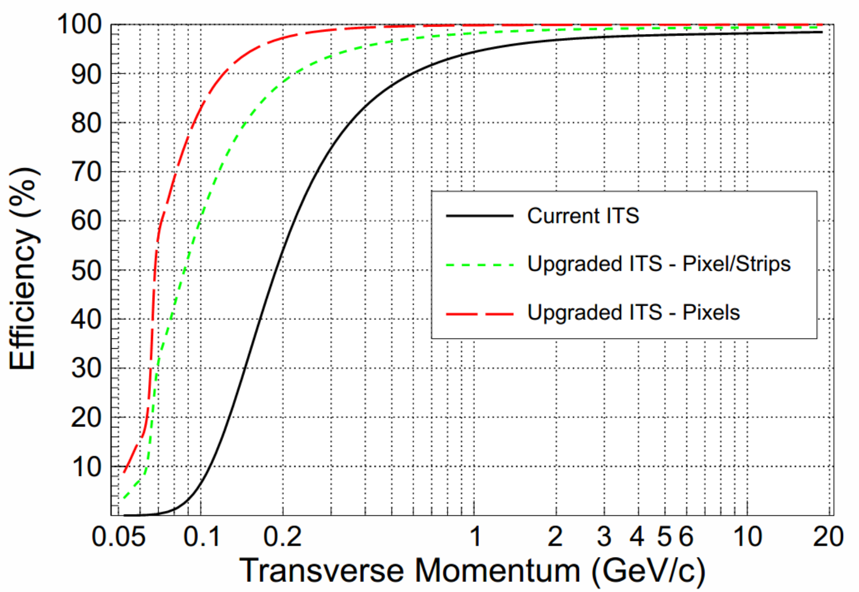
in the table above the intrinsic resolution and the material budget of pixel layers refer to CMOS monolithic pixels

Expected improvements of the detector performance:

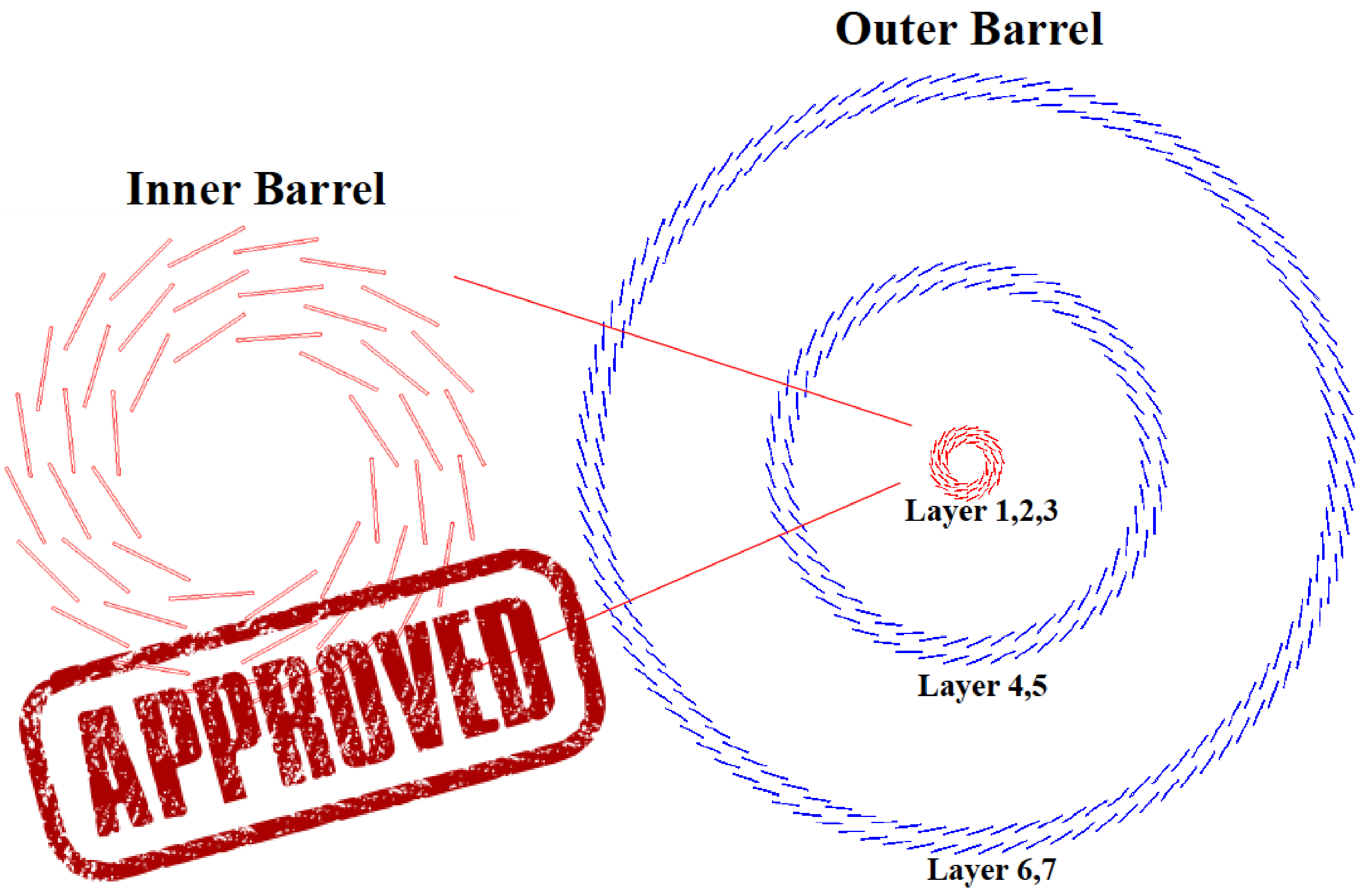
- 3 × better pointing resolution
- 2.5 × better p_T resolution
- 2 × better tracking efficiency at low p_T



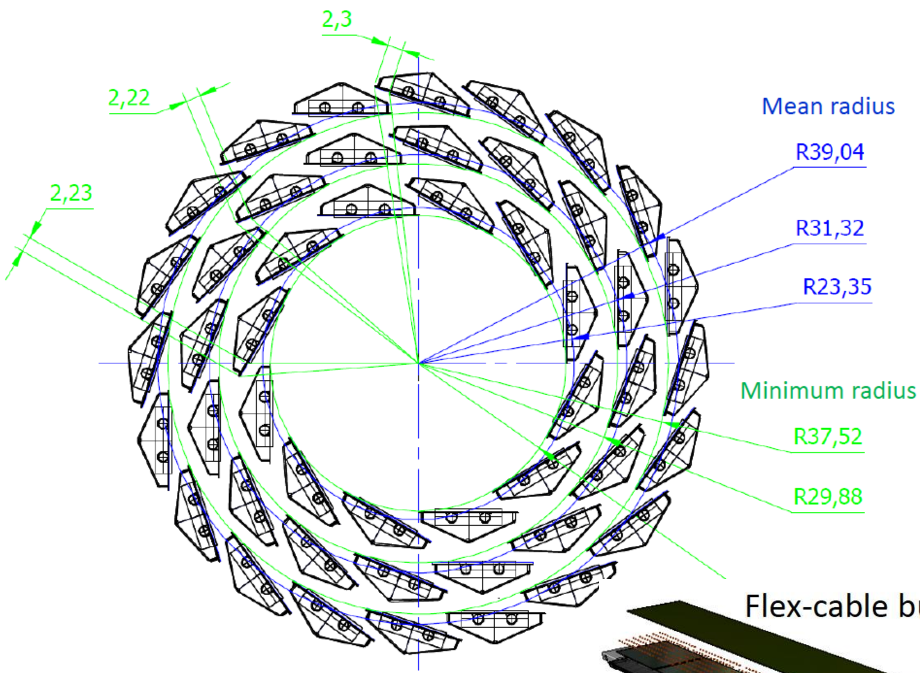




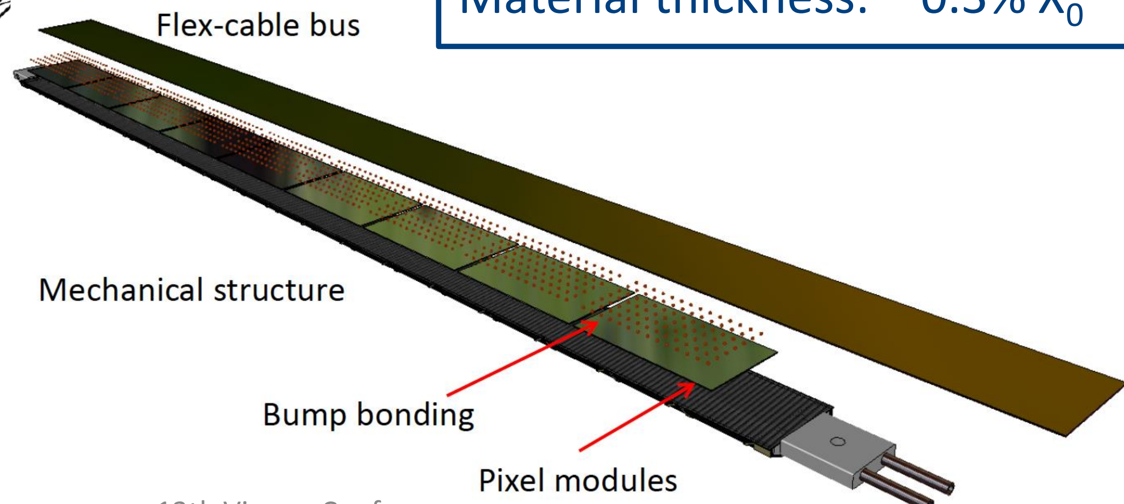
From the concept to the final design



Inner barrel design

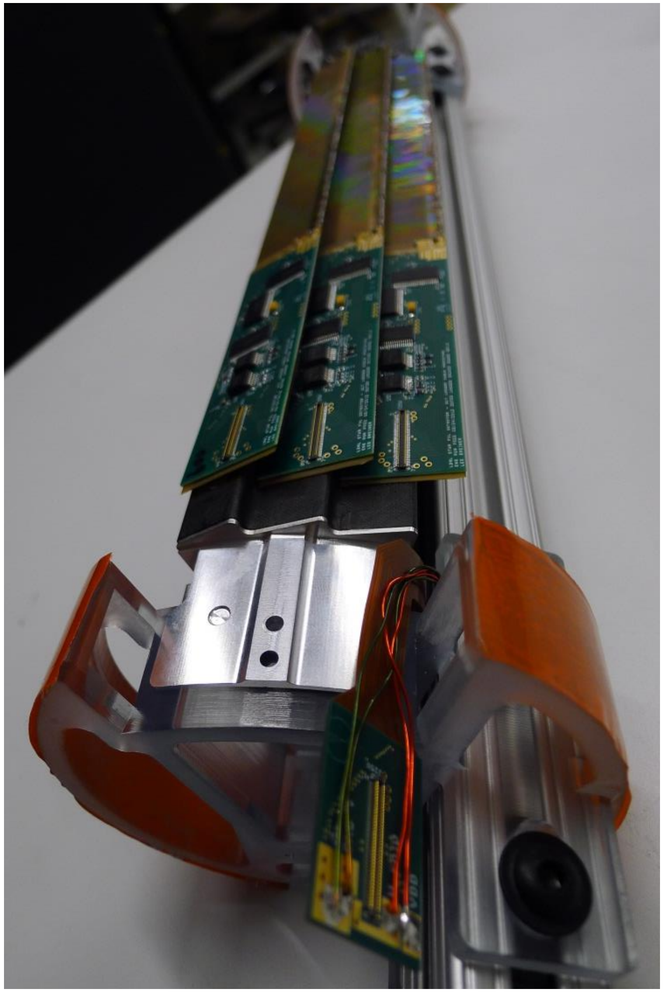


- Inner Barrel (IB): 3 layers pixels
- Radial position (mm): 22,28,36
- Length in z (mm): 270
- Nr. of staves: 12 + 16 + 20 = 48
- Nr. of chips/stave: 9
- Pixel size: ~ 20 µm x 20 (30) µm
- Material thickness: ~ 0.3% X_0



Pixel chip technology

- Experience of the STAR-PXL with 0.35 µm CMOS technology made us to consider CMOS pixel sensors (CPS)
- Smaller feature size was needed to meet the radiation hardness and speed requirements of the ITS upgrade
- In 2012 *TowerJazz 0.18 µm* CMOS process has been validated *(see talk by J. Baudot)*

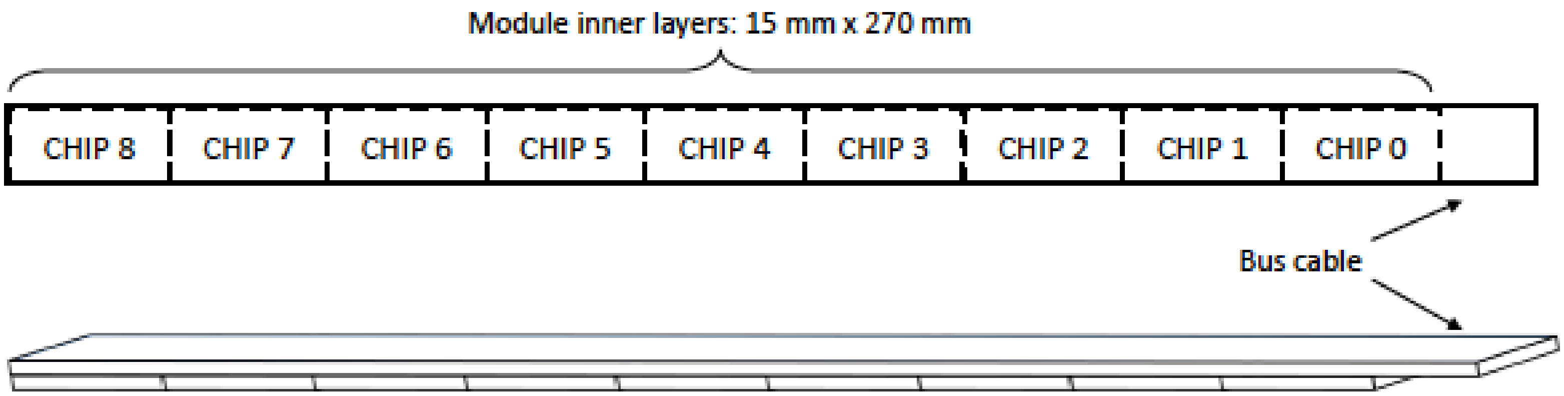


First sector of the STAR-PXL
(Photo by courtesy of Leo Greiner (LBNL)

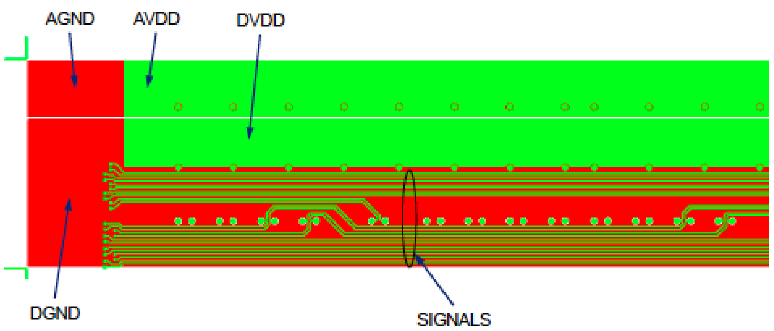
Pixel chip architecture

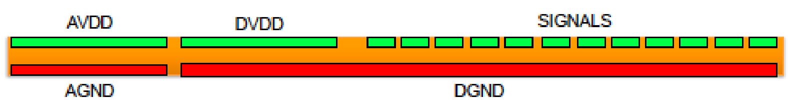
1. **MISTRAL** (IPHC Strasbourg) – baseline (most mature and advanced)
   - Rolling shutter with in-pixel CDS, column-level discriminator, 2 rows parallel RO
   - Integration time: 30 μs
   - Power ≤ 400 mW/cm^2 *(see talk of Jerome Baudot)*
2. **ASTRAL** (IPHC Strasbourg)
   - Rolling shutter with in-pixel CDS, in-pixel discriminators + data driven readout
   - Integration time: 15 μs
   - Power ≤ 350 mW/cm^2 *(see talk of Jerome Baudot)*
3. **Parallel Rolling Shutter** (RAL)
   - Based on previous development.
   - Integration time: ~40 μs
   - Power < 200 mW/cm^2
4. **In-pixel discriminator + data driven readout** (CERN)
   - shaping time ~2 μs, readout time ~4 μs; < 100 mW / cm^2

Stave and bus cable design



- Bus cable:
  - Al + polyimide + Al
- Chip-On-Flex connections:
  - BGA balls
  - Laser soldering





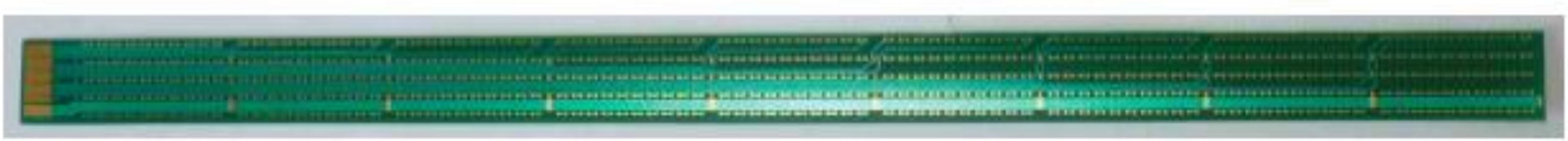
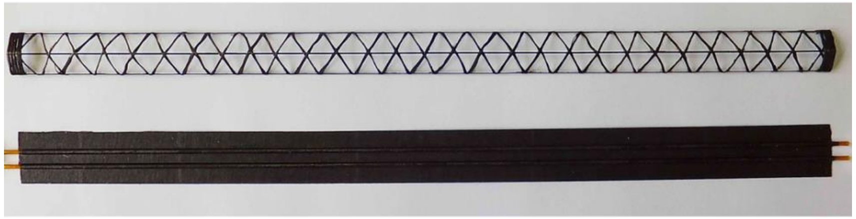


Figure 4.25: Picture of one polyimide flex cable.

See the poster #63 by G. Feofilov

Inner barrel stave

Wound Truss Structure plus Carbon Plate with Embedded Pipes



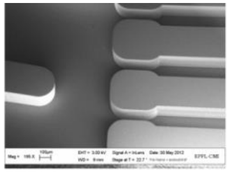
Weight	1.8 grams
X/X0	*0.31%*
Cooling capacity	*<25°C at 0.3W/cm2*
	<30°C at 0.5W/cm2

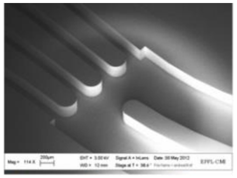
Wound Truss Structure with Pipes

Weight	1.4 grams
X/X0	*0.26%*
Cooling capacity	*<32°C at 0.3W/cm2*

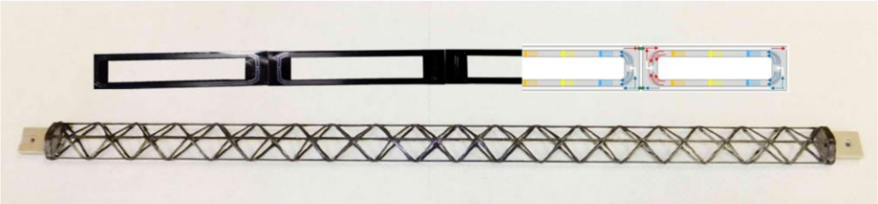
Wound truss structure +polyimide micro-channel

Weight	1.7 grams
X/X0	*0.30%*
Cooling capacity	*<22°C at 0.3W/cm2*
	<25°C at 0.5W/cm2



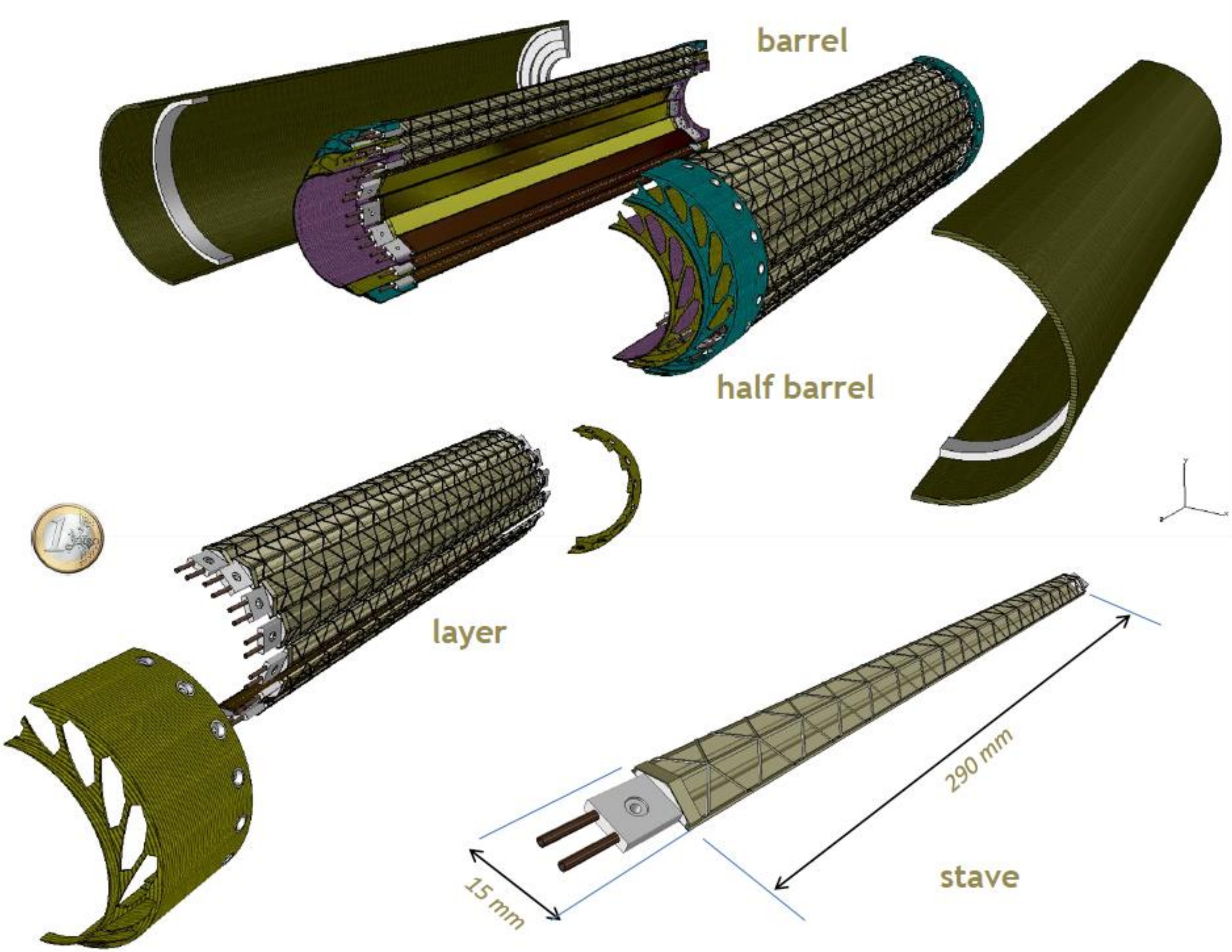


Wound truss structure +Silicon micro-channel

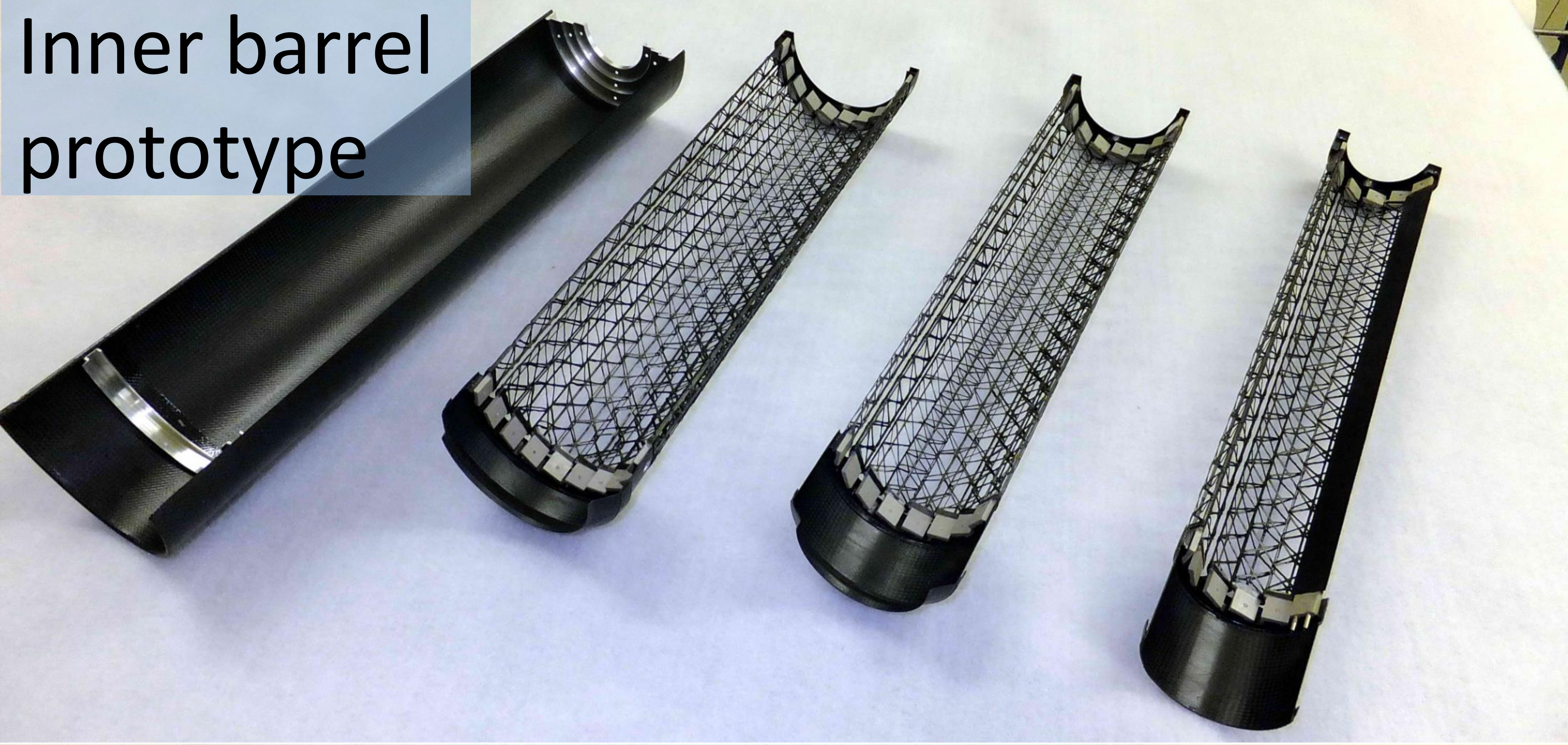


Weight	*tbd*
X/X0	*tbd*
Cooling capacity	*tbd*

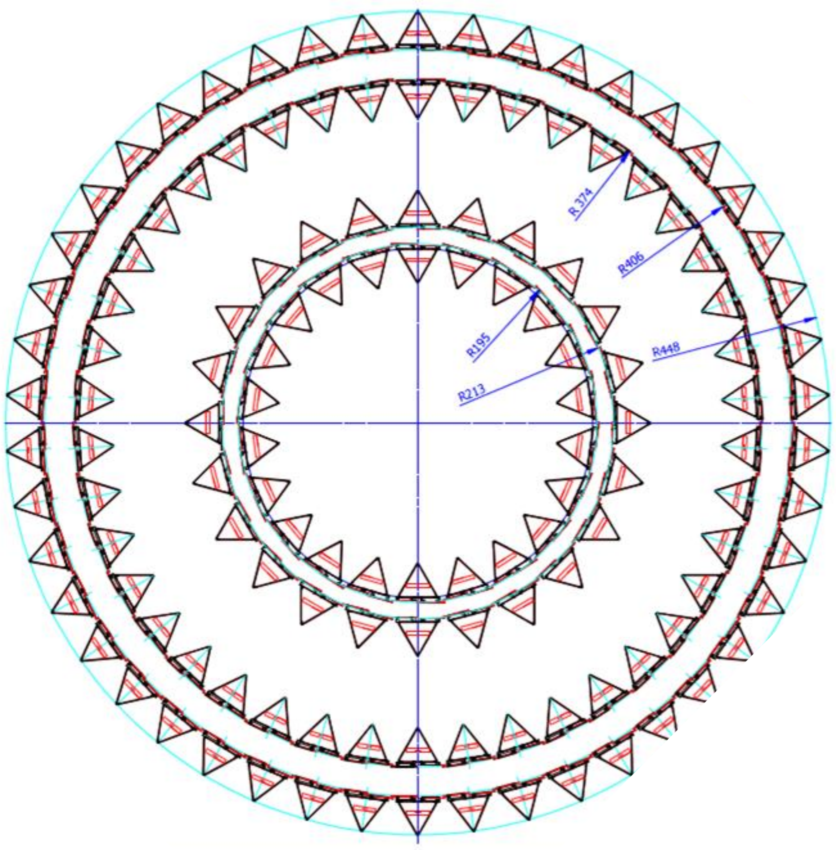
Inner barrel assembly



Inner barrel prototype



Outer barrel design (in progress)



Outer Barrel: 4 layers pixels (baseline)

Radial position (mm): 200, 220, 410, 430

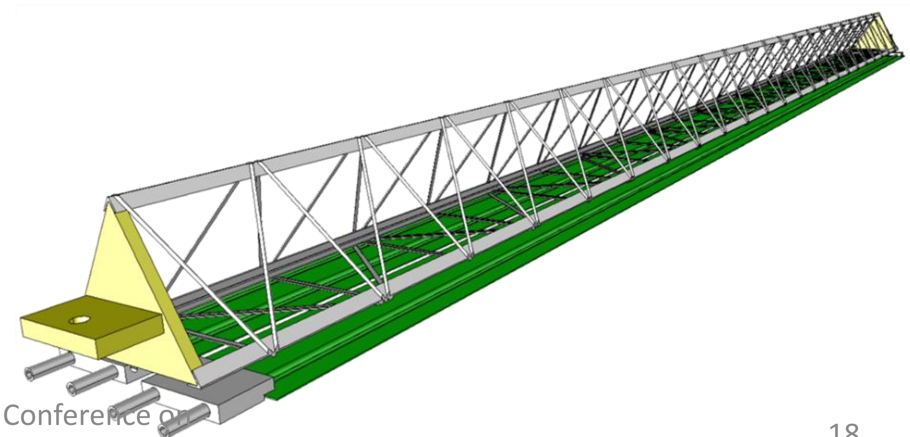
Length in z (mm): 843, 1475

Nr. of staves: 48 + 52 + 96 + 102 = 298

Nr. of chips/stave: 28, 28, 52, 52

Pixel size: 20×20 μm^2 or bigger

Material thickness: ~ 0.8% X_0



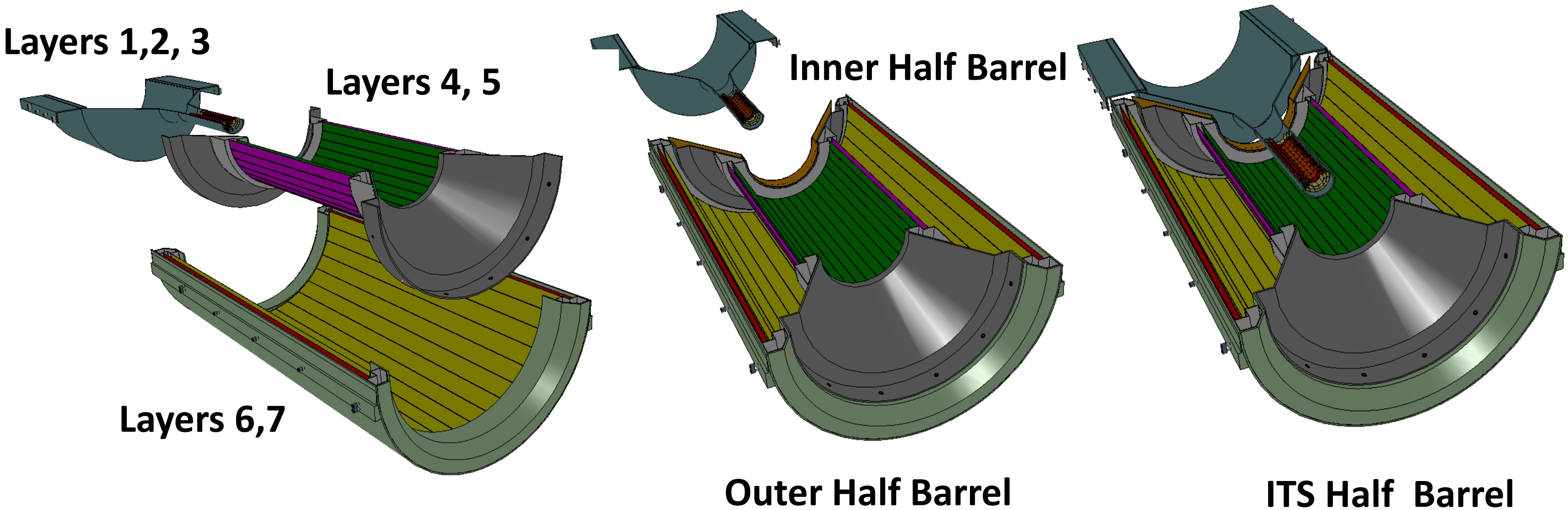
Pixels Vs. Strips

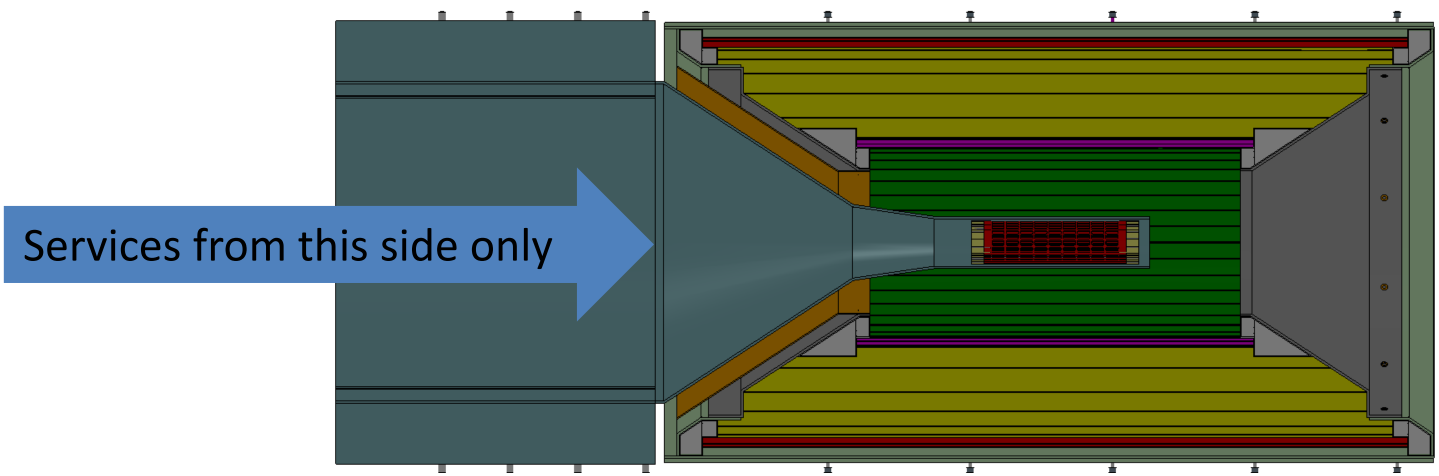
The choice for the outer barrel will be based on:

- the outcome of the ongoing studies about the benefit for some specific physics signal of the PID with strips
- technical feasibility of large area pixel layers ~10 m^2
  - power distribution
  - cooling
  - mechanical integration
- overall cost

Pixel chip with larger pitch and low power for the outer layers is under consideration

Final ITS integration





Conclusions and future plans

- Conceptual design of the new ALICE ITS:
  - with the single point resolution $\sigma_{r\phi} = \sigma_Z = 4\ \mu m$
  - and material budget: 0.3 % X_0 per layer
  - ensuring 3x better spatial resolution
  - and supporting high luminosity: $L = 6\times10^{27}\ cm^{-2}s^{-1}$

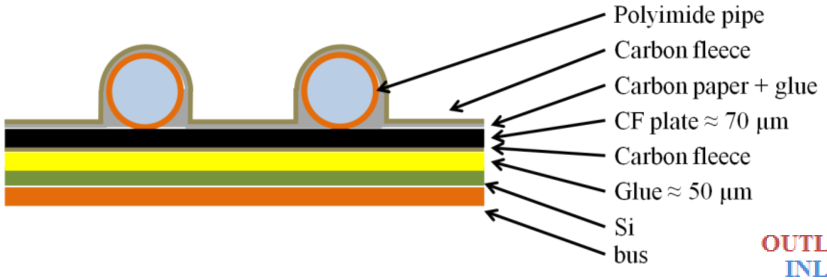
  has been approved by the LHCC
  as a part of the general ALICE upgrade
- Challenging R&D is in progress addressing:
  - stringent requirements of
    resolution × readout speed × power consumption
  - system integration of the large surface pixel detector
- TDR to be ready by the end of Summer 2013

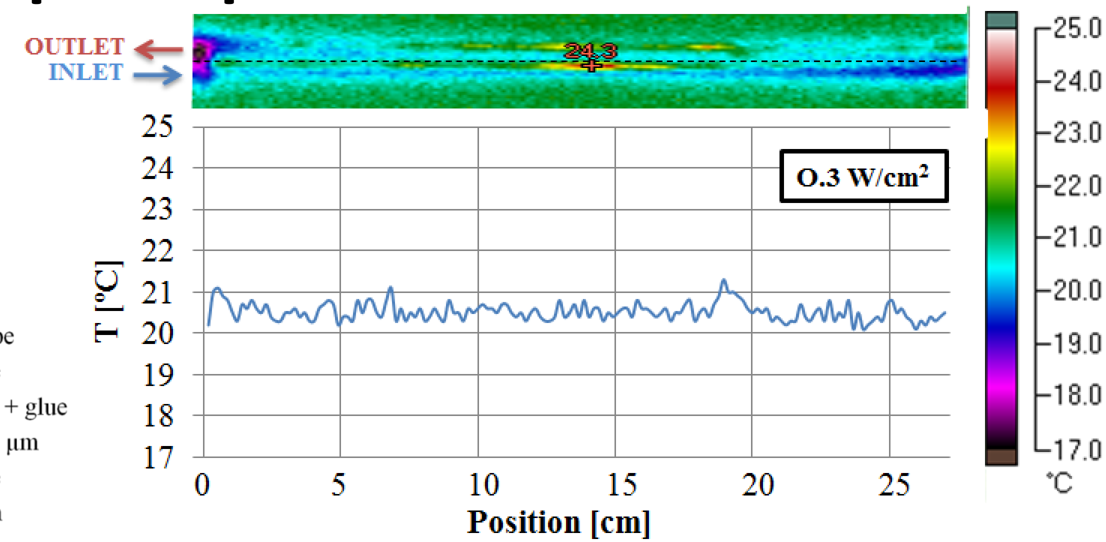
BACKUP SLIDES

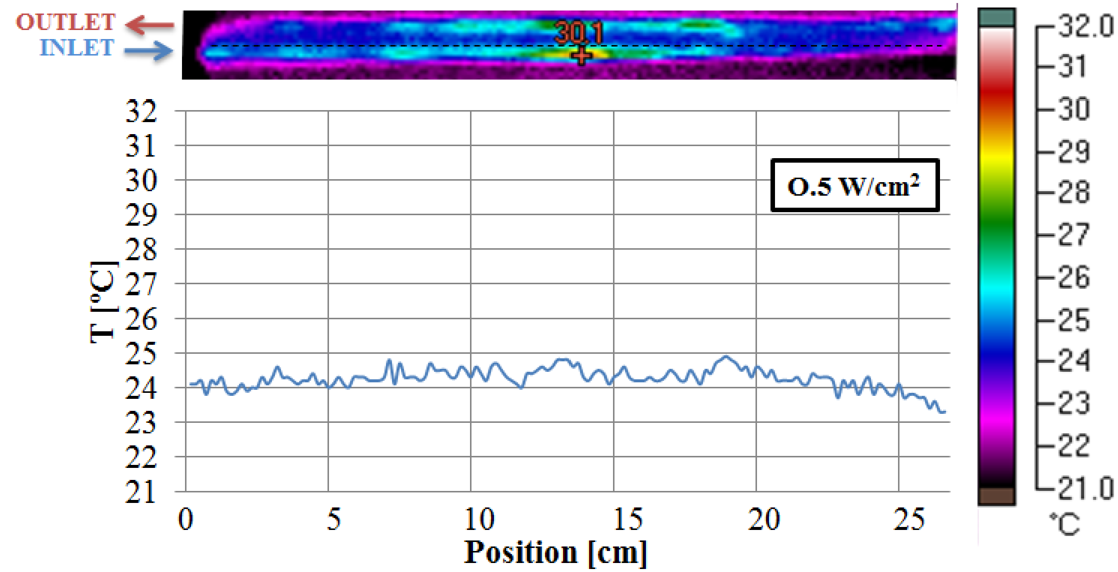
New ITS layout summary

Layer	Radius [mm]	Length [mm]	Staves	Chips/stave	Material budget [% X_0]
beam pipe	20	-			0.22
1	22		12		0.3
2	28	270	16	9	0.3
3	36		20		0.3
4	200	843	48	28	0.8
5	220		52		0.8
6	410	1475	96	52	0.8
7	430		102		0.8

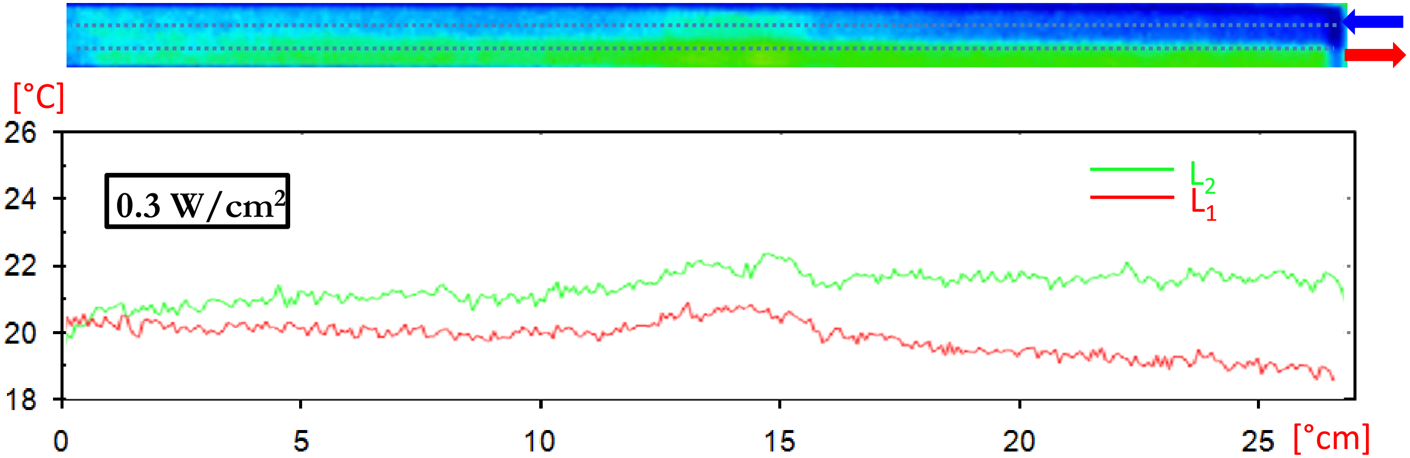
Cooling pipes performance

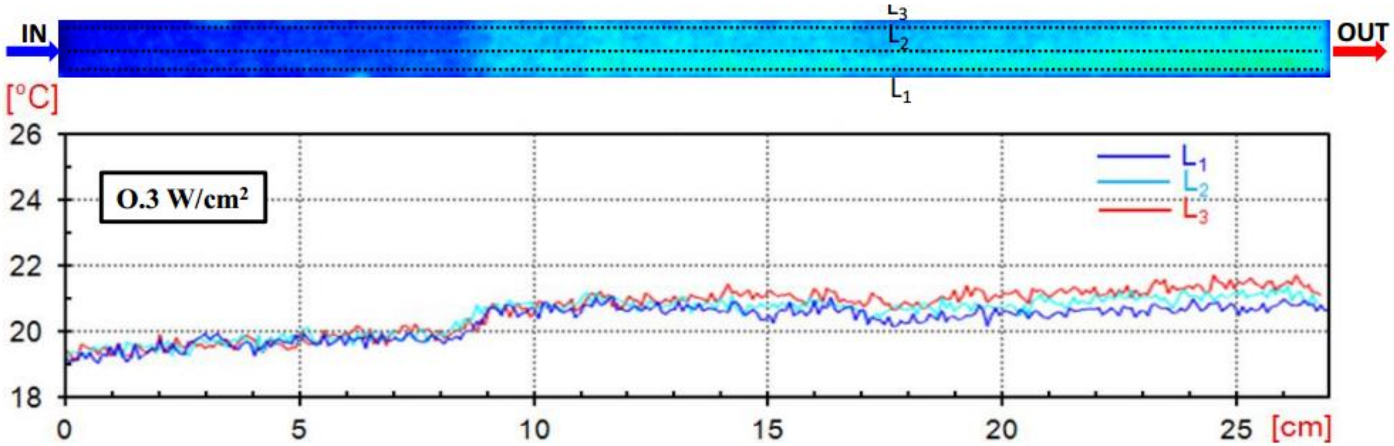






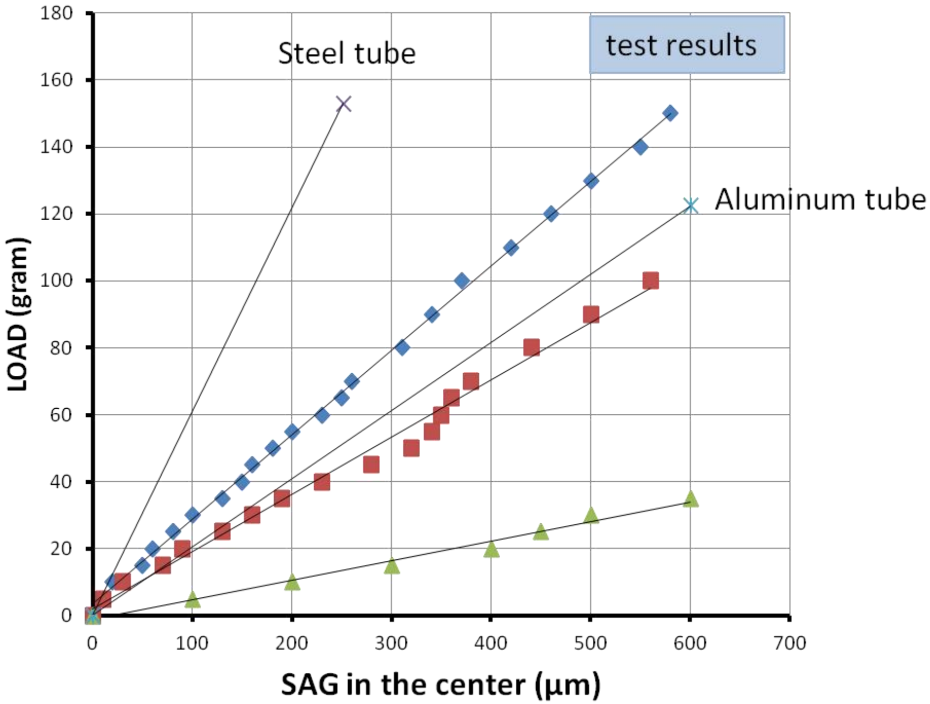
Polyimide micro-channels cooling performance

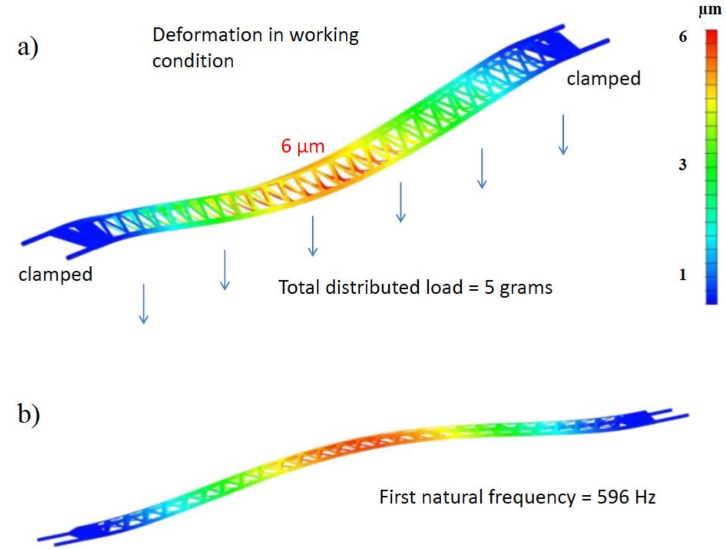


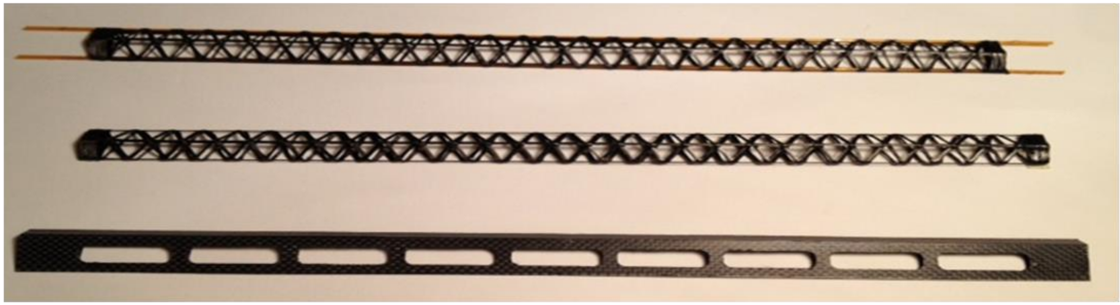


Stave stiffness tests

STRUCTURE STIFFNESS *TEST*







◆ Wound truss + pipes

■ Wound truss

▲ Open shell