Operation and Monitoring of the CMS Regional Calorimeter Trigger Hardware

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Abstract

The electronics for the Regional Calorimeter Trigger (RCT) of the Compact Muon Solenoid Experiment (CMS) have been produced, tested, and installed. The RCT hardware consists of one clock distribution crate and 18 double-sided crates containing custom boards, ASICs, and backplanes. The RCT receives 8-bit energies and a data quality bit from the HCAL and ECAL Trigger Primitive Generators (TPGs) and sends it to the CMS Global Calorimeter Trigger (GCT) after processing. Integration tests with the TPG and GCT subsystems have been successful.

Installation is complete and the RCT is integrated into the Level-1 Trigger chain. Data taking has begun using detector noise, cosmic rays, proton-beam debris, and beam-halo muons [1]. The operation and configuration of the RCT is a completely automated process. The tools to monitor, operate, and debug the RCT are mature and will be described in detail, as well as the results from data taking with the RCT.

I. Introduction

The Compact Muon Solenoid (CMS) is a general-purpose detector operating at the Large Hadron Collider (LHC). It is in the final stages of commissioning at the European Laboratory for Particle Physics (CERN) near Geneva, Switzerland. This large detector is sensitive to a wide range of new physics at the high proton-proton center of mass energy $\sqrt{s}$ =14 TeV [2]. First beam was seen September 2008 [1].

At the LHC design luminosity of 10^{34} cm^{-2} s^{-1}, a beam crossing every 25 ns contains on average 17.3 events. These 10^9 interactions per second must be reduced by a factor of 10^7 to 100 Hz, the maximum rate that can be archived by the on-line computer farm. This will be done in two steps. The level-1 trigger first reduces the rate to 75 kHz, and then a High Level Trigger (HLT), using an on-line computer farm, handles the remaining rate reduction.

The CMS level-1 electron/photon, τ-lepton, jet, and missing transverse energy trigger decisions are based on input from the level-1 Regional Calorimeter Trigger (RCT) [3]. The RCT plays an integral role in the reduction of the proton-proton interaction rate (10^9 Hz) to the High Level Trigger input rate (10^5 Hz) while separating physics signals from background with high efficiency. The RCT receives input from the brass and scintillator CMS hadron calorimeter (HCAL) and $PbWO_4$ crystal electromagnetic calorimeter (ECAL), that extend to |η|=3. An additional hadron calorimeter in the very forward region (HF) extends coverage to |η|=5. A calorimeter trigger tower is defined as 5x5 crystals in the ECAL of dimensions 0.087x0.087 (ΔφxΔη), which corresponds 1:1 to the physical tower size of the HCAL.

II. RCT Hardware

A. *Primary RCT Cards*

Eighteen crates of RCT electronics process data for the barrel, endcap, and forward calorimeters. There is another crate for LHC clock distribution. These are housed in the CMS underground counting room adjacent to and shielded from the underground experimental area.

Twenty-four bits comprising two 8-bit calorimeter energies, two energy characterization bits, a LHC bunch crossing bit, and 5 bits of error detection code are sent from the ECAL, HCAL, and HF calorimeter electronics to the nearby RCT racks on 1.2 Gbaud copper links. This is done using one of the four 24-bit channels of the Vitesse 7216-1 serial transceiver chip on calorimeter output and RCT input, for 8 channels of calorimeter data per chip. The RCT V7216-1 chips are mounted on mezzanine cards located on each of 7 Receiver Cards and the single Jet/Summary Card for all 18 RCT crates. The eight mezzanine cards on the Receiver Cards are for the HCAL and ECAL data and the single mezzanine card located on the Jet/Summary Card is for receiving the HF data. The V7216-1 converts the 1.2 Gbaud serial data to 120 MHz TTL parallel data, which is then deskewed, linearized, and summed before transmission on a 160 MHz ECL custom backplane to 7 Electron Isolation Cards and one Jet/Summary Card. The Jet/Summary Card receives the HF data and sends the regional E_T sums and the electron candidates to the Global Calorimeter Trigger (GCT). The GCT implements the jet algorithms and forwards the 12 jets to the Global Trigger (GT).

The Receiver Card (shown in Figure 1), in addition to receiving and aligning calorimeter data on copper cables using the V7216-1, shares data on cables between RCT crates. Lookup tables are used to convert the incoming calorimeter energy into several scales and set bits for electron identification. Adder blocks begin the energy summation tree, reducing the data sent to the 160 MHz backplane.

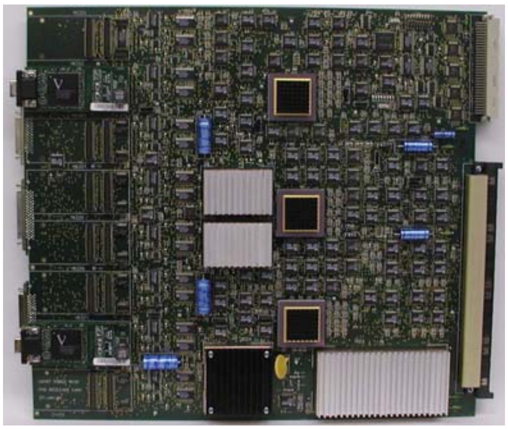

Figure 1: Front of a Receiver Card showing two Receiver Mezzanine Cards in place and Adder ASICs.

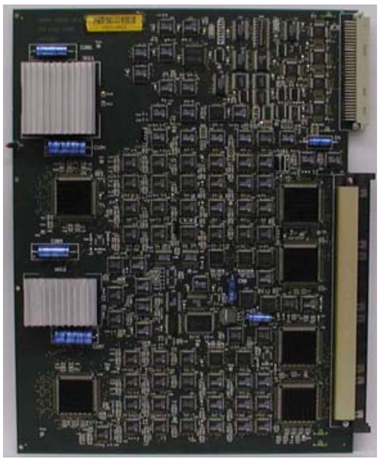

Figure 2: Electron Identification Card showing 4 Sort ASICs (right) and 2 EISO ASICs (left).

The Electron Isolation Card (shown in Figure 2) receives data for 32 central towers and 28 neighboring trigger towers via the backplane. The electron isolation algorithm is implemented in the Electron Isolation ASIC described below. Four electron candidates are transmitted via the backplane to the Jet/Summary (J/S) Card. The electrons are sorted in Sort ASICs on the J/S Card and the top 4 of each type are transmitted to the GCT for further processing. The J/S Card also receives E_T sums via the backplane, and forwards them and two types of muon identification bits (minimum ionizing and quiet bits – described later) to the GCT. A block diagram of this dataflow is shown in Fig. 3.

To implement the algorithms described above, five high-speed custom Vitesse ASICs were designed and manufactured, a Phase ASIC, an Adder ASIC, a Boundary Scan ASIC, a Sort ASIC, and an Electron Isolation ASIC [4]. They were produced in Vitesse FX™ and GLX™ gate arrays utilizing their sub-micron high integration Gallium Arsenide MESFET technology. Except for the 120 MHz TTL input of the Phase ASIC, all ASIC I/O is 160 MHz ECL.

The Phase ASICs on the Receiver Card align and synchronize the data received on four channels of parallel data from the Vitesse 7216 and check for data transmission errors. The Adder ASICs sum up eight 11-bit energies (including the sign) in 25 ns, while providing bits for overflows. The Boundary Scan ASIC copies and aligns tower energies for e/γ algorithm data sharing and aligns and drives them to the backplane. Four 7-bit electromagnetic energies, a veto bit, and nearest-neighbor energies are handled every 6.25 ns by the Electron Isolation ASICs, which are located on the Electron Isolation Card. Sort ASICs are located on the Electron Isolation Card, where they are used as receivers, and are located on the J/S Cards for sorting the e/γ candidates. All these ASICs have been successfully tested on the boards described, and procured on in the full quantities needed for the system, including spares. The boards described have been produced using these ASICs and sufficient quantity has been obtained to fill 18 crates and create a stock of spares.

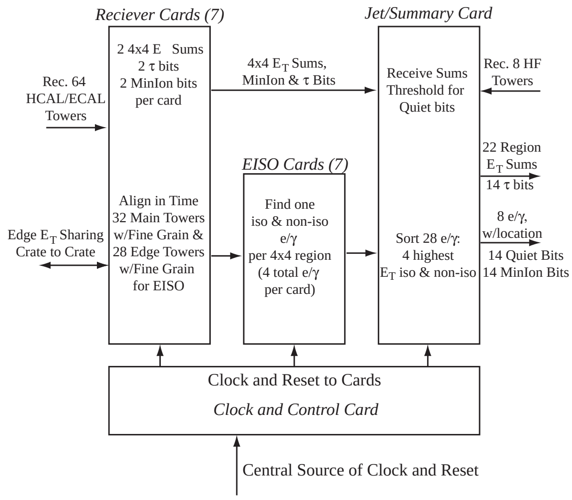

Figure 3: Dataflow diagram for an RCT crate, showing data received and transferred between cards on the 160 MHz differential ECL backplane. Brief explanations of the card functionality are shown. For more details see the text or ref. [3].

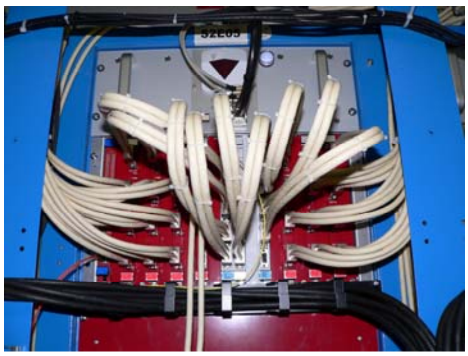

Figure 4: The Master Clock Crate and cards. Central is the CIC, receiving the fibre from the TTC system, and moving outwards, 2 CFCm cards, and 7 CFCc cards.

A Master Clock Crate (MCC) and cards are centrally located in the 10 RCT racks to provide clock and control signal distribution (Figure 4). Input to the system is provided by the CMS Trigger Timing and Control (TTC) system [5]. This provides the LHC clock, Bunch Crossing

Zero (BC0), and other CMS control signals via a optical fibre from a TTCci (TTC input card) which can internally generate or receive these signals from either a Local Trigger and Control board (LTC) or the CMS Global Trigger.

The MCC includes a Clock Input Card (CIC) with a LHC TTCrm mezzanine board [5] to receive the TTC clocks and signals via the fibre and set the global alignment of the signals. The CIC feeds fan-out cards, a Clock Fan-out Card Midlevel (CFCm) and a Clock Fan-out Card to Crates (CFCc) to align and distribute the signals to the individual crates via low-skew cable. Adjustable delays on these 2 cards allow fine-tuning of the signals to the individual crates.

III. Input and Output of the RCT

A. *Trigger Primitive Generators - Input*

The HCAL Trigger Readout (HTR) Boards and the ECAL Trigger Concentrator Cards (TCCs) provide the input to the RCT using a Serial Link Board (SLB), a mezzanine board with the V2716-1 mounted on it. The SLB is configurable, with two Altera Cyclone® FPGAs for data synchronization at the V2716-1, Hamming code calculation, FIFOs, and histogramming. The clocking for the SLB is separate from the HTR and TCC primary clocking to ensure data alignment at the RCT. The HTR can have up to 6 SLBs and receives data from the front end on fibres into its front panel. The TCC has up to 9 SLBs and also receives front-end data via a fibre to its front panel.

B. *GCT Source Cards – Output*

Each RCT crate is connected to GCT Source Cards, which convert the parallel ECL output of the RCT to optical, so that it may be sent easily to the lower floor of USC55. They are located in the RCT racks, directly above the RCT crates.

IV. Operation and Monitoring

A. *Commissioning the RCT at CMS*

Installation of the RCT is complete. The RCT has 10 racks that hold a total of 21 RCT crates, 6 GCT Source Card Crates, and a crate for clock distribution to the SLBs (See Figure 5). The MCC and eighteen of the 20 standard RCT crates are part of the final system. The remaining 2 RCT crates will be used for local testing and storage.

B. *Detector Slow Control and Rack Monitoring System*

A custom monitoring system has been installed in each RCT rack. This system, at the heart of which is a Rack Monitor Card (RMC), monitors the status of the power supplies, fans and crate temperatures. A serial port on the card is attached to a serial-to-ethernet connection. PVSS [6], an object-oriented process visualization and control system, is used for the software interface to the RMC. Figure 6 shows a sample control panel for one of the racks. This software provides Detector Slow Control (DCS) and on-line monitoring of the system. System variables, such as current and temperature are histogrammed and stored in a database for later access. The entire system is integrated with CMS's central DCS and the alarms and alerts are sent and recorded at a global level.

Figure 5: The front of the RCT Racks. Additional, temporary cables seen are for testing.

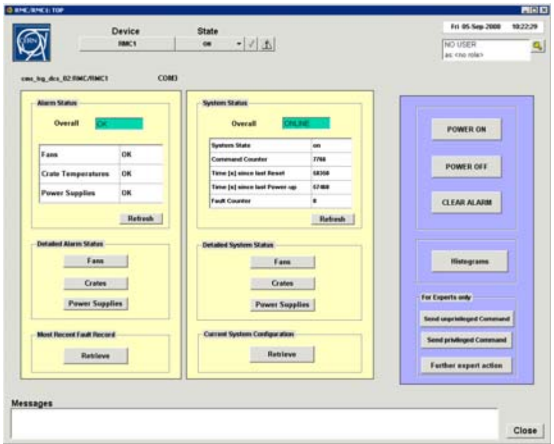

Figure 6: PVSS control panel for one RCT rack. From right to left are Alarm Status, System Status, and control and histograms.

C. *RCT Trigger Supervisor*

The Trigger Supervisor (TS) is an online framework to configure, test, operate, and monitor the trigger components and to manage communications between trigger systems [7]. Individual cells are set up for each system, with a central cell interacting with multiple systems at one time using SOAP [8] commands.

The RCT Trigger Supervisor enables system configuration via a pre-defined key and state machine. For data taking this is done for all detector subsystems, including trigger, with CMS Run Control. For internal and interconnection tests configuration can be done centrally or by hand. Figure 7 shows the panel for key input and the state machine.

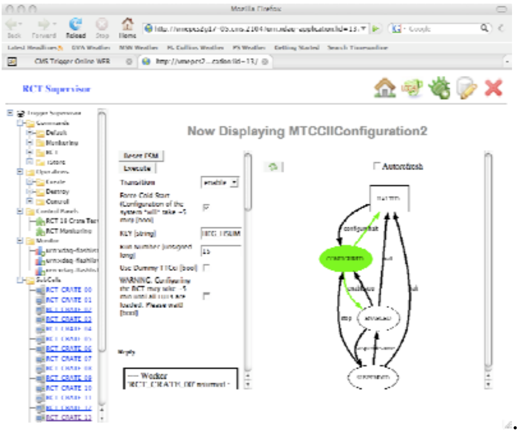

Figure 7: RCT Trigger Supervisor window for programming the RCT based on a pre-defined key (middle). The state machine is on the right.

The RCT Trigger Supervisor also monitors the system status (Figure 8). Link and clock error states are checked and can be masked if needed using database or flat file. Error history is stored in a database. Alerts and alarms are implemented in an expert mode for now, but a system to send alerts and alarms to CMS Run Control is currently in development.

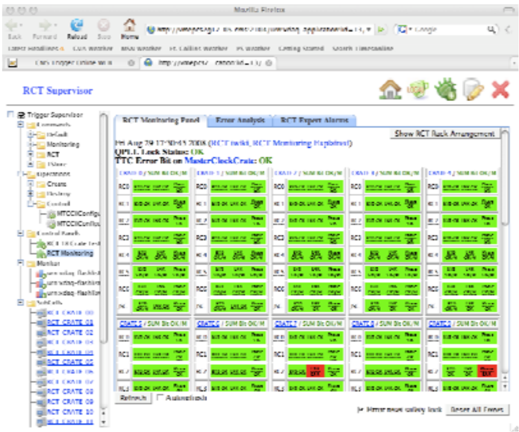

Figure 8: RCT Trigger Supervisor window for monitoring the RCT links and clock states. Problems appear highlighted in red, and are on a per-card basis. Holding the pointer over a specific error type provides information about which link is in error.

D. *RCT Intercrate Tests*

The RCT is able to cycle the addresses of its LUTs on the Receiver and Jet/Summary Cards to emulate up to 64 LHC bunch crossings. To debug the internal connections of the RCT all 18 crates are programmed and the GCT Source cards are used to capture the output.

A pattern is chosen, written to the LUTs, and the output is captured. This pattern is also fed to the Trigger Emulator (next section) and the output predicted is compared to the output captured and errors logged.

The bulk of the tests done so far have been internal, testing the timing of data sharing in and between the RCT crates. Patterns like walking zeros and ones, random, and simulated data were used. A number of small problems were found and fixed, and the timing was refined.

Currently this is a stand-alone program, but it will be integrated into the Trigger Supervisor. Expansion of the tests to use the pattern capability of the HTR and TCC boards to test the links is also underway.

V. Data Quality

A. *Trigger Emulator*

The trigger emulator is a software package designed to reproduce the hardware response of the trigger exactly. It replicates all of the on-board logic including all configurable options such as hardware registers and Look Up Tables (LUTs). It is used for hardware validation and monitoring, and is currently in use during calorimeter trigger commissioning.

The trigger emulator is very versatile and can either use real data or pattern files to predict output. The files used by the HCAL and ECAL can be used as input to their TPG pattern generators and files of data captured by the RCT, GCT, and GT as output can be compared directly. In this way errors are tracked down in the software, hardware, and firmware. In reverse, the validation of the algorithms can be done by injecting physics patterns into the hardware pattern generators and verifying the output. Additionally, the Look Up Tables (LUTs) are generated by the emulator using input from the HCAL and ECAL TPG emulators, saved to files, and written to the physical LUTs via the Trigger Supervisor.

B. *Global Runs and Data Taking*

In order to get the detectors, all electronics, and data acquisition systems ready for data taking, there have been a series of “Global Runs” with increasingly more of the CMS detector included. In order to not interfere with the ongoing commissioning of CMS, these were designated periods of a week to a few days. They started in the fall of 2007 and continue up to and after first beam in fall 2008.

Various subsystems participated in the early runs, depending on their commissioning status. The RCT was able to participate in most runs after the commissioning of the GCT e/γ source cards. The flexibility of the RCT LUTs enabled the RCT to send either the HCAL or ECAL TPGs to the RCT e/γ path, and these were triggered on at the Global Trigger level. Separate keys for the Trigger Supervisor were created for each LUT configuration. Data was studied offline and later checked online to validate algorithms and detect any problems (next section).

C. *RCT Data Quality Monitoring*

1) Online Data Quality Monitoring (DQM)

In order to monitor the RCT as data is taken, real-time histograms are created and filled in the CMS High-Level-Trigger filter farm during data taking at a rate of about 10 Hz. A small set of selected histograms allows the shift crews to see if any problems have arisen. These include data validity checks with the emulator and comparisons to reference histograms that are highlighted if in error. One can also retrieve older runs with the same tool. A screen shot is shown in Figure 9,

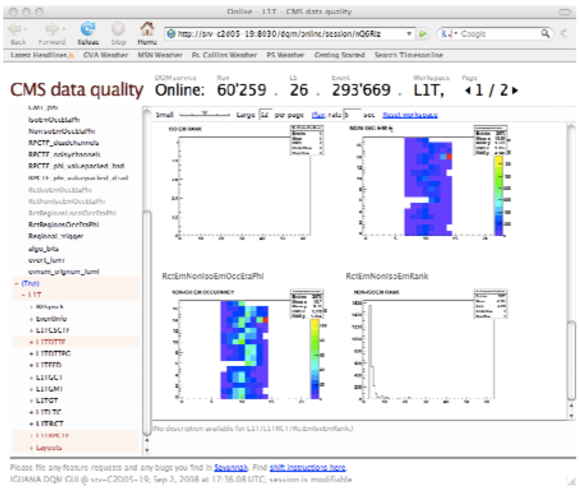

Figure 9: Online DQM browser window for a recent run. Calorimeter triggering was with the ECAL barrel. Two ECAL modules were out for the run and can be seen as white space in the two occupancy plots. Each RCT region is a single square.

2) *Offline DQM*

For more detailed analysis of the RCT performance, offline DQM is very valuable. Access to a greater number of events is possible, and more histograms and a data array are stored for more detailed analysis. DQM can be run on CMS online machines for a near real-time analysis.

The trigger emulator is fed the TPGs from the data and the RCT response is predicted, providing efficiencies at the RCT region level (Figure 10). Plots of energy distributions and additional one-dimensional plots are able to show subtle differences and problems with triggering thresholds (Figure 11 and 12). In this way problems can be traced back to the hardware that caused them.

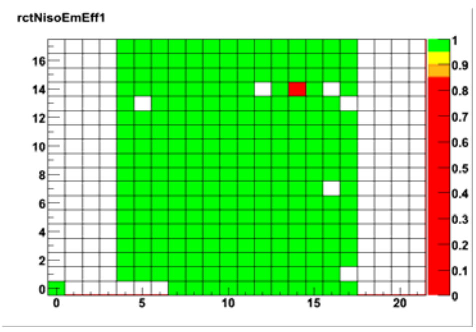

Figure 10: Non-isolated e/γ candidate efficiency for HCAL barrel as a function of eta index (horizontal, η=0 at 10 and 11 boundary) and phi index (vertical) of the RCT regions.

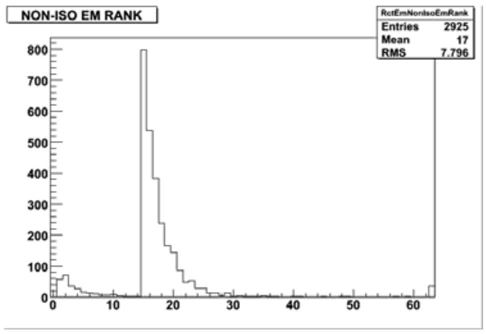

Figure 11: Non-isolated e/γ candidate rank (bits) as seen by the GCT. Threshold was at rank 15, and the rank from other triggers is seen below that.

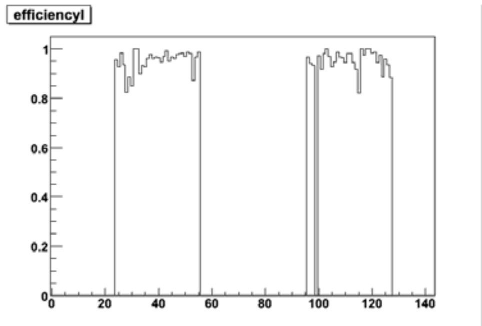

Figure 12: Non-isolated e/γ candidate efficiency plotted on a one-dimensional scale (each bin is an RCT region). Smaller drops can be seen more clearly. This was a very early run and only a small portion of HCAL was included in the calorimeter trigger.

VI. Future Operations and Plans

VII. Conclusions

The commissioning of the Regional Calorimeter Trigger at CMS is complete. A suite of tools for operation and monitoring the RCT has been developed and is mature. With DCS, internal testing, basic operation and configuration with the Trigger Supervisor, and analysis of the incoming data with the Trigger Emulator and DQM, this toolbox is essential for the RCT and its operators.

VIII. References

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[3] CMS, The TRIDAS Project Technical Design Report, Volume 1: The Trigger Systems, CERN/LHCC 2000-38, CMS TDR 6.1.

[4] W. Smith et al., CMS Regional Calorimeter Trigger High Speed ASICs, *Proceedings of the Sixth Workshop on Electronics for LHC Experiments*, Krakow, Poland, September 2000, CERN-2000-010.

[5] http://ttc.web.cern.ch/TTC/intro.html http://cmsdoc.cern.ch/cms/TRIDAS/ttc/modules/ttc.html

[6] http://www.pvss.com

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