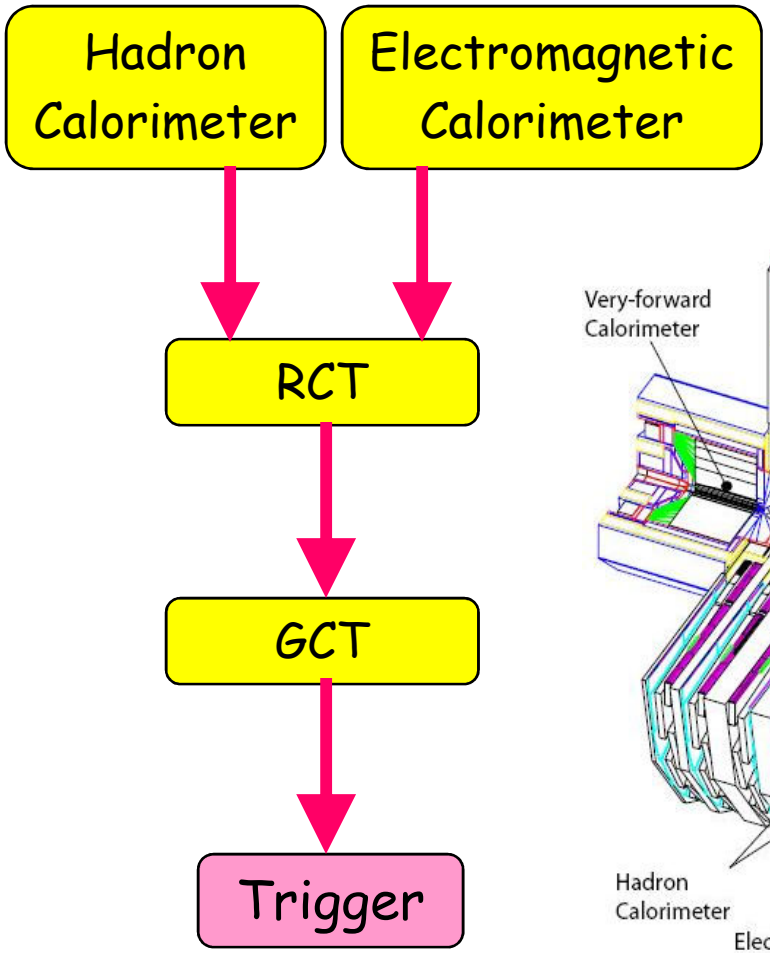
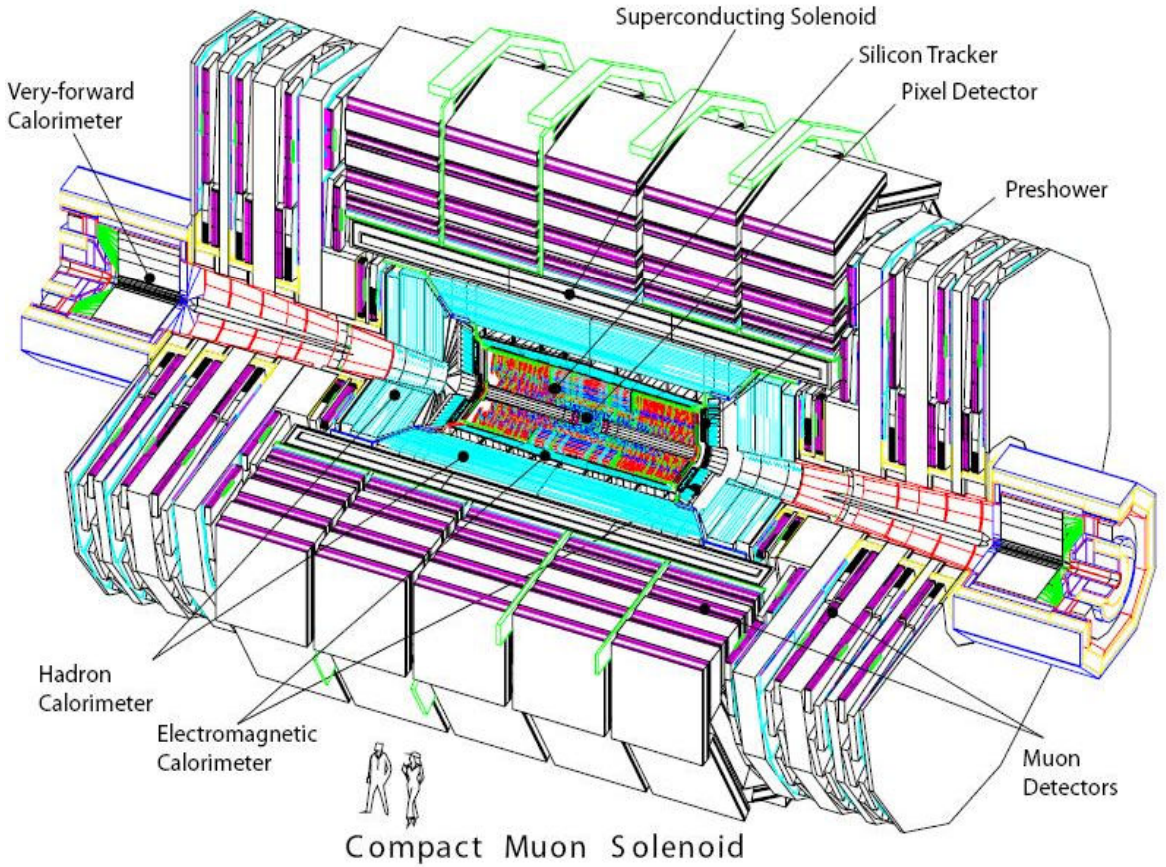
Trigger R&D for CMS at SLHC: Part 1

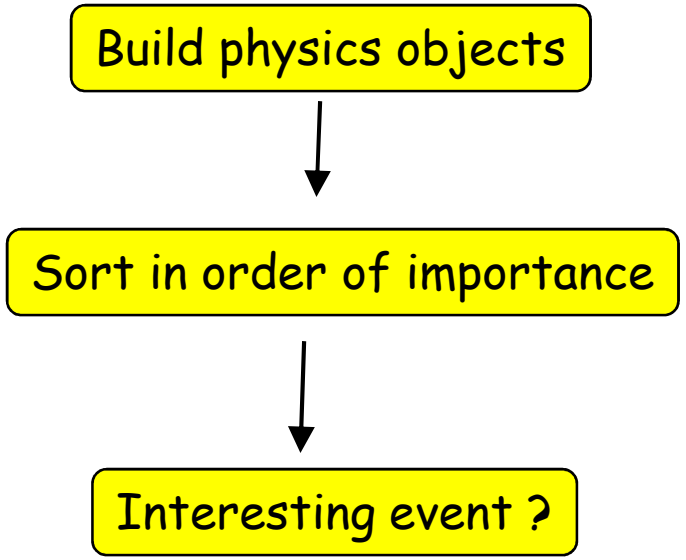
An evolving trigger architecture...


Hadron Calorimeter
Electromagnetic Calorimeter
RCT
GCT
Trigger


Superconducting Solenoid
Silicon Tracker
Pixel Detector
Very-forward Calorimeter
Preshower
Hadron Calorimeter
Electromagnetic Calorimeter
Muon Detectors
Compact Muon Solenoid

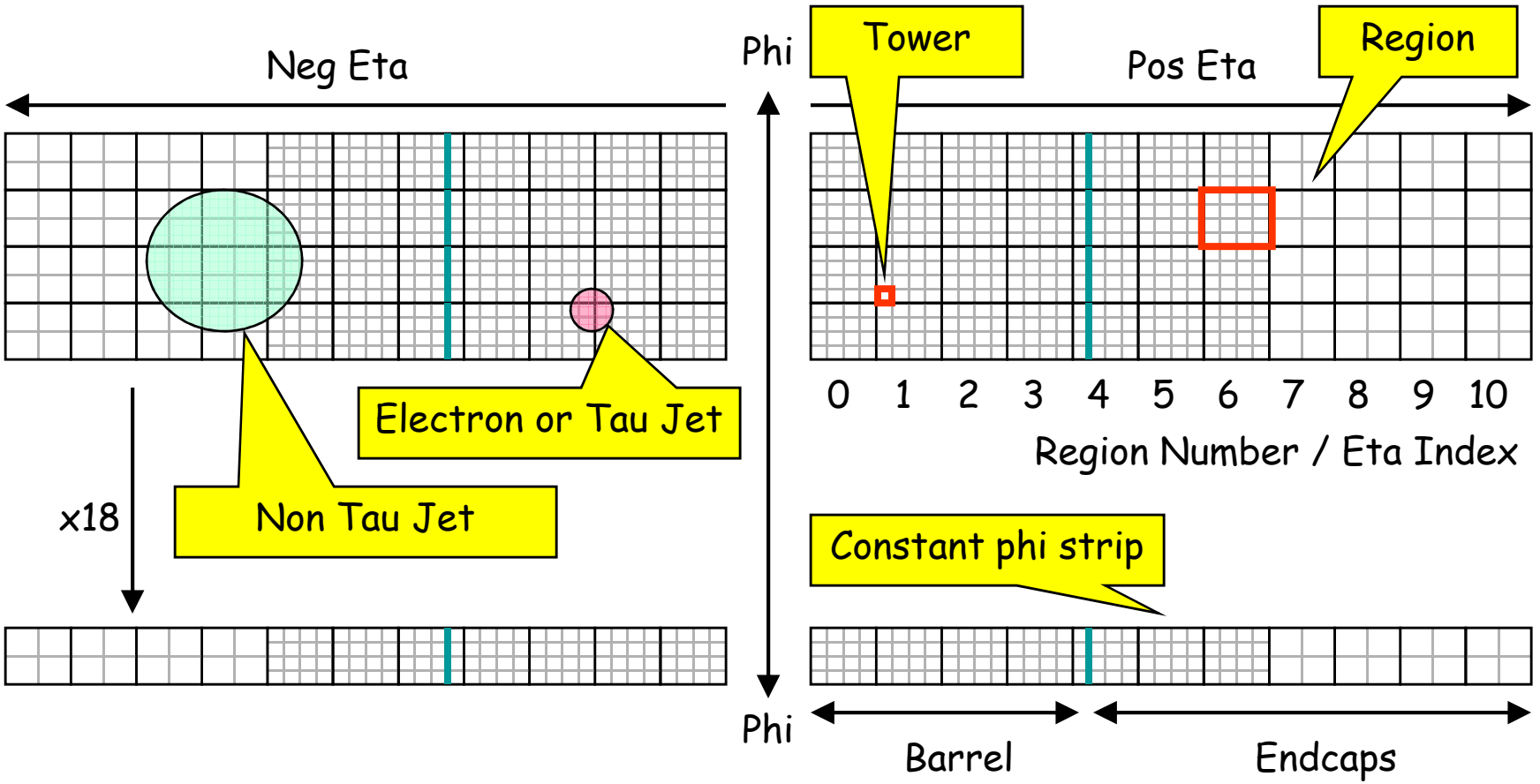
Trigger Requirements

- Task
  - Build physics objects
    - cluster electrons, taus, jets
    - calculate quantities such as total-et
  - Sort in order of rank
  - Identify physics topologies
    - Must not miss interesting events
    - Can be crude: just a trigger!
  - Latency must be short



- Questions
  - How best to map task onto physical geometry?
  - What type of hardware architecture
  - What services required?

Geometry of RCT

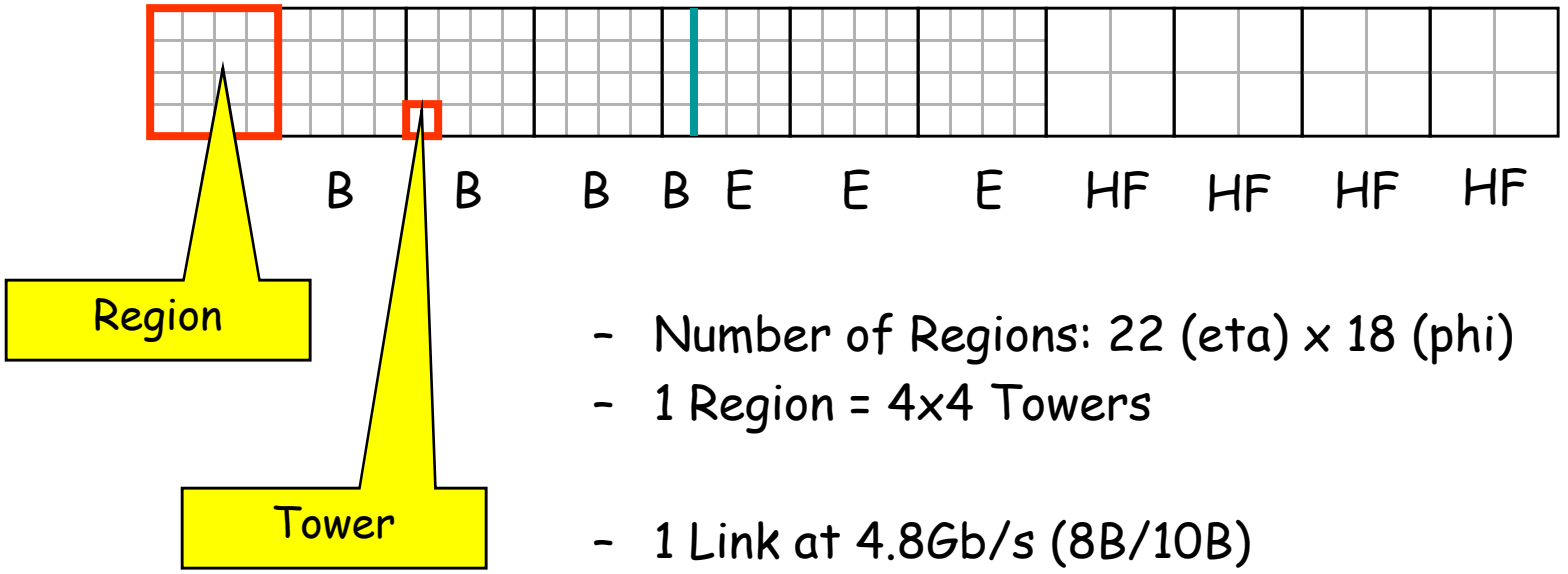


Data per tower, per bx

ECAL: 8bits energy + FGV (FineGrainVeto)

HCAL: 8bits energy + MIP (MinIonisingParticle)

Geometry & link capacity



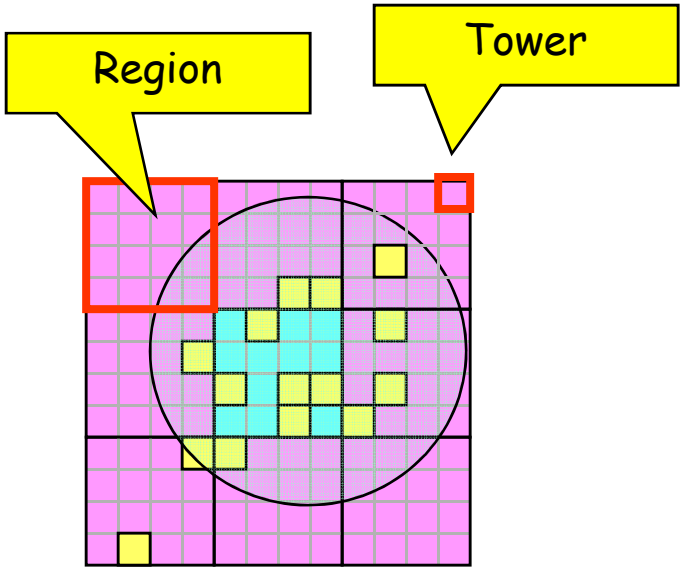
- Number of Regions: 22 (eta) x 18 (phi)
- 1 Region = 4x4 Towers

- 1 Link at 4.8Gb/s (8B/10B)
  - 12bytes per bx
  - Hence 1 region = 2 links (12bits)

- 4 links per region for both ECAL & HCAL data.

Plan A: Original Plan

- Apply all jet + electron clustering in single FPGA
- To contain jet centred on middle region requires 3x3 regions
  - i.e. 36 links at 5Gb/s
- 14x18 regions (excluding HF)
  - More than 252 cards

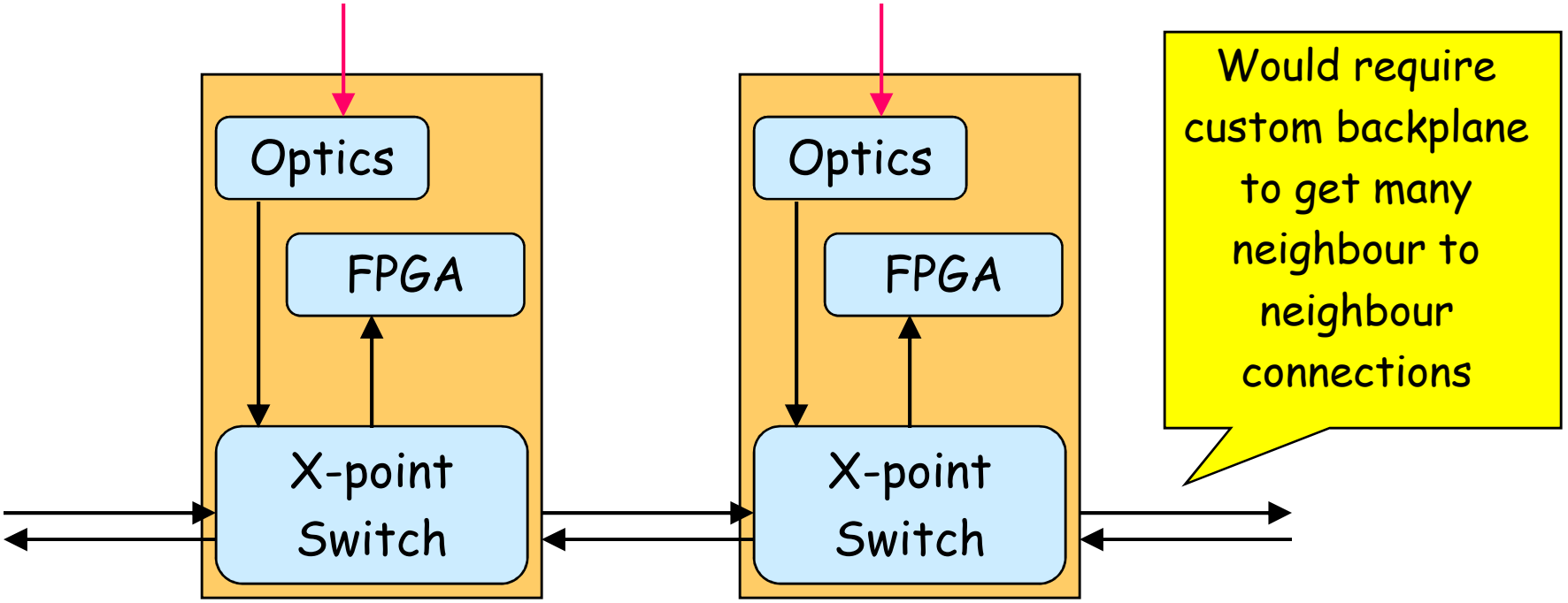


How best to achieve such large duplication of data ?

Technology

- Use large protocol agnostic crosspoint switches (~100x100) to duplicate data and route it to where required

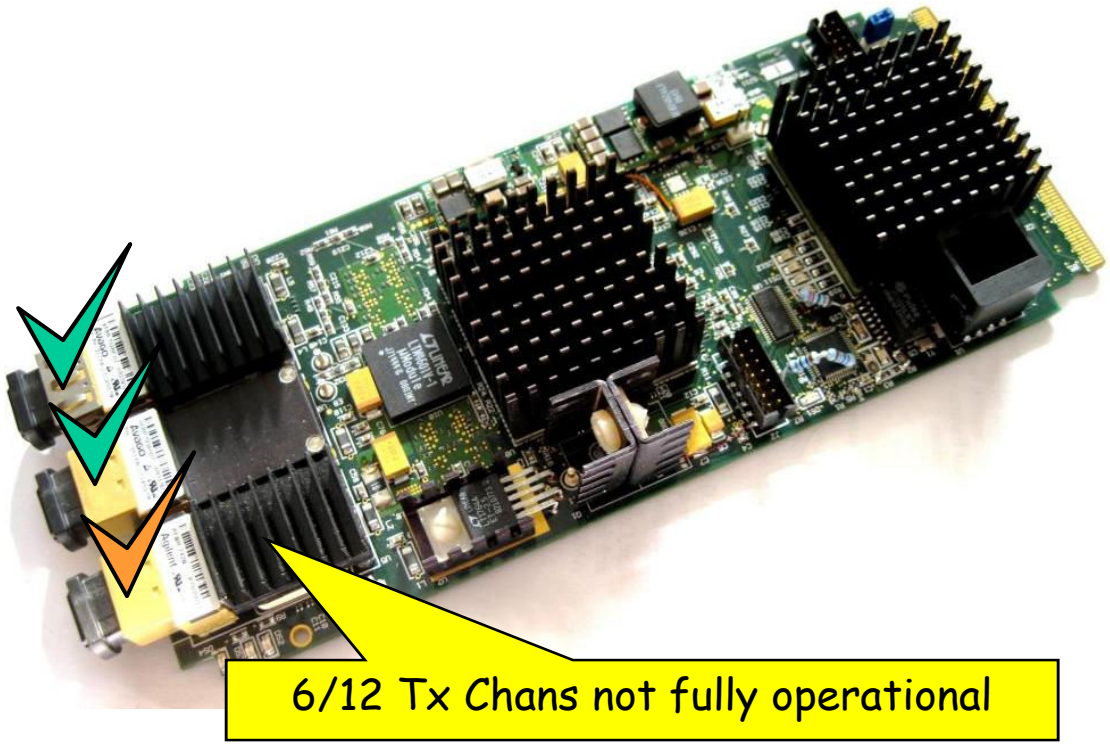
- uTCA crate provides high density serial interconnect
  - Based on AMC cards (daughter cards used in ATCA)
  - 20 serdes links + ethernet
  - Compact form factor ideal for serdes links

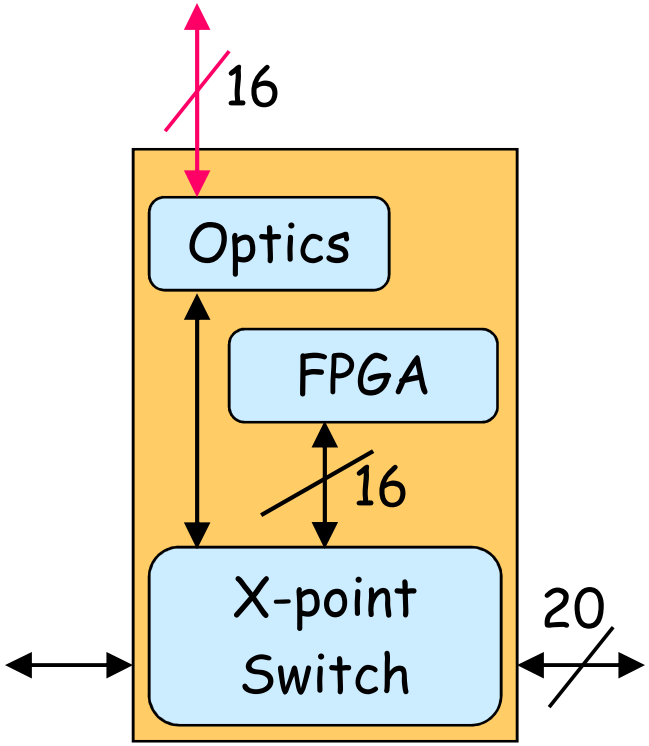


Matrix card

- Developed as part of the GCT project
  - Design was conceived by Matt Stettler from LANL

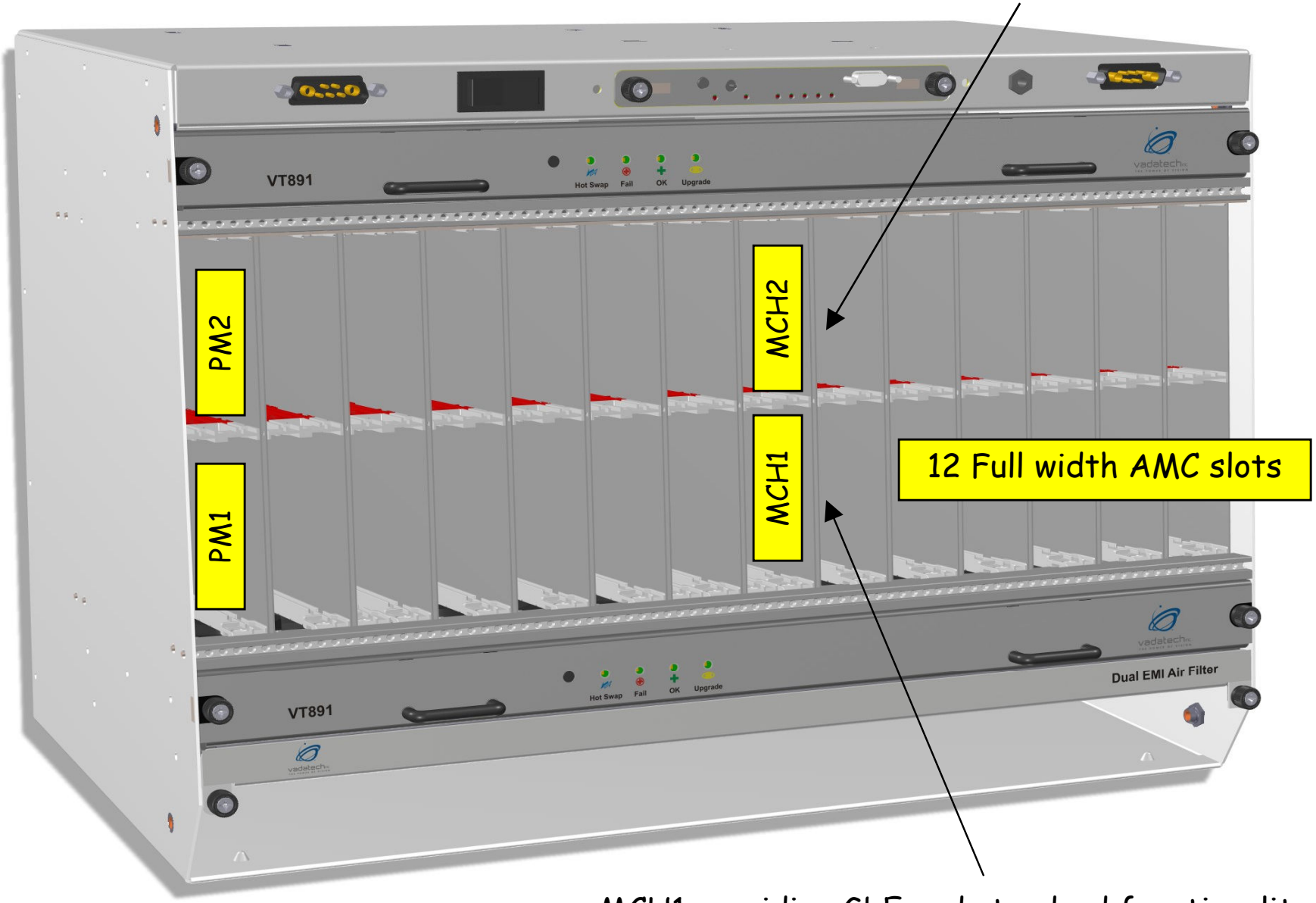
- John Jones will describe it in more detail in a following talk that will describe "Plan C"





Vadatech VT891

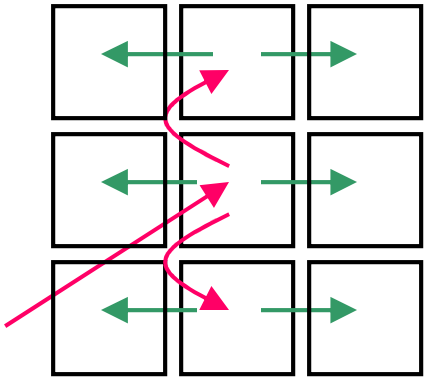
MCH2: LHC-CLK, TTC & TTS and DAQ Concentrator



MCH1 providing GbE and standard functionality

Plan A: Issues

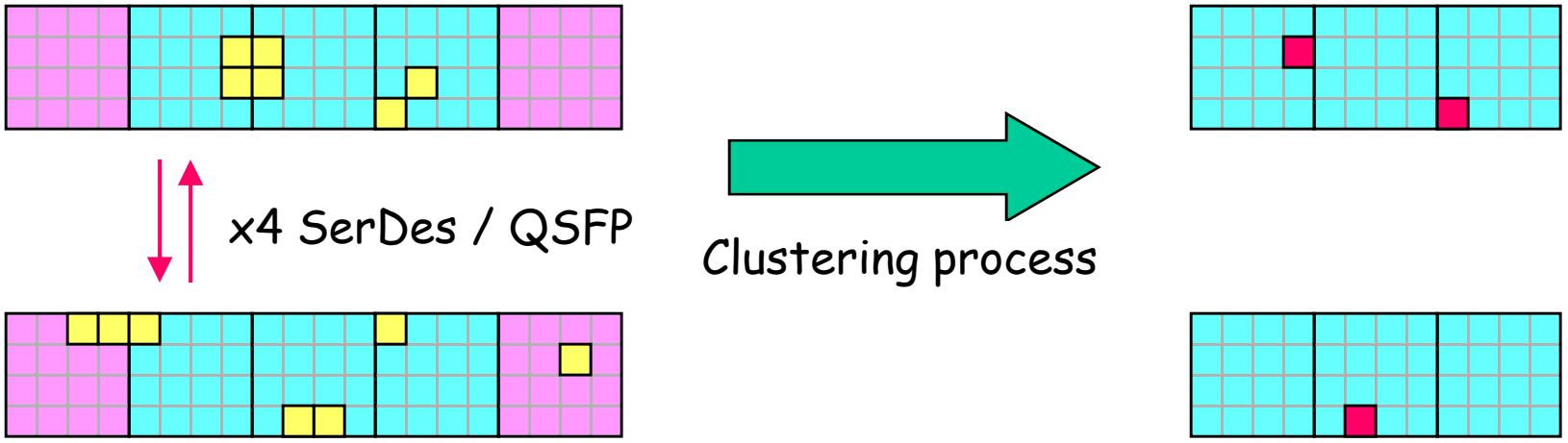
- Matrix card very novel concept, but doesn't have enough links to realise the original vision....



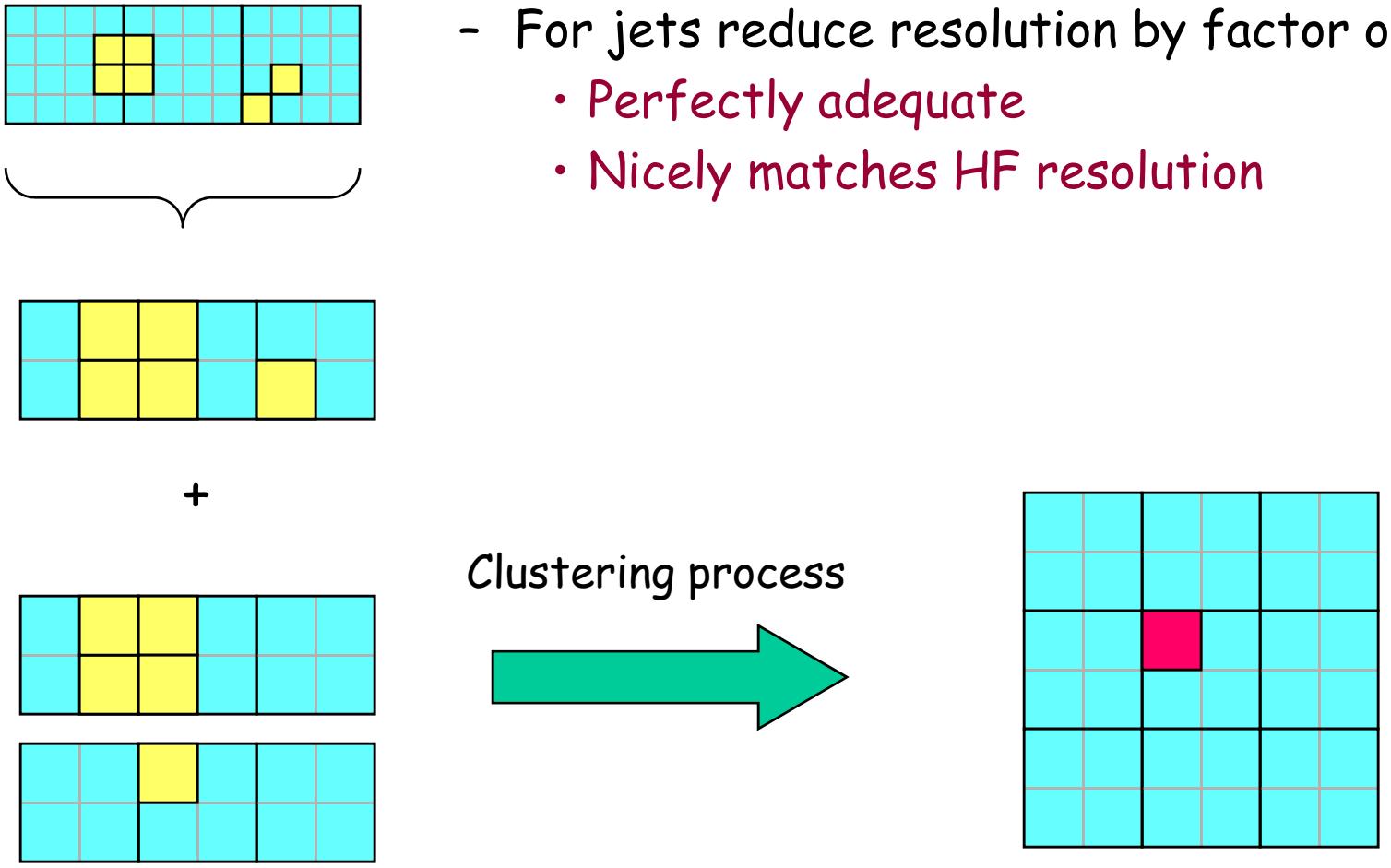
- Original plan does have some drawbacks...
  - Large system of > 252 identical cards
  - Requires 2 stage sort with resulting latency penalty
  - Very inefficient
  - Serdes signal making too many hops without regeneration
  - 20 serdes links on backplane insufficient

Plan B: Fine Processing

- Concentrate on electron and tau jet processing initially
  - Small area – typically < 2x2 towers
- Allow capability to explore different algorithms
  - Could use existing algorithms
    - "Calorimeter Trigger for Phase I", M.Bachtis et al., Wisconsin
  - or Pre-cluster method used in GCT



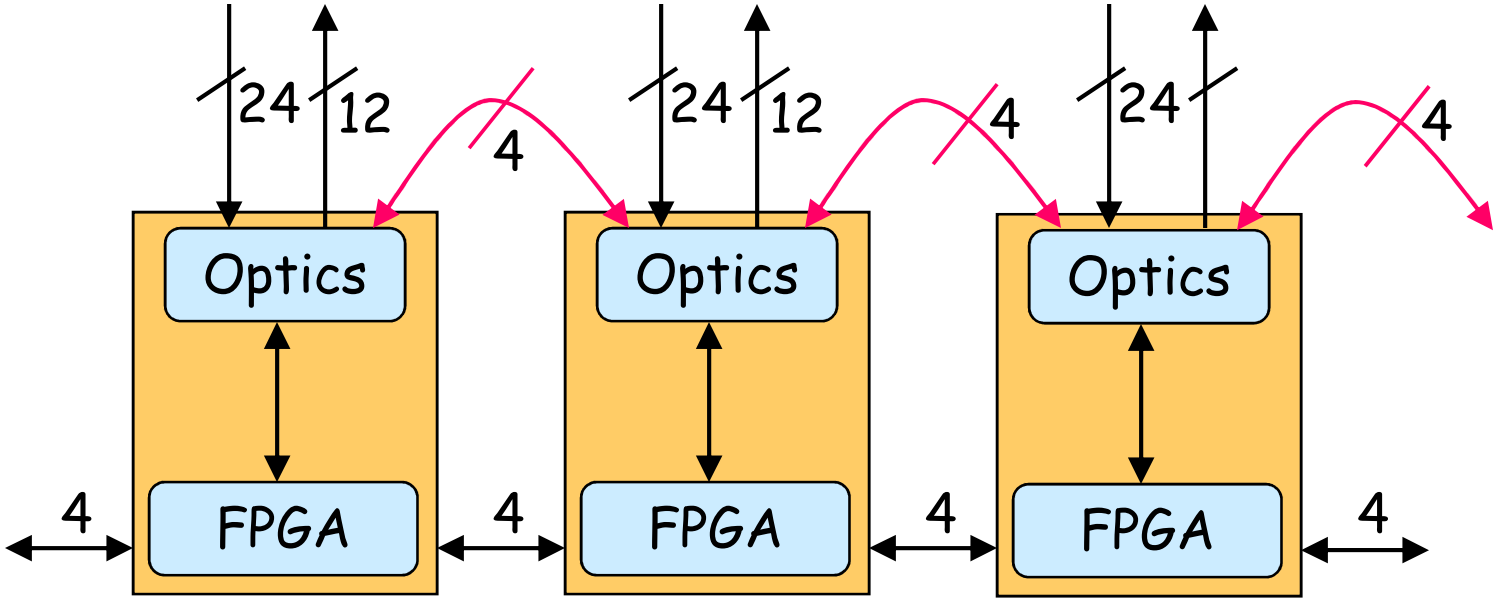
Plan B: Coarse Processing

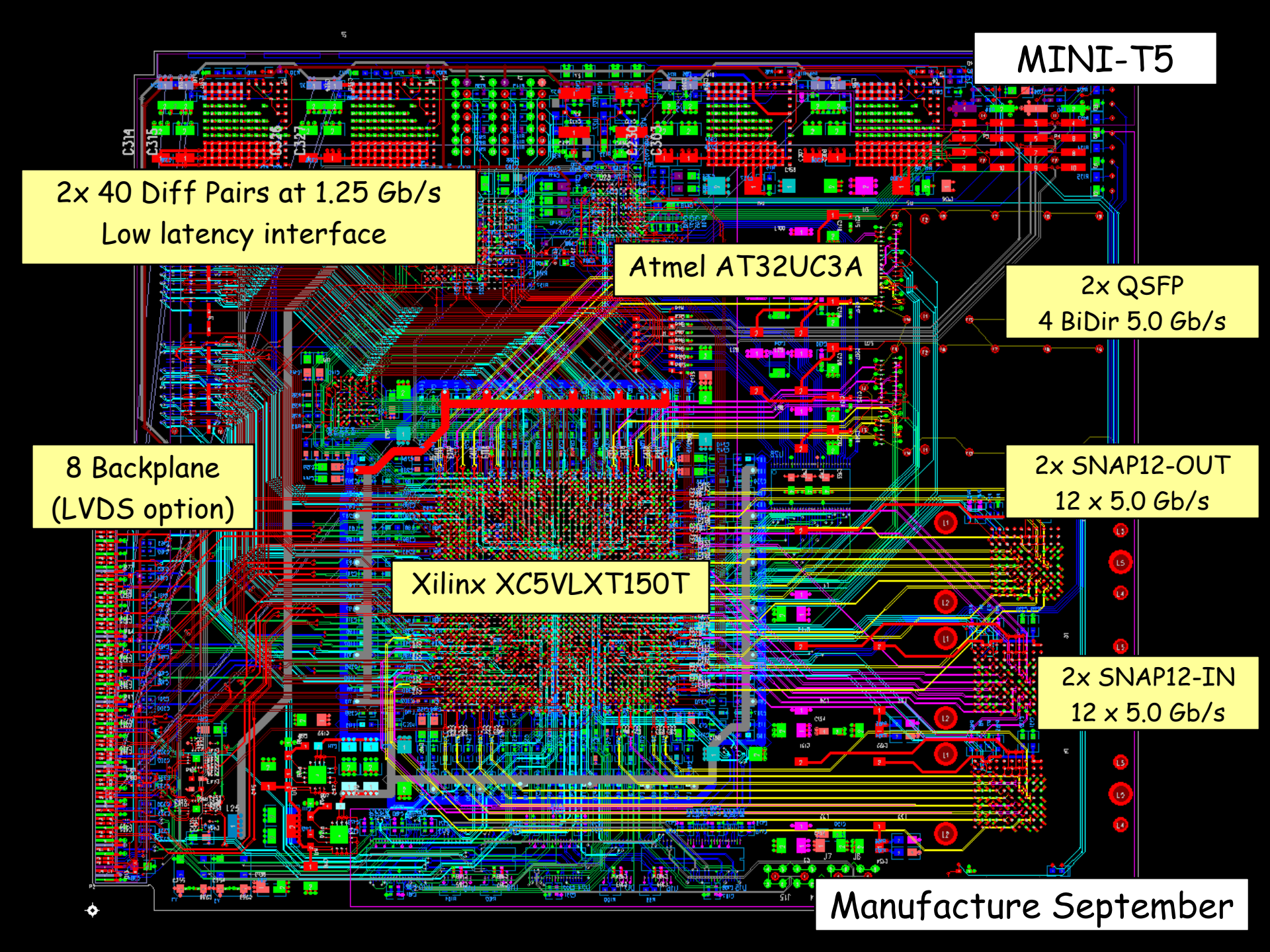


- For jets reduce resolution by factor of 2
  - Perfectly adequate
  - Nicely matches HF resolution

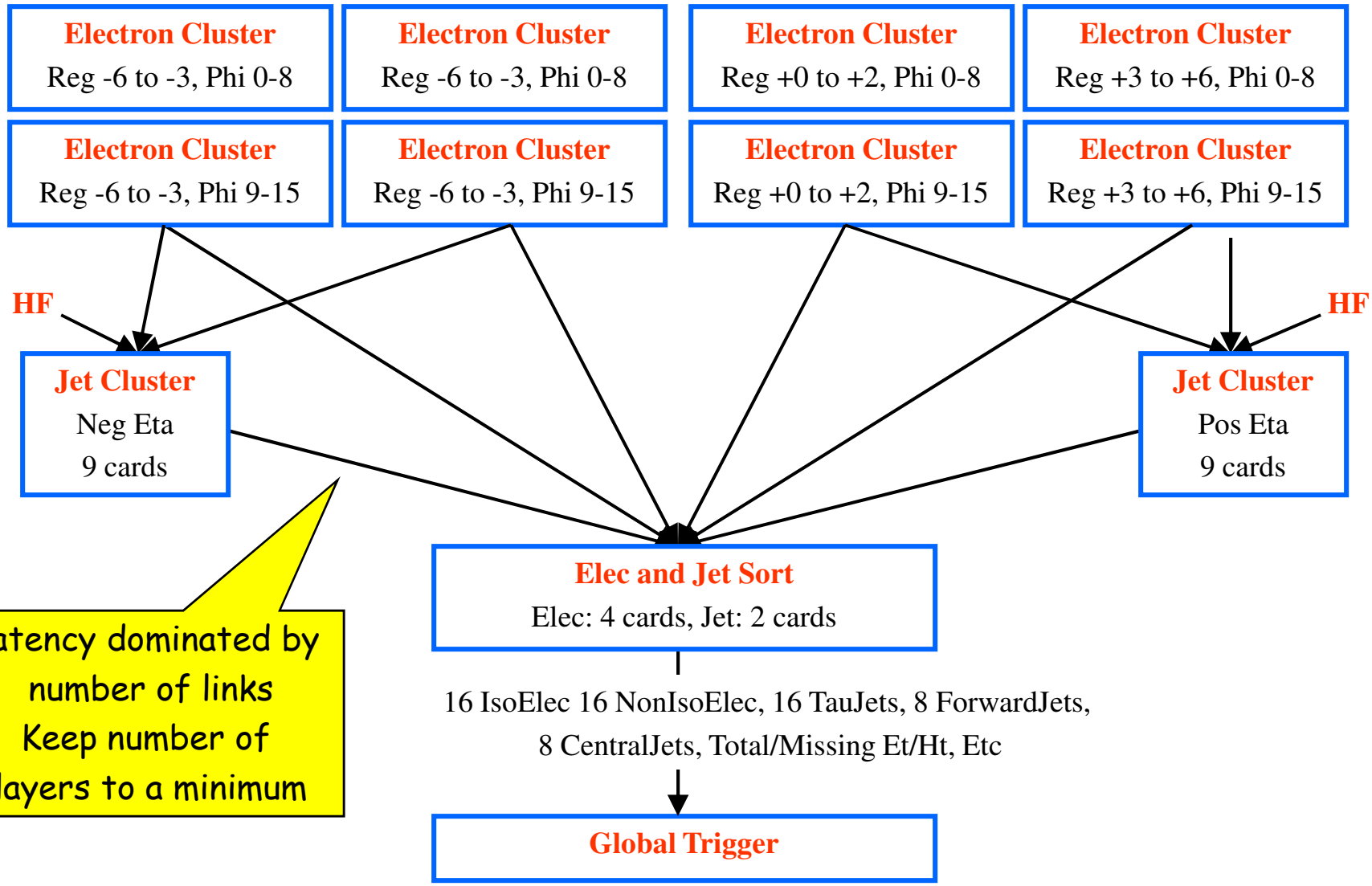
Plan B Card

- No need for a custom backplane,
  - although one could be used to either provide additional bandwidth or to reduce optical components.
- Only uses ~100 cards => single stage sort
- Substantially simpler to connect
  - Single QSFP cable between cards. Can span crates
- The compromise is a a less flexible algorithm
  - i.e. electron/jet processing separated



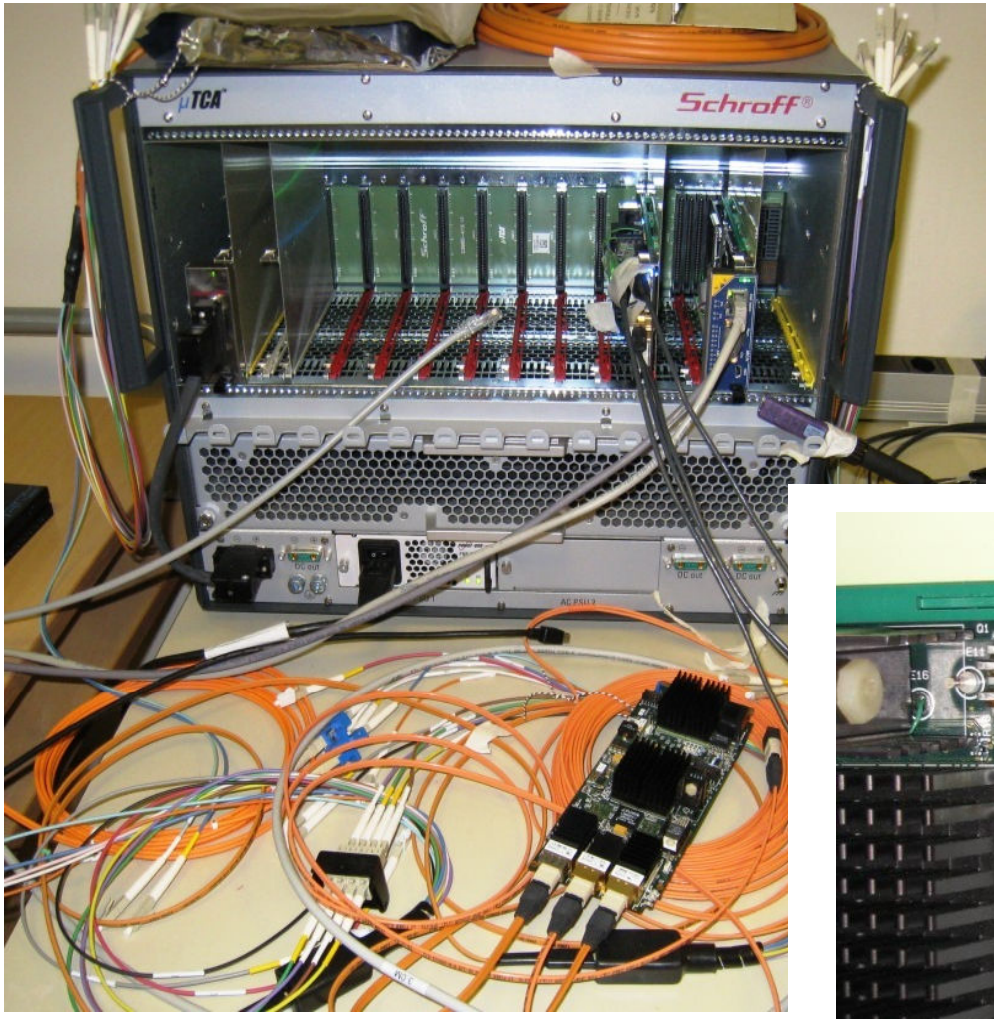

MINI-T5
2x 40 Diff Pairs at 1.25 Gb/s
Low latency interface
Atmel AT32UC3A
2x QSFP
4 BiDir 5.0 Gb/s
8 Backplane
(LVDS option)
2x SNAP12-OUT
12 x 5.0 Gb/s
Xilinx XC5VLXT150T
2x SNAP12-IN
12 x 5.0 Gb/s
Manufacture September

Plan B: System view (uTCA crates)



Trigger R&D for CMS at SLHC: Part 2

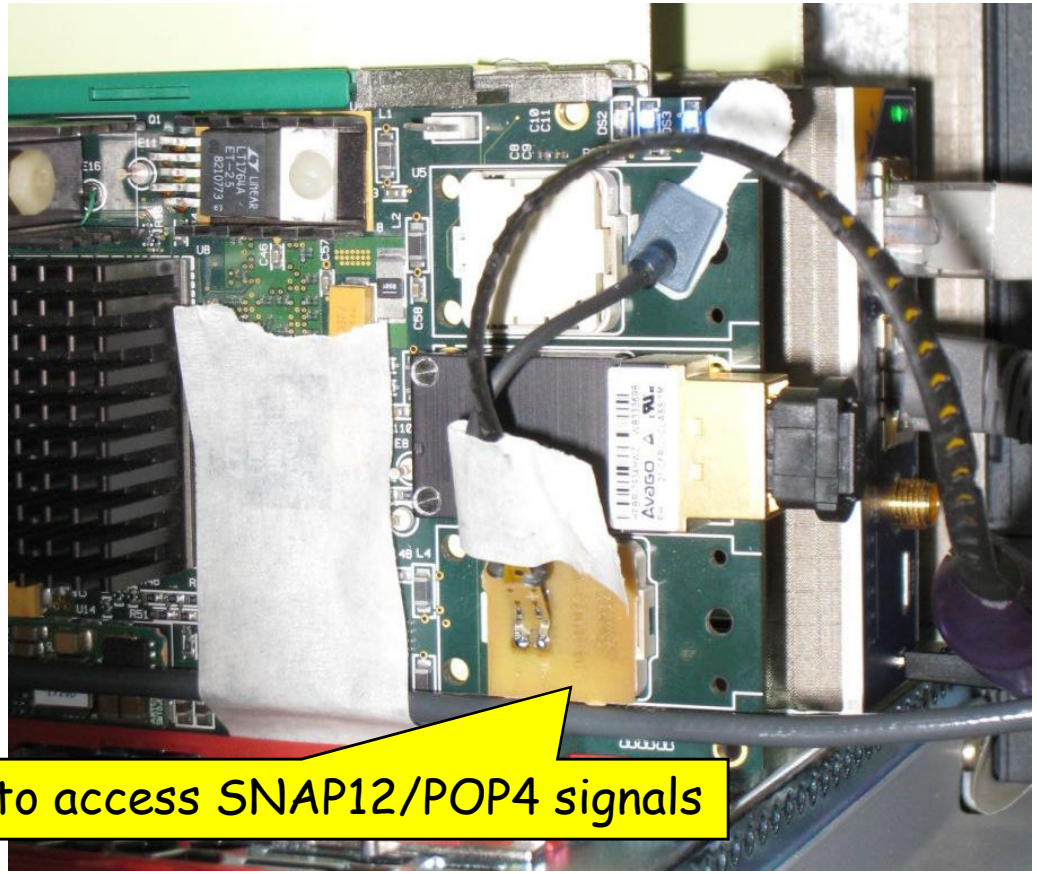
Analysis of failing high speed serial links on the Matrix Card



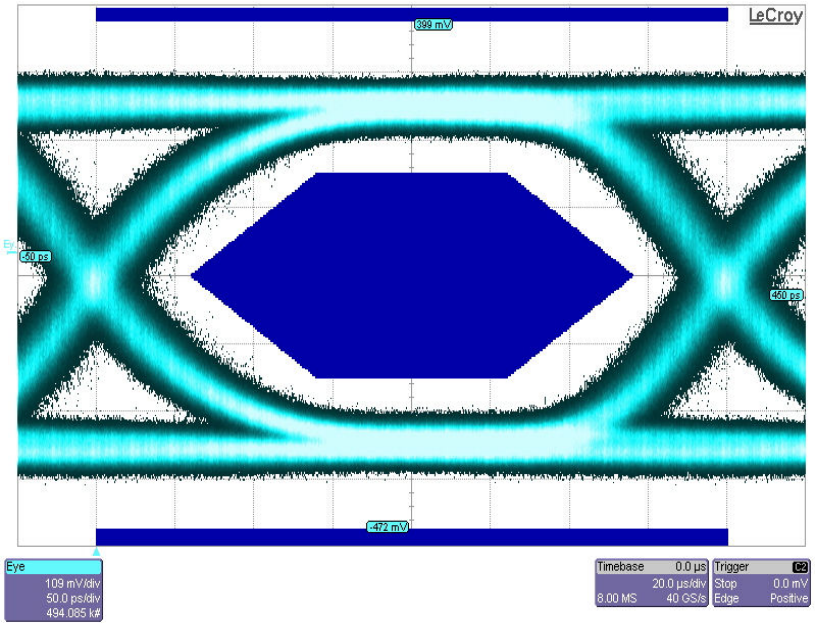
- Hard to debug

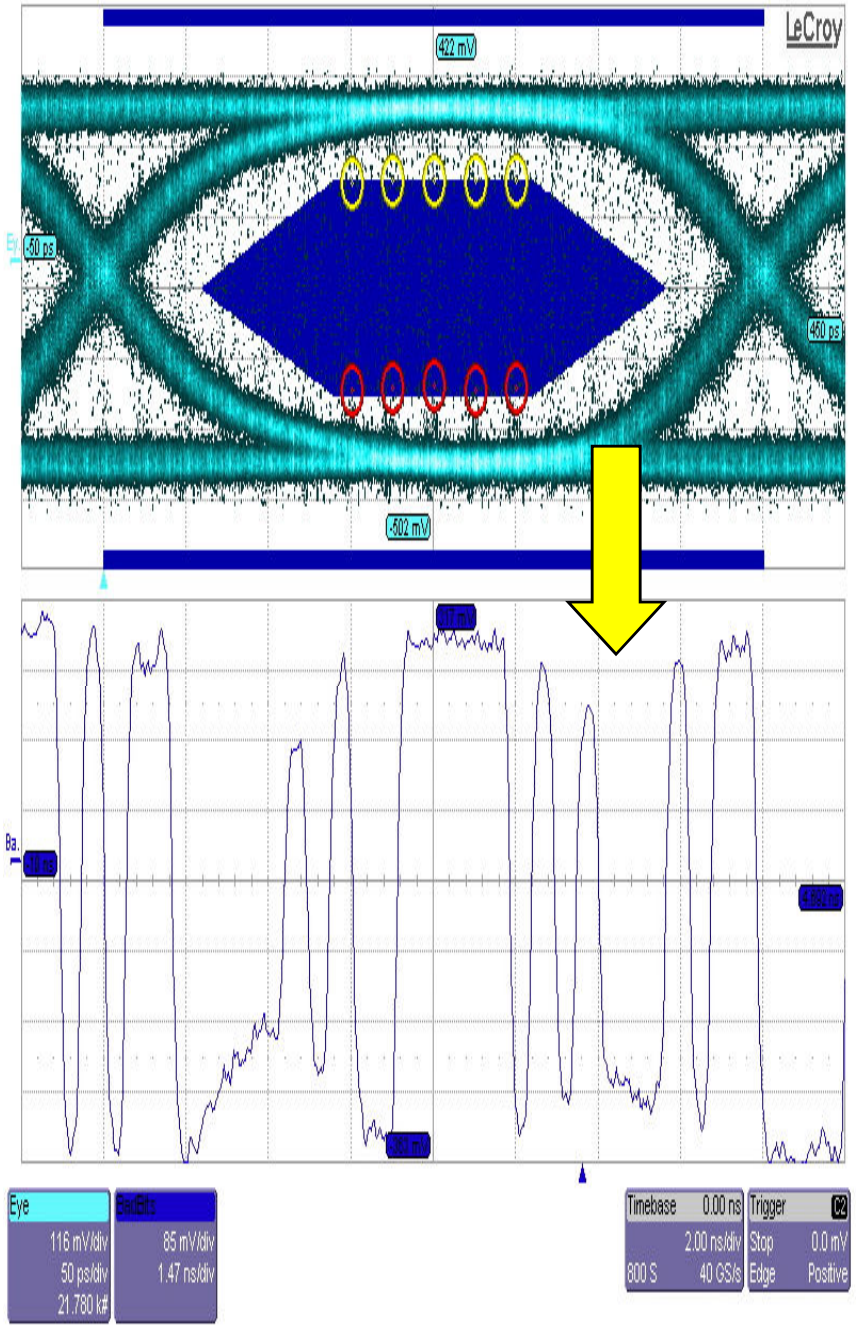
  => Lot of conjecture.

- Initial hypothesis completely wrong in all cases



Test board to access SNAP12/POP4 signals

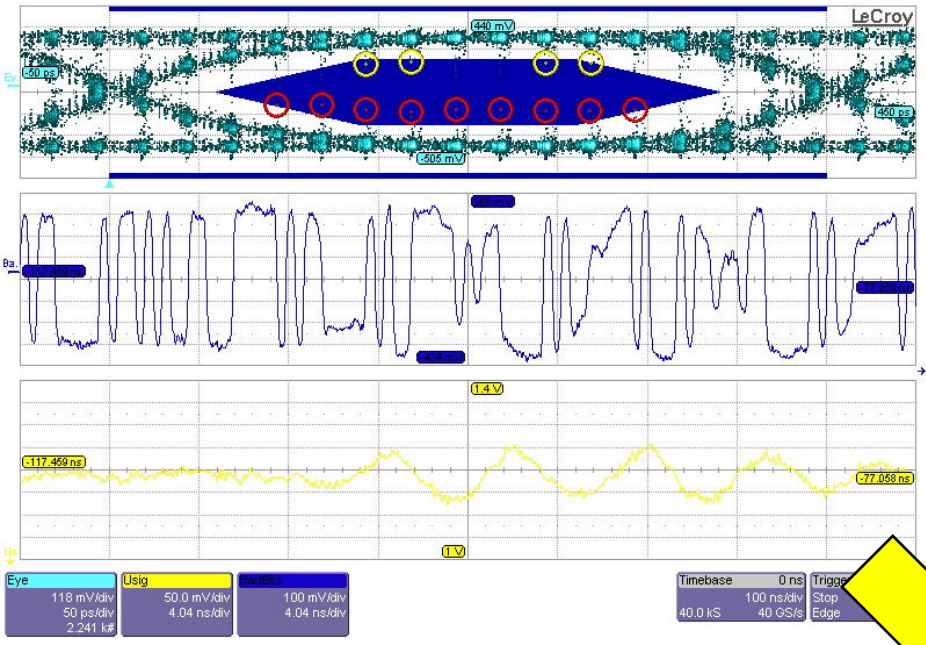


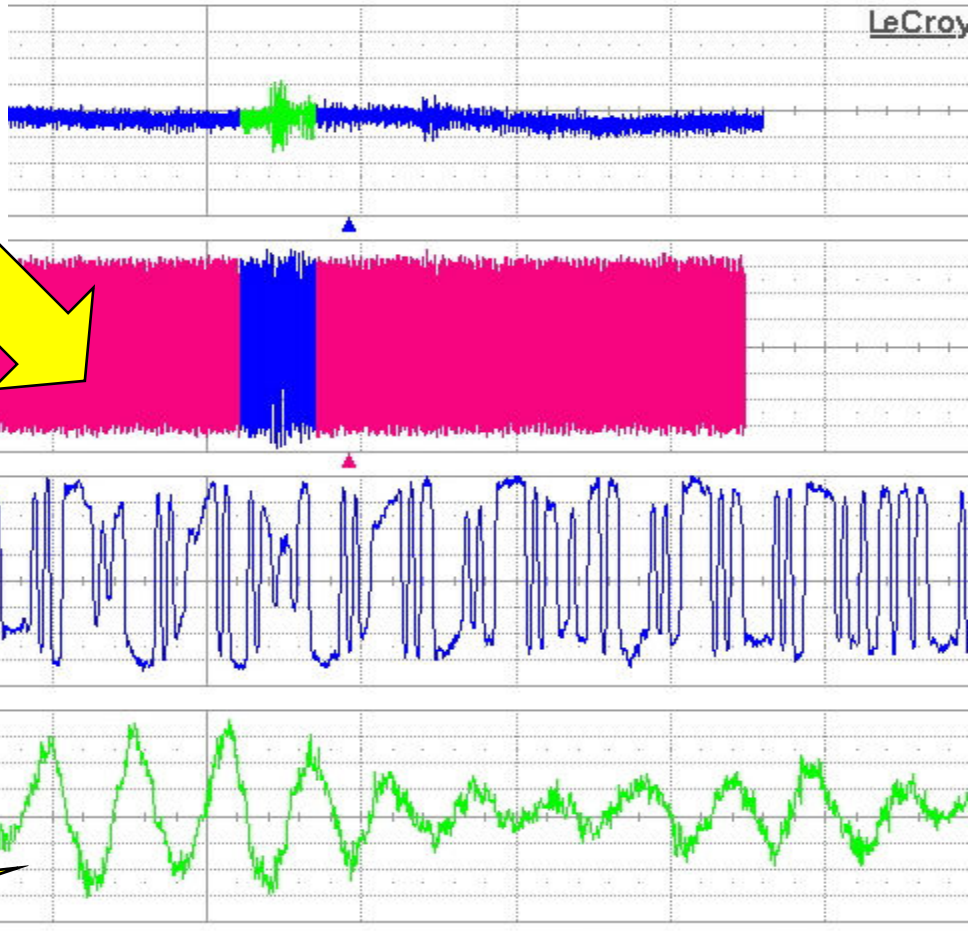


Link running at 2.5Gb/s

- Infiniband Tx mask
- Assumed CDR PLL has cut-off at ~ 1000 bit periods (2.5MHz)
- Fits perfect theoretical clk to data, then extracts "eye"
- Can correlate mask failure with position on data stream
- Only possible on real time scope...

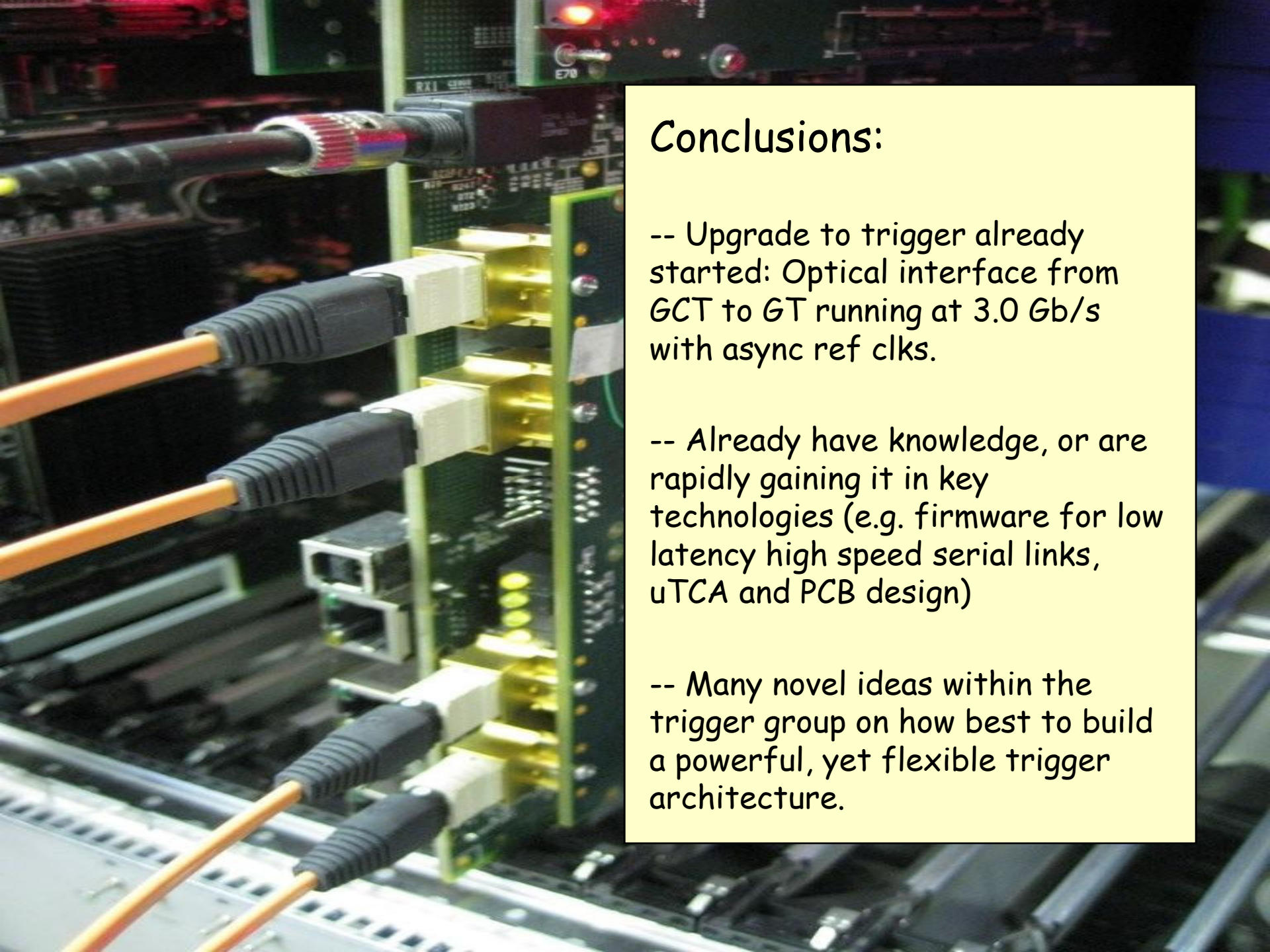
Scope can store second channel while in SDA (Serial Data Analysis Mode)
Allows correlation between SDA events and other signals on the PCB





- *At 200MHz Interplane impedance is ~0.4 Ohm*
  - *Simple parallel plate model*
- *At 200 MHz capacitors behaving like inductors*
  - *Impedance > 1 ohm*

~ 200MHz noise, 100mV pk to pk



Conclusions:

-- Upgrade to trigger already started: Optical interface from GCT to GT running at 3.0 Gb/s with async ref clks.

-- Already have knowledge, or are rapidly gaining it in key technologies (e.g. firmware for low latency high speed serial links, uTCA and PCB design)

-- Many novel ideas within the trigger group on how best to build a powerful, yet flexible trigger architecture.