Scalable Readout System SRS

"from test systems to very large LHC systems"

= proposal for RD51, WG 5 =

(updated version after comments)

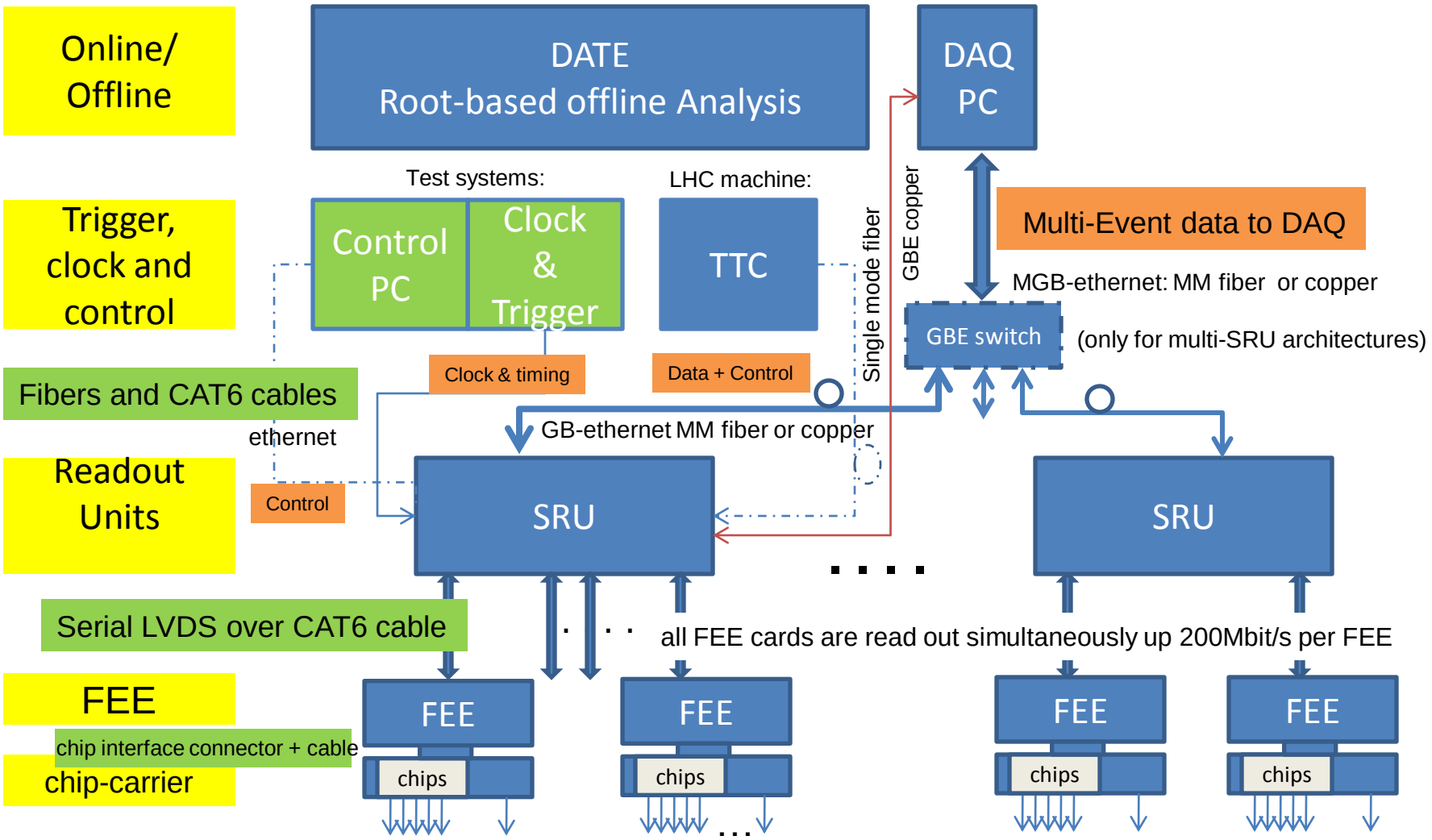
based on existing concepts:

Data and Trigger streams via GBE (LHCb)
DATE readout software (ALICE DAQ)
DCS: networked Linux mezzanine card with TTC chip (ALICE/ KIP Heidelberg)
HV bias control for photo-diodes (ALICE PHOS)
High bandwidth LVDS data transfer via Network cables (ALICE EMCal)
LCU board (ALICE EMCal, under design)

Motivation

- Common system for: gas- solid state- photon- detectors
- Scalable from minimal test system to large readout system
- User friendly and robust DAQ software: DATE
- Offline data analysis and presentation: Root of CERN
- Scalable Data link: Gigabit Ethernet via copper or fiber
- Link archicture (instead of bus)
- TTC option for LHC clock and trigger distribution
- based on only 2 custom hardware elements: FEE and SRU
- frontend interface on FEE to application dependent readout ASICS

Scalable concept in a nutshell



People, Teams*

- Dr. H. Muller, CERN PH: scalable RO proposal , coordination and documentation
- Dr. W. Riegler, CERN PH: RD51 convenor WG on Electronics & Readout systems
- Dr. H. Hillemanns, CERN DG/KTT Technology Transfer officer: legal and WEB
- Dr. J. Wotschak, CERN PH, for ATLAS MMega project: User: as upgrade to current test-systems based on FEE +Altro frontend
- Dr. P. van de Vyvre, CERN PH, ALICE DAQ: Gigabit ethernet port for DATE
- Dr. Jose Toledo , Univ. o. Valencia: applications for medicine and Neutrino experiments

  + Alfonso Tarazona , Univ. o Valencia, NEXT project: Gigabit Ethernet implementation
- Rui Pimenta, Satellite services: Cadence design SRU
- Dr. Alex Walsch, GE Global Research, Garching Munich: industrial research application (ad interim observer)
- Dr. Yaping Wang, CCNU Wuhan: Offline Root analysis

  + Dong Wang CCNU Wuhan: Firmware Board Controllers

  + N.N . CCNU Wuhan: DATE compatible Data formats and protocols

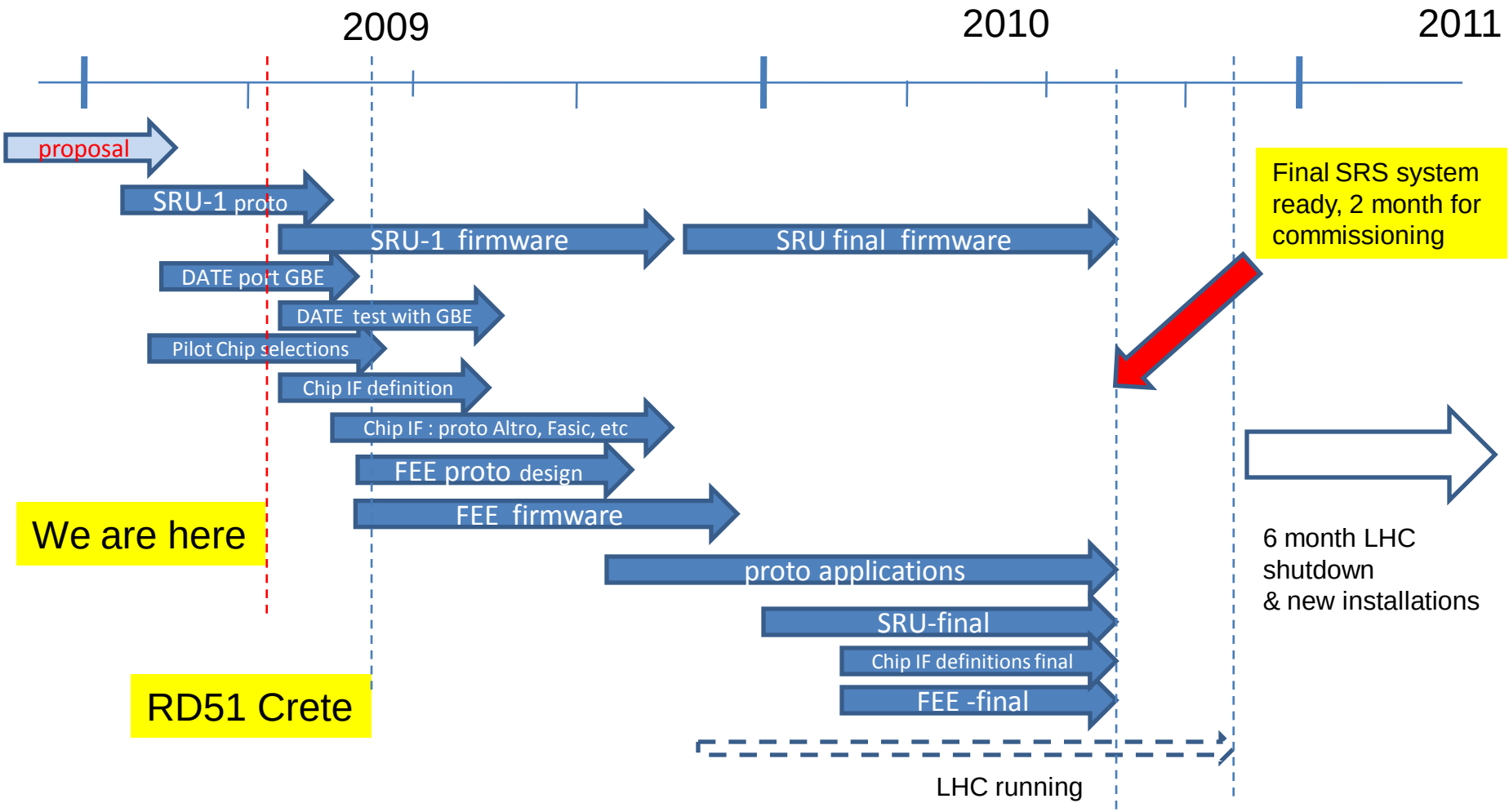
  ----------t.b.d----------
- NN FEE Chip Interfaces: decoding, data compression algorithms, formatting & buffering*

confirmed

request

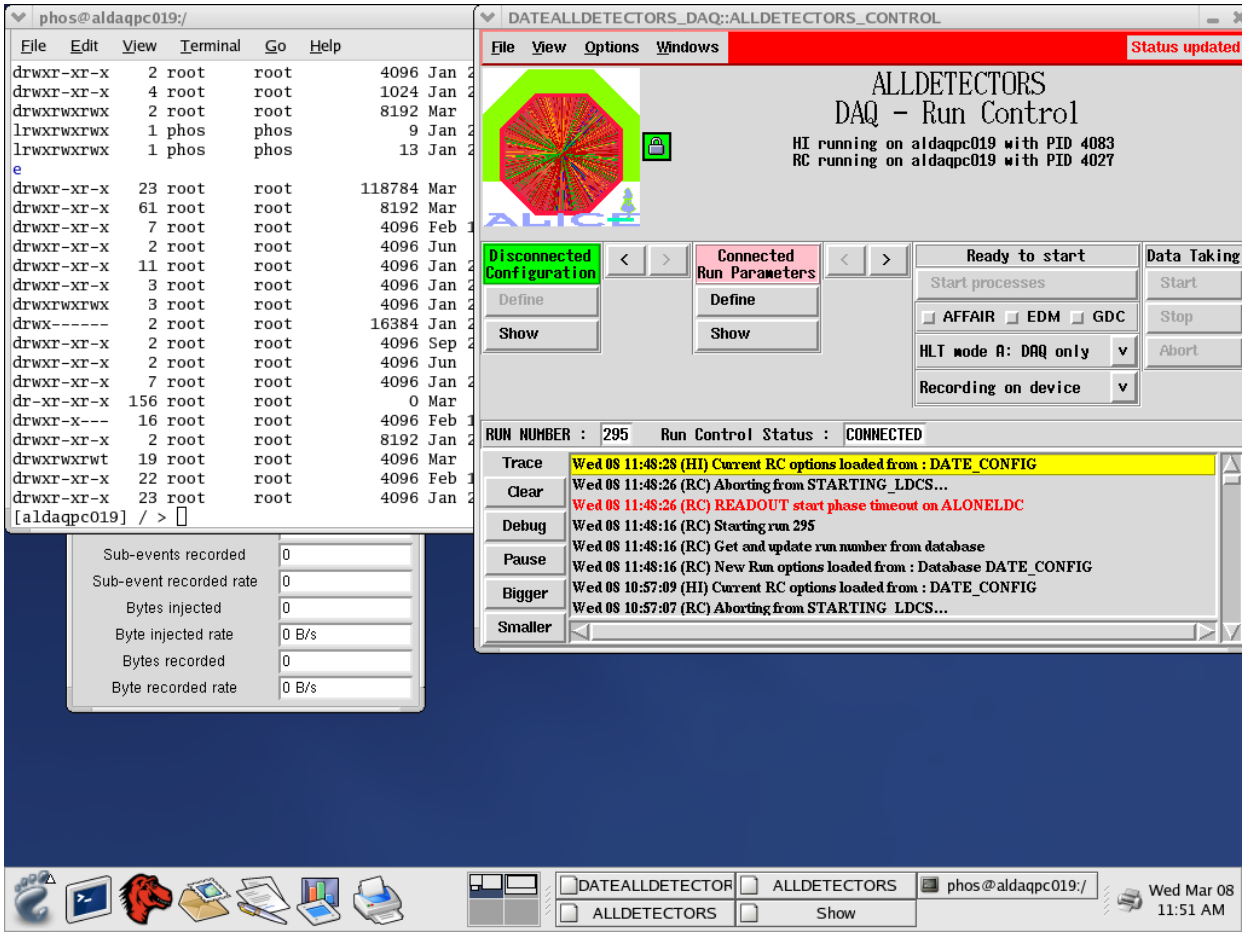
* Fellow requested via RD51

Project Timing SRS



DATE Data Acquisition software

http://ph-dep-aid.web.cern.ch/ph-dep-aid/



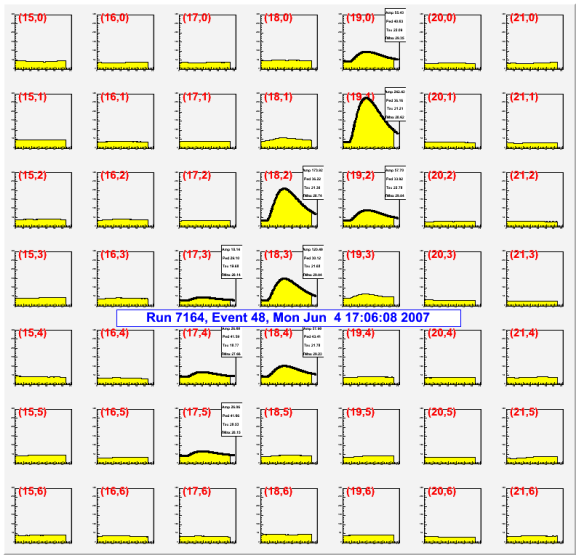
- Linux-based
- baseline for all ALICE detectors
- also used by other users
- easy User interface
- very well documented
- in use both for test-systems and full ALICE detector system
- Root file storage
- I/O interface to MM fiber
- porting to GBE over MM fiber has started

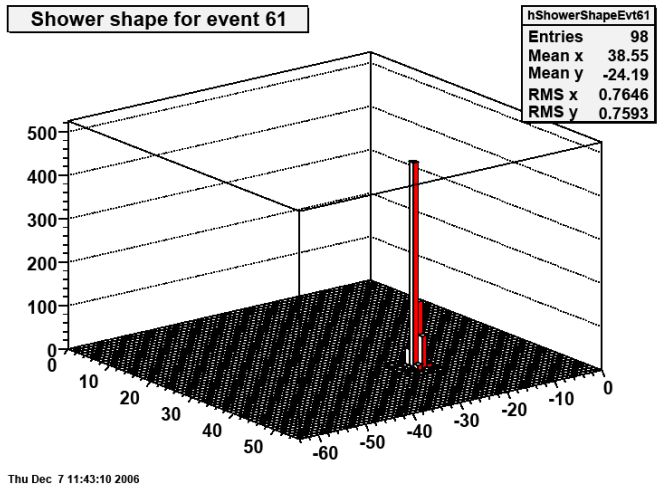
Root Data Analysis

http://root.cern.ch/

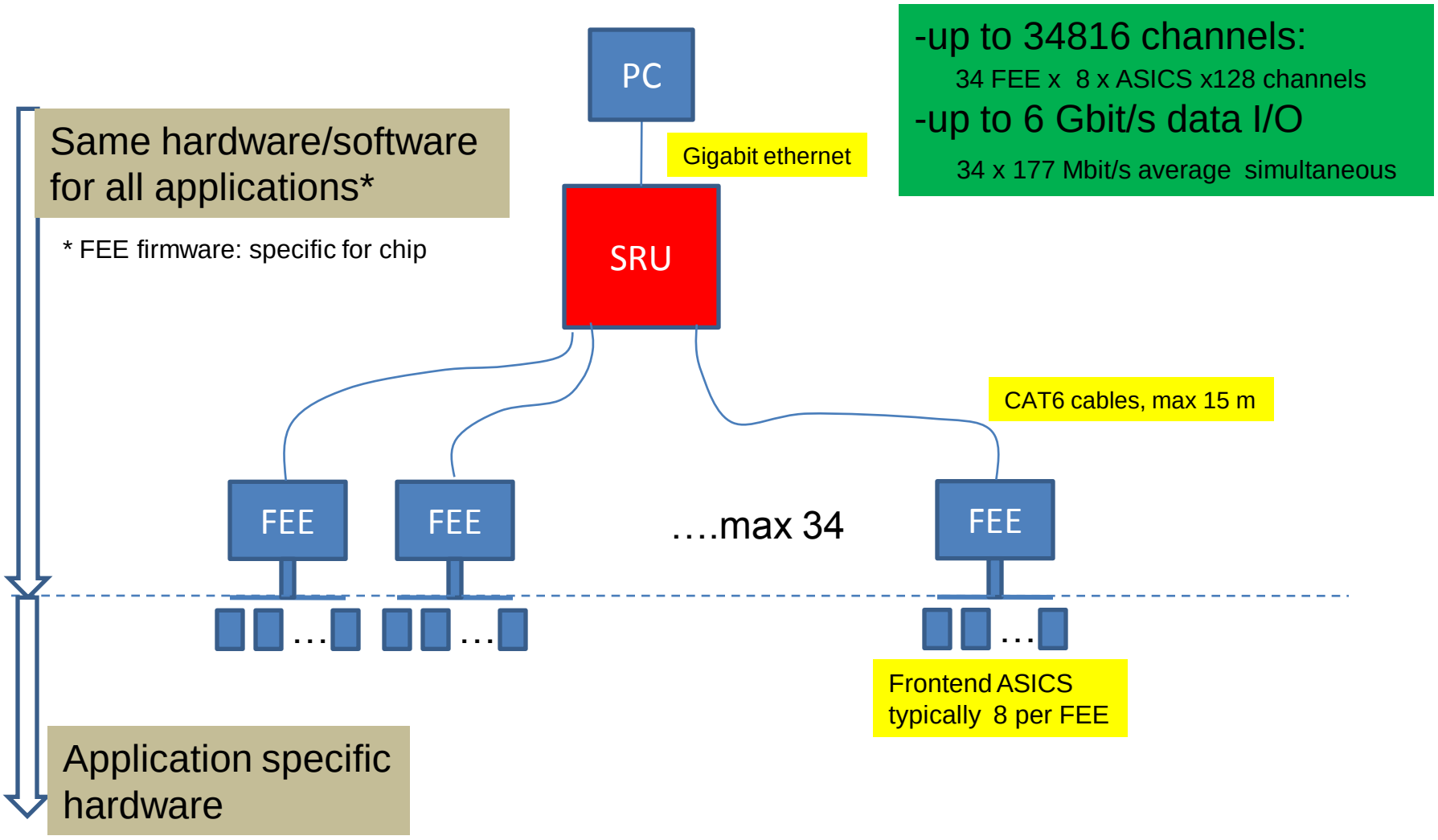
Baseline Data Analysis Package for LHC experiments

Example of Root analysis with a simple 1PC test system



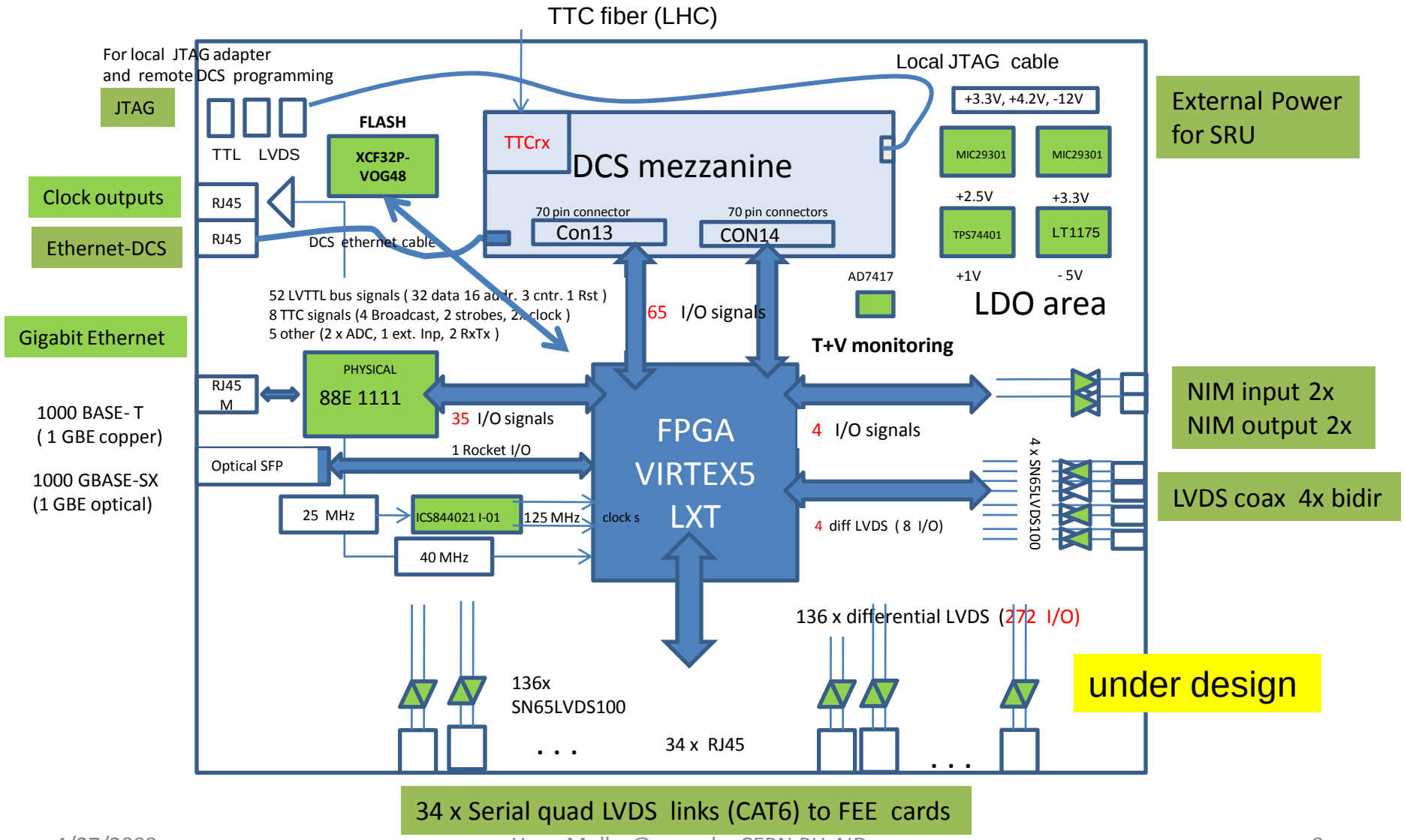


Single SRU system



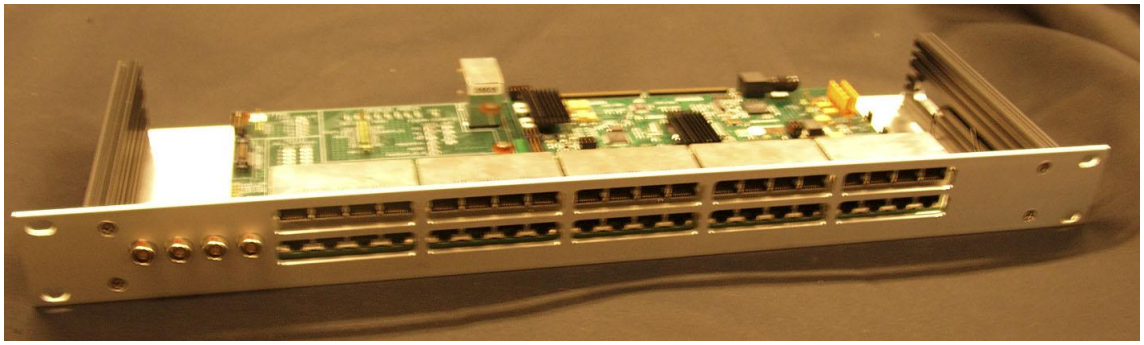
First SRU: 1 Gbit/s

based on Virtex-5 LXT FPGA



SRU board: rack mounting in 19”

Photo of a similar card with RJ45 network plugs on the front panel

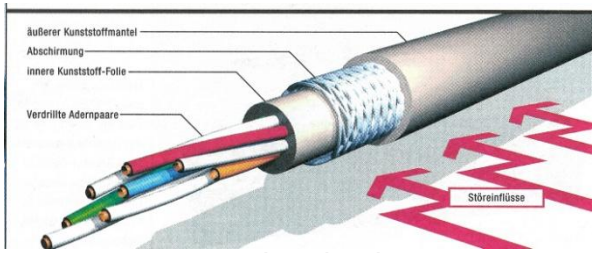


With similar layout, the SRU board will fit in 1U of a 19” chassis, power from backside

RJ45 cables to FEE’s

Trigger and clock coaxial cables

SRU<->FEE: serial LVDS



4 x twisted pairs

max 15 m @ 280 Mbit/s

clock
data
select
return

CAT 6 cable

34 x

FEE

RJ45

FPGA

4

chip Interface bus

SRU

RJ45

Reversible LVDS drivers/receivers

FPGA

4

10 GBE

Input data stream from
34 FEE's = 9.52 Gbit/s

Serial readout/contol modes over CAT6 cables

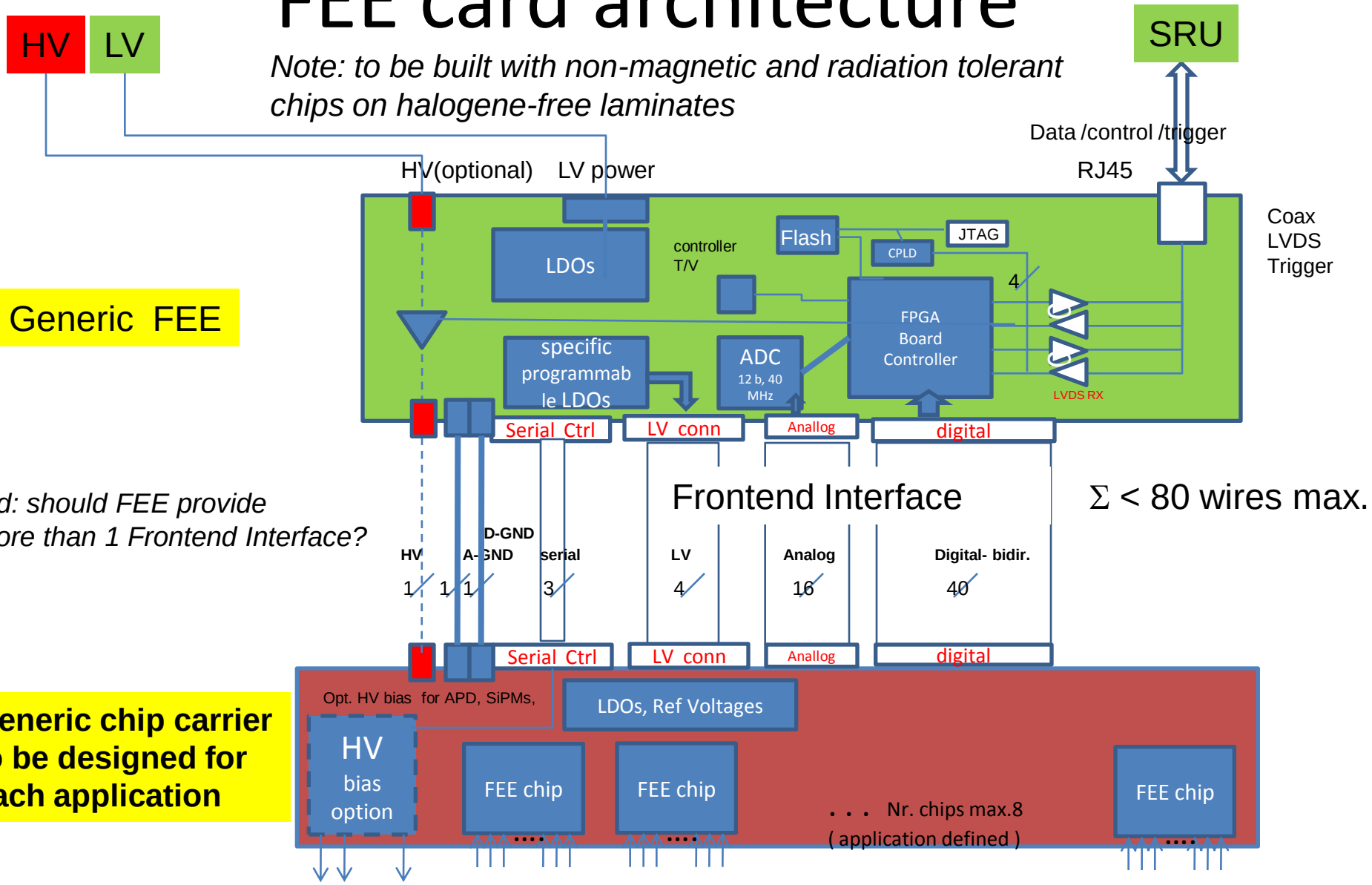
2 modes of operation defined by SRU clock
FEE board controller senses clock to switch mode

Readout mode: clock = 40 MHz to FEE
data = 280 Mbit/s to SRU
select = readout-trigger to FEE
return = local trigger to SRU

Control mode: clock <= 4 MHz to FEE
data = Serial data out to SRU
select = Serial data in to FEE
return = coded status to SRU

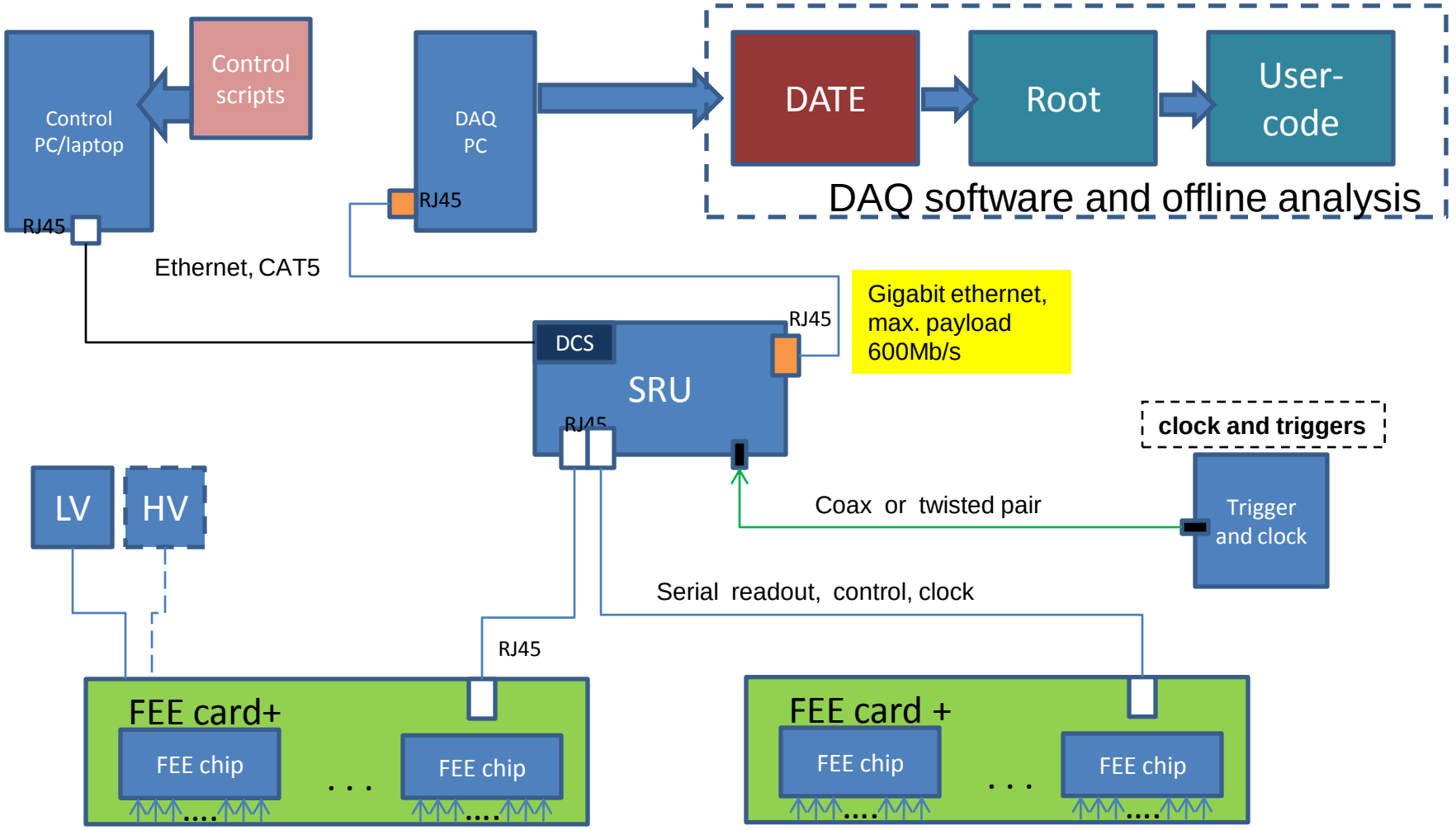
FEE card architecture

Note: to be built with non-magnetic and radiation tolerant chips on halogene-free laminates



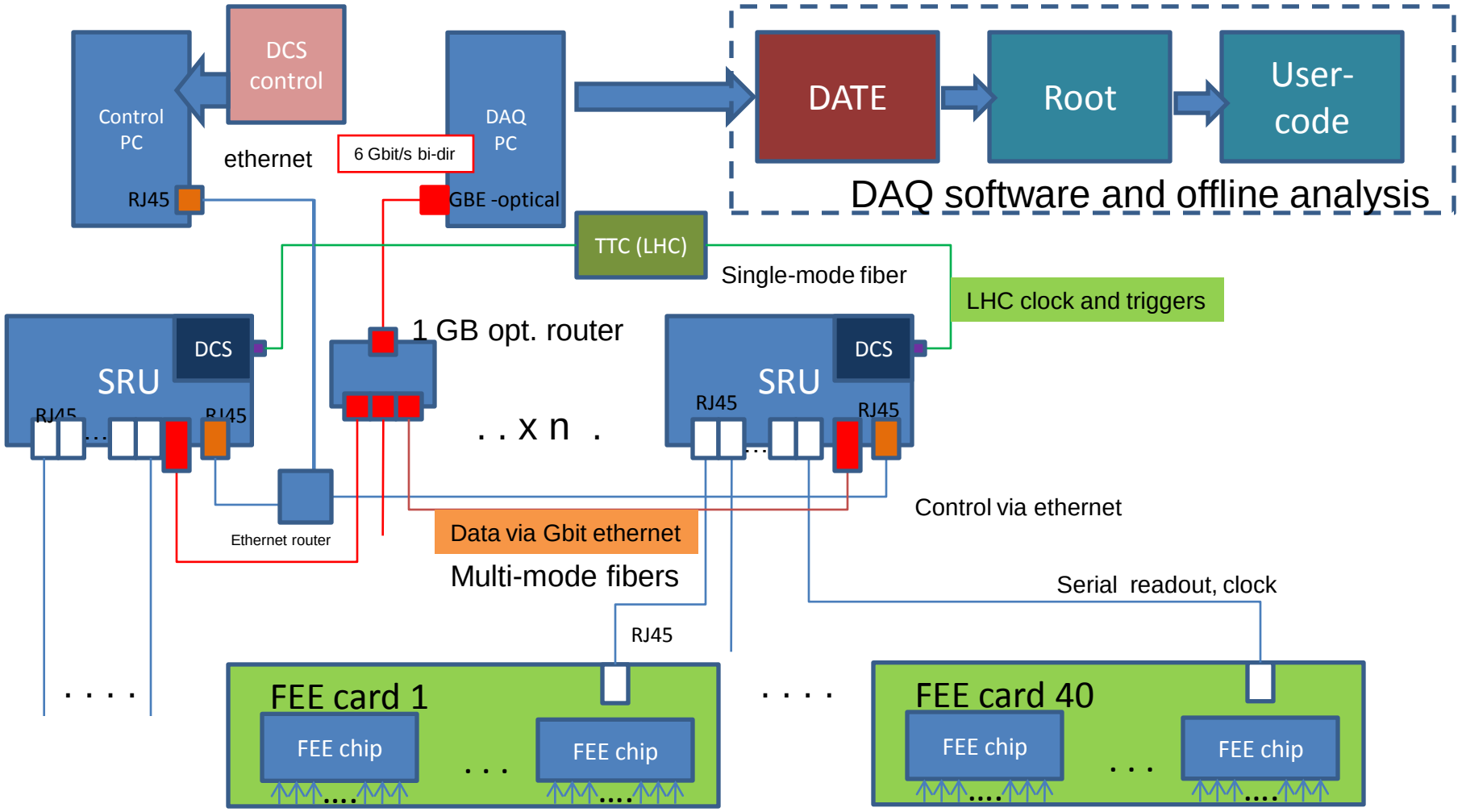
Test system architecture

1 SRU, 1 GBE copper, User trigger+clock, control ethernet/DCS



LHC architecture

n x SRU's, optical GBE router, TTC, Control via ethernet/DCS



Template Fontend chips for FEE

VFAT (Totem)
http://jinst.sissa.it/LHC/TOTEM/ch07.pdf
Digital chip for silizium detectors, rad hard
Special version with protection diodes for gas detectors
128 channels, 22 ns shaper + 1 bit ADC (comparator)->buffer
Trigger latencies up 6.4 us.
noise 650+50e/pF
programmable channel patterns for Fast OR trigger
Register parameters via I2C
USB readout board for up 64 chips (8320 channels) exists

But: No Z-suppression
no bunch identifcation for LHC
not available in bigger Qty

APV25 (CMS), also used by COMPASS and Totem
http://www.hep.ph.ic.ac.uk/cms/tracker/apv25_chip.html
Analogue chip for pixel and gas detectors
LEB99 workshop proceedings, p. 162
128 channels, preamplifier 4.5 mV/fC
50 ns shaper, Rad-hard, Multievent buffer 10 events,
192 deep pipeline sample memory @ 40 MHz
analogue output from 196 deep pipeline, peak samples multiplexed
APSP deconvolution filter to extract amplitude and time
noise 1200 e- for 20pF.
Latch mode and Sparse mode (rate up 50 kHz)
latency 4.8 us

But: No Fast OR
external I->V conversion needed

Prime candidate for startup Interface design: APV25
Longterm goal: standard IF for majority of ASIC

ALTRO (ALICE TPC and calorimeters)
Made for large TPC
http://ep-ed-alice-tpc.web.cern.ch/ep-ed-alice-tpc
Digital chip with zero-supression and multi-event buffer
requires additional preamp- shaper
frontend (PASA chip for TPC) Rad-hard for gas and photon-detectors
16 x ADC with baseline restore and ZS features
10 bit max 20 MHz
16 bit sampling pipeline, 512 deep Multi-Event Buffer
40 bit bus readout @ 40 MHz
0.25 W /chip

Only considered for upgrade of existing systems

Other chips to be considered:
Medipix, Timepix, Beetle, SVX4 , AFTER, SPIROC, MiMac…

Short term Plans

SRU: In parallel with SRU-1 proto-design
Xilinx ML505 development system is used for firmware development,
Already ongoing: making of IP packet frames for Gigabit ethernet
(Univ. Valencia, CERN)

FEE: Add serial RJ45 port to existing FEE card for new calorimeter with Altro chip to replace TPC-like parallel readout bus.
Develop Board controller for serial readout
(Huazhong Normal University, CCNU, Wuhan)

DAQ: Add a UDP interface to I/O software of DATE. Initially use software- generated IP packets, then change over to hardware generated ones. (DAQ team of CERN-ALICE)

Readout: DAQ-SRU-FEE:
Make SRU firmware look for the DATE software like RCU firmware of the ALICE TPC. Readout of an Altro on the FEE via serial port to SRU
(all above teams, test applications: Alice EMCal upgrade, ATLAS MMega)

Medium/ long term plans

(manpower tbd)

- design and build standard FEE front interface to chip carriers
- build FEE-1 card with board controller firmware
- design and build the following chip carriers and firmwares

  -VFAT for digital readout

  -APV25 for analogue readout

  -ALTRO with frontend for calorimeters

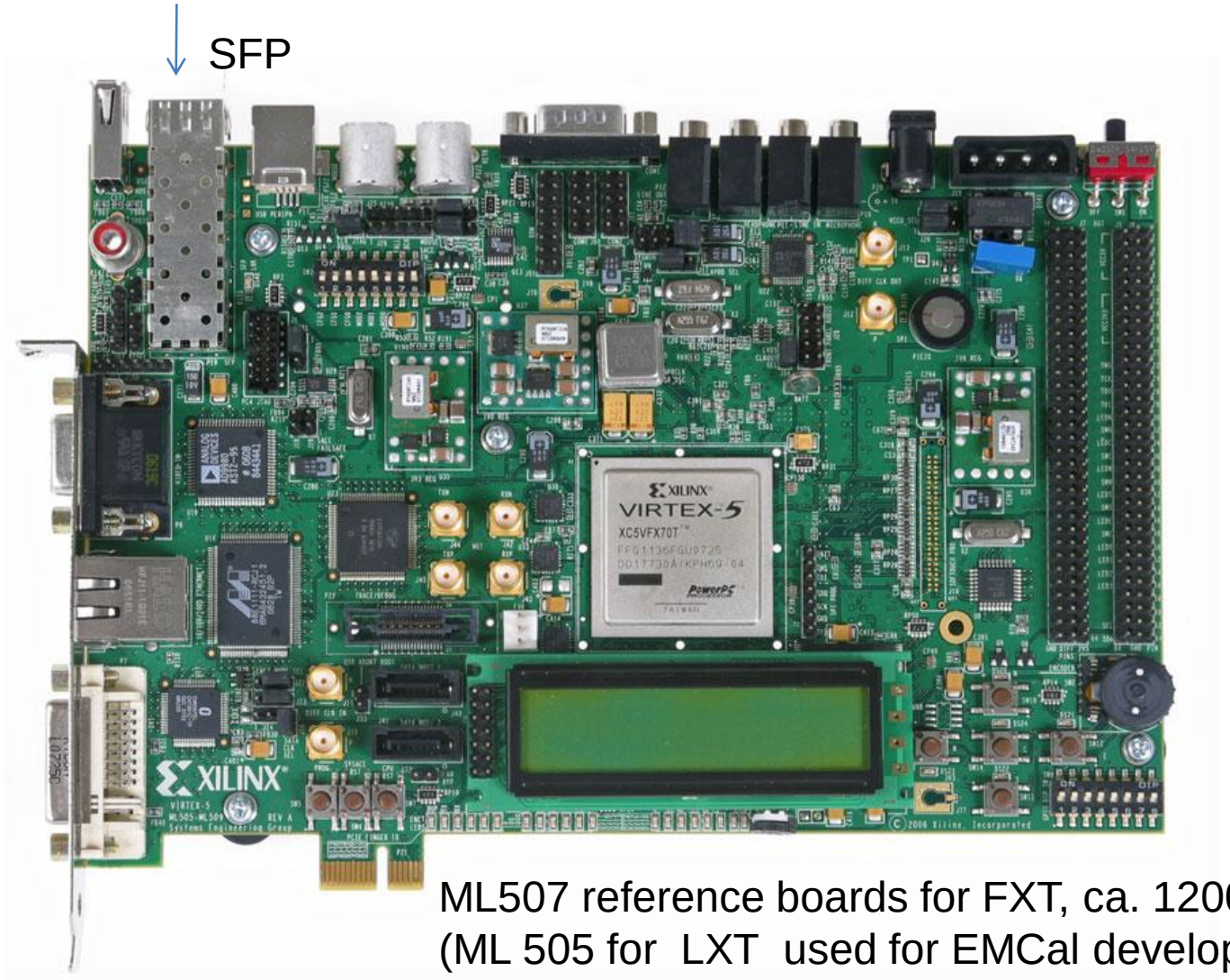
  -“ideal chip” …. still to be defined !
- upgrade SRU to 10 Gbit capability (optical SFP+)
- upgrade FEE to compatibility with “ideal chips”
- Commission first SRS application with DATE and offline Root packages

Summary

- Coordinate users, engineers and project managers in order to build and deliver a scalable readout system
- Build up upon existing technologies
- Startup defacto done and advancing well with team of experienced engineers in all domains
- Use industry-standard readout backend and supported DAQ system
- Provide flexibility on the chip frontend
- Participation on all levels welcome !

Backups

development platform already in use



ML507 reference boards for FXT, ca. 1200 USD
(ML 505 for LXT used for EMCal development)

Ad interim: add SRU port to existing FEE

(in use by ATLAS MMega)