Digital Signal Integrity and Stability in the ATLAS Level-1 Calorimeter Trigger

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Abstract

The ATLAS Level-1 calorimeter trigger is a hardware-based system with the goal of identifying high-p_{T} objects and to measure total and missing E_{T} in the ATLAS calorimeters within an overall latency of 2.5 μs. This trigger system is composed of the Preprocessor which digitises about 7200 analogue input channels and two digital processors to identify high-p_{T} signatures and to calculate the energy sums. The digital part consists of multi-stage, pipelined custom-built modules. The high demands on connectivity between the initial analogue stage and digital part and between the custom-built modules are presented. Furthermore the techniques to establish timing regimes and verify connectivity and stable operation of these digital links will be described.

I. Introduction

The ATLAS trigger system consists of the hardware-based Level-1 trigger and two software-implemented high level trigger stages for further event selection. The ATLAS Level-1 trigger system provides a trigger decision within 2.5 μs and reduces the LHC bunch-crossing rate of 40.08 MHz to a rate less than 100 kHz. The Level-1 selection of interesting and rare events is based on reduced granularity calorimeter and muon detector data. The Level-1 trigger determines Regions-of-Interest (RoI) from which the algorithms of the next high level trigger are seeded. The high level triggers reduce the data rate to about 200 Hz for data storage. Trigger information is processed by the Level-1 calorimeter trigger and the Level-1 muon trigger. In the case of the Calorimeter trigger, the complete hardware components were tested in 2007 and finally installed in the end of 2007. This calorimeter trigger identifies electron/photon-like, tau-like and jet-like clusters above programmable transverse energy thresholds and compares the calculated energy sums against programmable thresholds. The results of the Level-1 trigger subsystems are combined in the central trigger processor (CTP) [1] which decides about the acceptance or rejection of an event. The latency of 2.5 μs is the maximum allowed time to transmit the signals from the calorimeter, to find high-p_{T} objects and to receive the acceptance signal (L1A signal) from Level-1 trigger at the front-end electronics. The data transmission takes up most of this time. The architecture and the algorithms have to be simple enough to process over a large number of input signals in this limited time. The physics algorithms are performed by FPGAs which are flexible and fast. The algorithms use the mechanism of overlapping, sliding windows which requires transfer and sharing of a large amount of digital data between eletronic modules. The different stages of processing data in the system need to be properly connected and timed in to allow optimal performance of the system. The system tests on the duplication and transmission of data within the digital part of the system and the timing procedure to ensure stable operation will be reported.

II. The ATLAS Level-1 Calorimeter Trigger

The basic architecture of the system is documented in [2]. A simplified schematic of the calorimeter trigger is shown in Figure 1. The real time data path consists of three subsystems: Preprocessor (PPr), Cluster Processor (CP) and the Jet/Energy-sum Processor (JEP). The Preprocessor which contains 124 modules is the initial analogue stage of the system. The PPr digitises the input channels and provides the input data for the CP and the JEP. The PPr consists of eight crates of 9U VME modules.

Their input data are analogue pulses mostly corresponding to a 0.1×0.1 in eta/phi space (so called trigger towers), separately for the electromagnetic and hadronic calorimeter compartments. The data is then sent downstream to the CP and JEP systems using LVDS 400 Mbit/s serial link chipsets. The Cluster Processor (CP) consists of 56 Cluster Processor Modules which locate and count electron/photon and single tau/hadron candidates. The final results are then summed by the Common Merger Modules (CMM) and sent to the CTP. The Jet/Energy-sum Processor (JEP) consists of 32 Jet/Energy Modules (JEM) which count and identify jet candidates and calculates total and missing transverse energy. Their final results are also summed by CMMs. This digital part of the system occupies 6 custom-built processor crates with a high density backplane with 22000 pins to support the transfer of a very large amount of data.
The read-out and Region-of-Interest data is handled by 20 Read-out Driver modules (ROD). These receive the data on optical links running at a maximum speed of 800 Mbit/s. These reformat the data to standard ATLAS data fragments and transmit them using the ATLAS standard S-Link protocol.

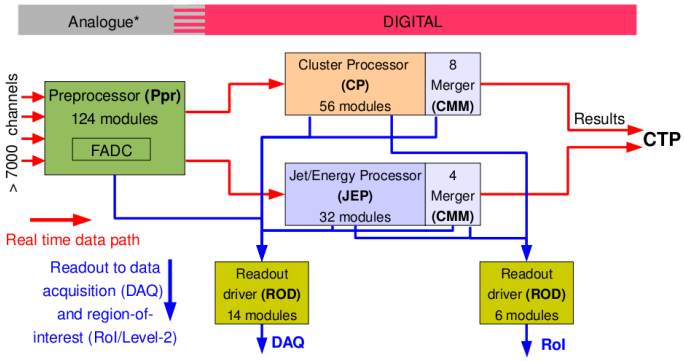

Figure 1: Module types, numbers and connectivity in the Level-1 calorimeter trigger system

The connections of the Preprocessor to the system processors CP and JEP are crucial issues for a working system. These connections consist of more than 1800 LVDS cables each carrying 4 separate input signals and additional data duplication links due to the sliding window algorithms. The read-out of the systems need to be properly aligned to ensure to read-out the correct event with its bunch-crossing identification. In the next section the tests for these connections and read-out links will be explained and the results for the system presented.

III. Digital Signal Integrity and Stability

This section will concentrate on the results from the timing calibrations and the stability tests of the system. The system will be divided into three parts. These parts are illustrated in Figure 2. The sliding window algorithm [3] requires sharing and duplicating of the data in eta and phi. This overlap in eta and phi is created in two steps in the system indicated in the Figure 2. The incoming data is transmitted to both processor systems. These connections are LVDS 400 Mbit/s serial links between the Preprocessor crates and the JEP/CP custom crates, the so called inter-crate connections. The trigger towers are digitised to 8-bit transverse energy as input data for the CP system and 4 trigger towers are summed up to build 9-bit jet elements for the JEP system. The input data to both processors needs to be timed in (input timing scan). Furthermore within the processor systems data is shared via fan-in/fan-out between neighbouring modules with up to 160 Mbit/s in one crate and sent to the CMMs over a custom made high density backplane including VME connections. To latch the fan-in/fan-out data correctly and synchronously into the FPGAs for processing we need to calibrate the timing of each module. These connections are labelled as inter-module connections in Figure 2. The data is afterwards read-out via Glink optical fibres with a maximum of 800 Mbit/s (read-out links) and transmitted to the RODs.

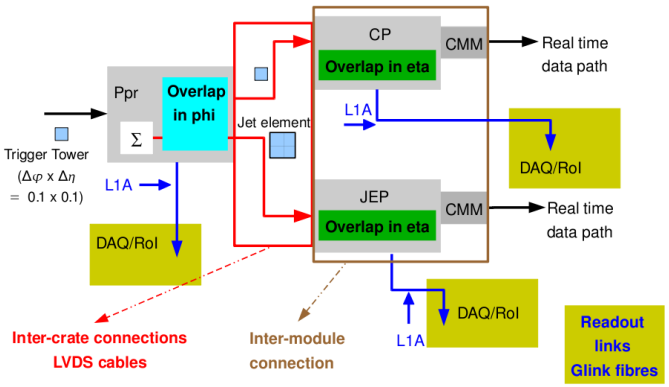

Figure 2: Overview of connectivity in the Level-1 calorimeter trigger system

Now the tests and timing procedure for these three type of connections will be described in detail.

A. Inter-crate Connectivity

The Inter-crate connectivity is established by LVDS serial links which enter the modules through the backplanes. The LVDS cables transmit the input data to the CP and JEP systems. Every channel and every cable needs to be tested to verify the correct data transmission between the subsystems and also every input channel requires its own time settings. Because of device and cable skew all serial links operate on different phases. This connectivity is tested with the help of firmware integrated checks on status of the link and parity errors. Furthermore the data reception and processing can be tested with the help of the comparison between the simulation and the read-out of the hardware. The correctness of the cable mapping can be checked with a specific test pattern unique for every channel. These checks can find misconnected cables and hardware problems of cables, source or receiver modules and backplanes. These cabling problems were found at the 0.5% level, and these problems have been identified and fixed.
The CP and JEP systems are driven by 2 deskew clocks (so

called deskew 1 and 2) derived from the overall bunch clock (40.08 MHz). These clocks deskew the bunch clock to a sub-nanosecond accuracy to compensate delays of the input signals and to time in the fan-in/fan-out signals. These clocks have an adjustable delay of 240 steps each 104 ps long. The deskew 1 clock is responsible for the input synchronisation and these signals are latched into the FPGAs on one of two clock phases derived from the global LHC bunch clock (see Figure 3). This is the coarse time setting for the input signals. An additional offset in phase by a full tick would then need to be determined by diagnostic spy memories. This can then be corrected by applying programmable length pipelines in the FPGA to delay input data by a full tick.

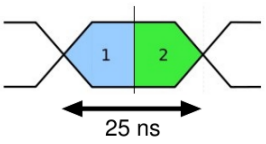

Figure 3: LHC bunch clock phase

The time settings for phase and delay of the input channels are established in a calibration run with synchronous data patterns by passing through all 240 steps of the deskew clock and reading out the parity error counters for each step. The delay is determined by calculating the misalignment between the data in each channel in units of clock ticks. The choice of the phase is made by analysing the number of parity errors in each phase and to choose the one with less errors. Such input timing scans are shown in Figures 4 in case of the JEP and in Figure 5 in case of the CP.

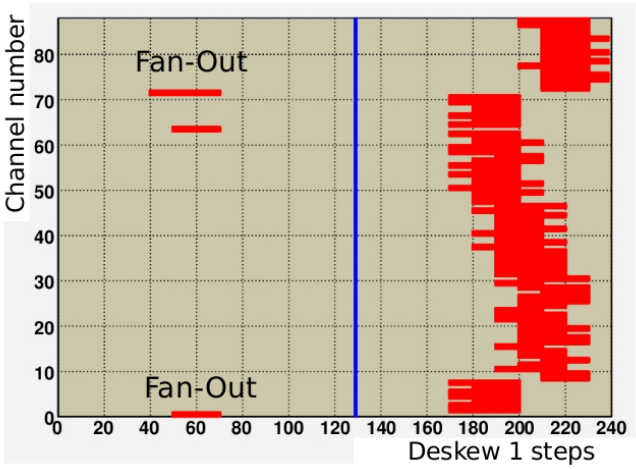

Figure 4: Input timing scan of one Jet/Energy module

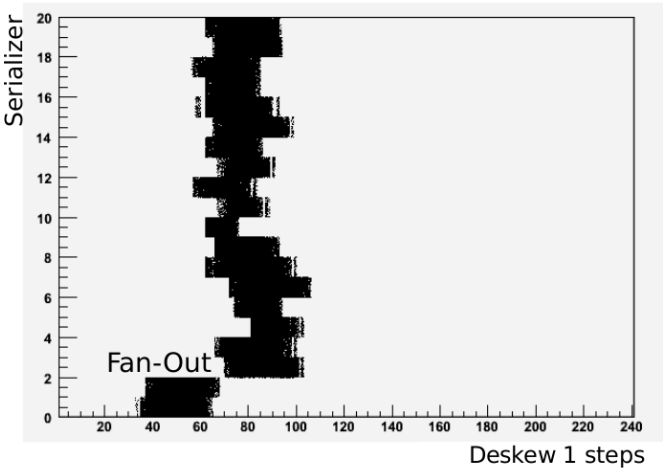

Figure 5: Input timing scan of one Cluster processor module

The bars in Figure 4 and 5 represent the sampled parity errors for each time step. Some channels and serializers show slightly different behaviour because they are receiving data from different quadrants with a different timing (fan-out channels). These Figures show that the system has a good time margin of 15 out of 25 ns. So one chosen phase always will have valid data.
This calibration procedure discovered a variety of hardware problems of which none was serious and all have been revised. Very few problems were found on the CP and JEP processor modules and a couple of problems on the Preprocessor modules.

B. Inter-module Connectivity

This connectivity creates the overlap regions on every module to support algorithms based on sliding windows. Every module duplicates 3 out of 4 input channels and transmits them to its right and left neighbours. Figure 6 shows a schematic drawing of the traffic on the backplane for this purpose. The data is transmitted via the backplane connectors with a speed up to 160 Mbit/s. The backplanes have about 22000 pins.

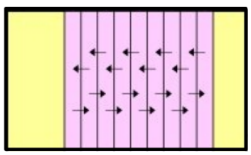

Figure 6: Backplane traffic for Fan-In/Fan-Out

The deskew 2 clock times the data processing of all FPGAs with a sliding window algorithm to identify electrons/photons, taus and jets. Every processor and every system configuration require their own calibration constants. The data needs to

latched in the FPGAs error-free. The time settings are determined by a fan-in/fan-out timing scan. This procedure enables 10-bit counters on each module, steps through each deskew 2 clock setting and samples parity errors for each clock step. This data is then analysed to find a valid time window for processing the input data and the shared data. The JEP system works with a fan-in/fan-out data speed of 80 Mbit/s and the CP system works with twice this speed. One would expect that the valid time window is therefore about half of that from the JEP system.

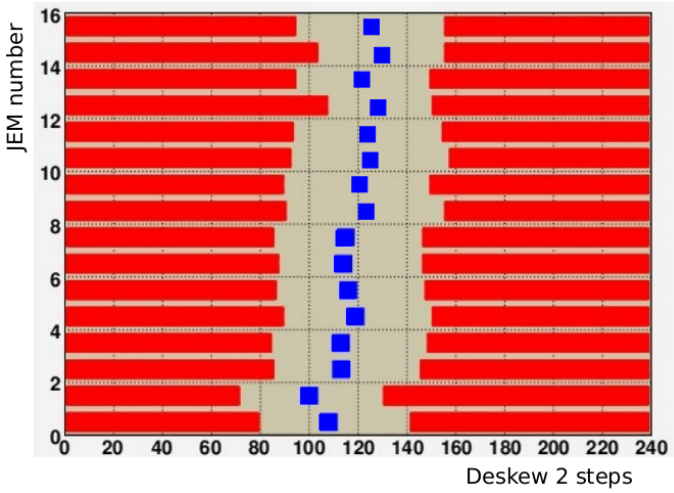

Figure 7: Fan-in/Fan-out timing scan of one crate of the JEP with a signal speed of 80 Mbit/s

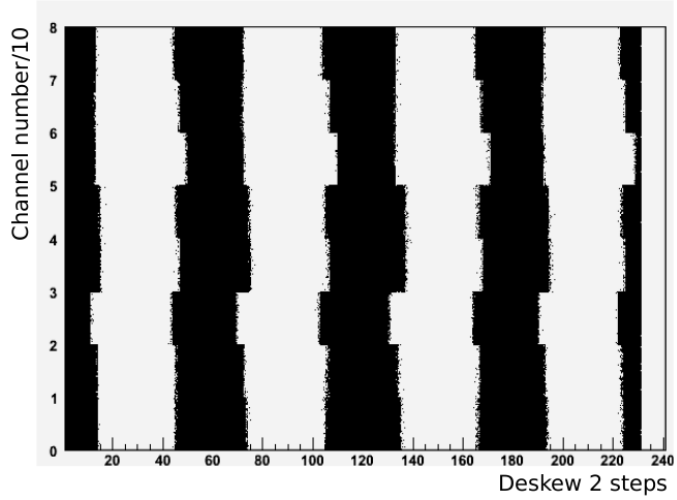

Figure 8: Fan-in/fan-out timing scan of one CPM with a signal speed of 160 Mbit/s

In Figure 7 a result of such a fan-in/fan-out timing scan is shown. The dark regions in the Figure mark where parity errors occurred. The actual time setting is then determined by choosing the point which is as far as possible away from the error bars. In general such a window would have a size of 5-7 ns which was proven to be sufficient for a error-free transmission. The CP system is similar but the data speed is 160 Mbit/s. The result of the timing scan shows four valid time ranges for different phases. One valid window size is about 2-3 ns. The timing procedure is equivalent and Figure 8 shows the result of a fan-in/fan-out timing scan of one CPM.
These procedures discovered hardware problems of the backplanes where connections were missing. These problems were caused on the one hand by difficulties at the production stage and on the other hand by damage during installation. All backplanes were additionally computer-scanned via a microscope in 2007. Each backplane had an average of 1-2 faults. In Figure 9 a bent pin which was damaged by module insertion can be seen. These problems were all fully solved.

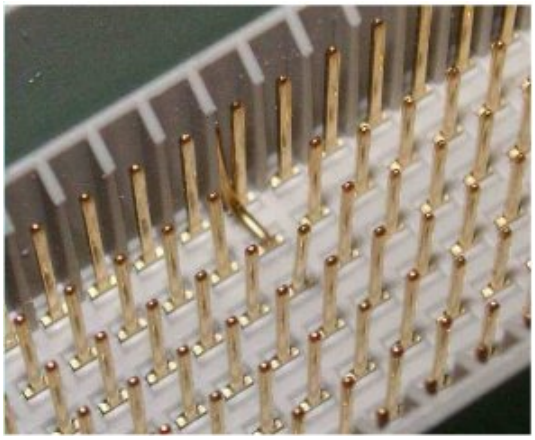

Figure 9: Bent pin of a production backplane at CERN after module insertion

C. *Read-Out links*

The read-out links are running at a maximum of 800 Mbit/s using the Agilent G-Link protocol [5]. The read-out is initiated if the processors receive an acceptance signal from the CTP. For a functional read-out one needs to determine the so called read-out pointers for each subsystem to fetch the correct event which was accepted from the data buffers in the processors. Figure 10 illustrates this correlation.

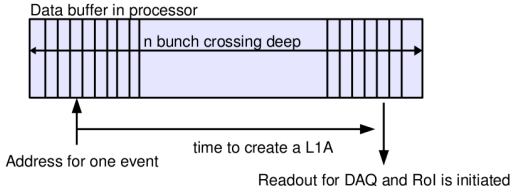

Figure 10: Schematic of the data buffers in a subsystem

Offline analysis of special data can provide the correct time

settings for the read-out pointers. To determine these a standalone run with playback data is needed in which a fake L1A rate forces a read-out. The playback data only contains one event which is unequal to zero. The read-out always includes 5 adjacent time slices and therefore looking at the data stream provides you with information of the alignment of the system. This is illustrated in table 1.

Table 1: Illustration of read-out pointers

Default	0	0	data	0	0
Hardware output	0	data	0	0	0

These settings are necessary to match the data to a bunch crossing and are automatically checked in every read-out. In the commissioning phase the read-out was tested with random triggers up to 60 kHz and the result was that the event synchronisation was stable during a long running time.

IV. Conclusion

The hardware of the Level-1 calorimeter trigger was completely installed by December 2007. The years 2007 and 2008 was dedicated to the installation and commissioning of all components. The signal integrity was tested and proven by establishing and verifying the inter-crate and inter-module connectivity and read-out pointers. In detail the cabling and processors were fully tested and backplane connections are completely functional. The read-out pointers were confirmed in various data analysis. The procedures for establishing correct data processing were presented. Each subsystem is calibrated with respect to input data and fan-in/fan-out data. The system is has been exercised by taking cosmic-ray data for a long time, and is now ready for taking first collision data.

Acknowledgments

We wish to acknowledge the work of the ATLAS TDAQ community in providing the underlying online software and infrastructure for triggering, read-out and data flow. We would also like to thank the ATLAS calorimeter communities, in particular those working on the trigger tower builders and receivers, for their efforts to provide genuine input signals to the trigger. Finally the successful installation of the infrastructure and cabling would have been impossible without the careful work of many technicians connected to the institutes involved.

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