Digital signal integrity and stability in the ATLAS Level-1 Calorimeter Trigger

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on behalf of

ATLAS Level-1 Calorimeter trigger collaboration:

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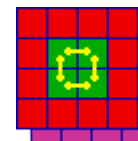
Kirchhoff-Institut für Physik, University of Heidelberg, Heidelberg, Germany

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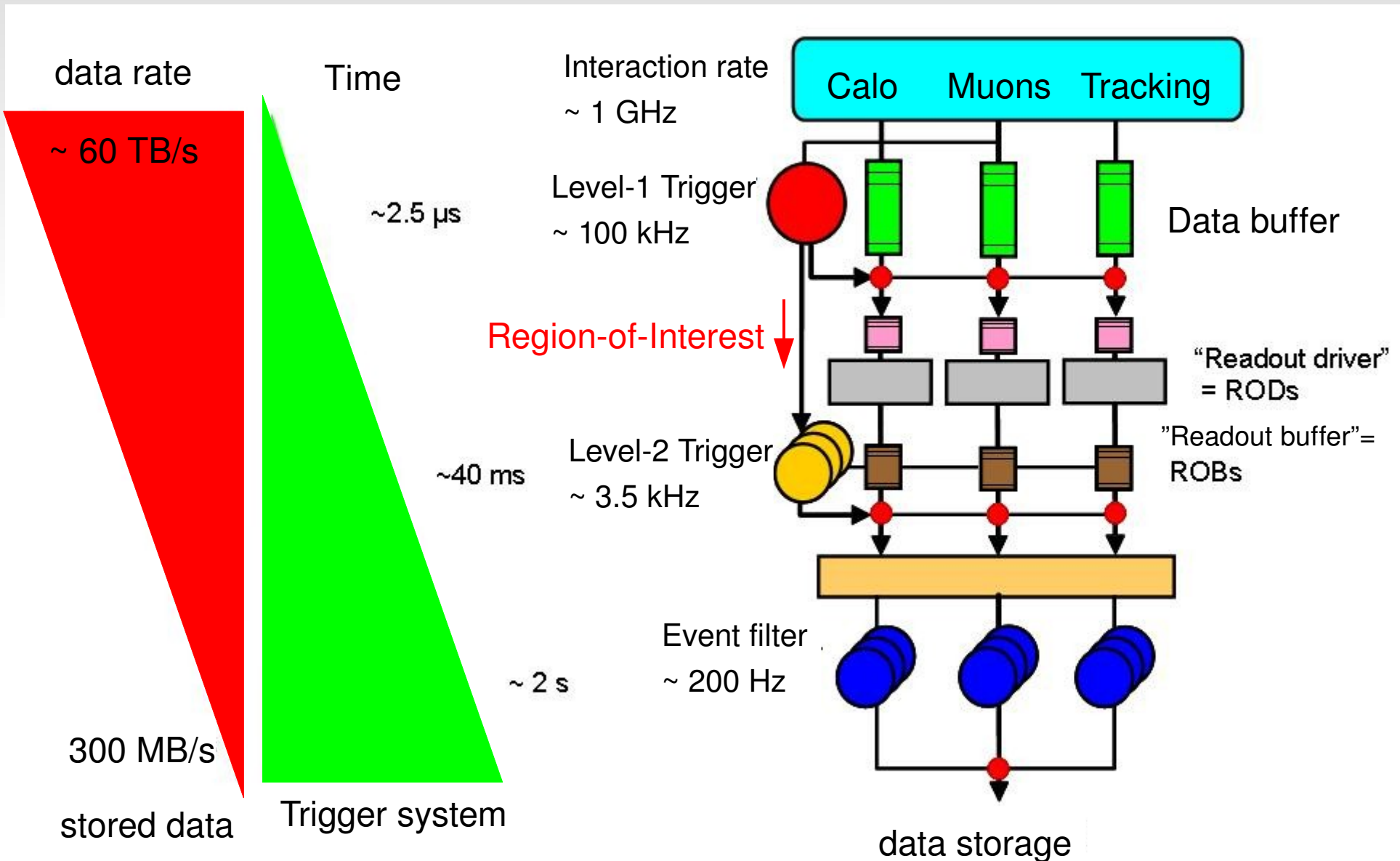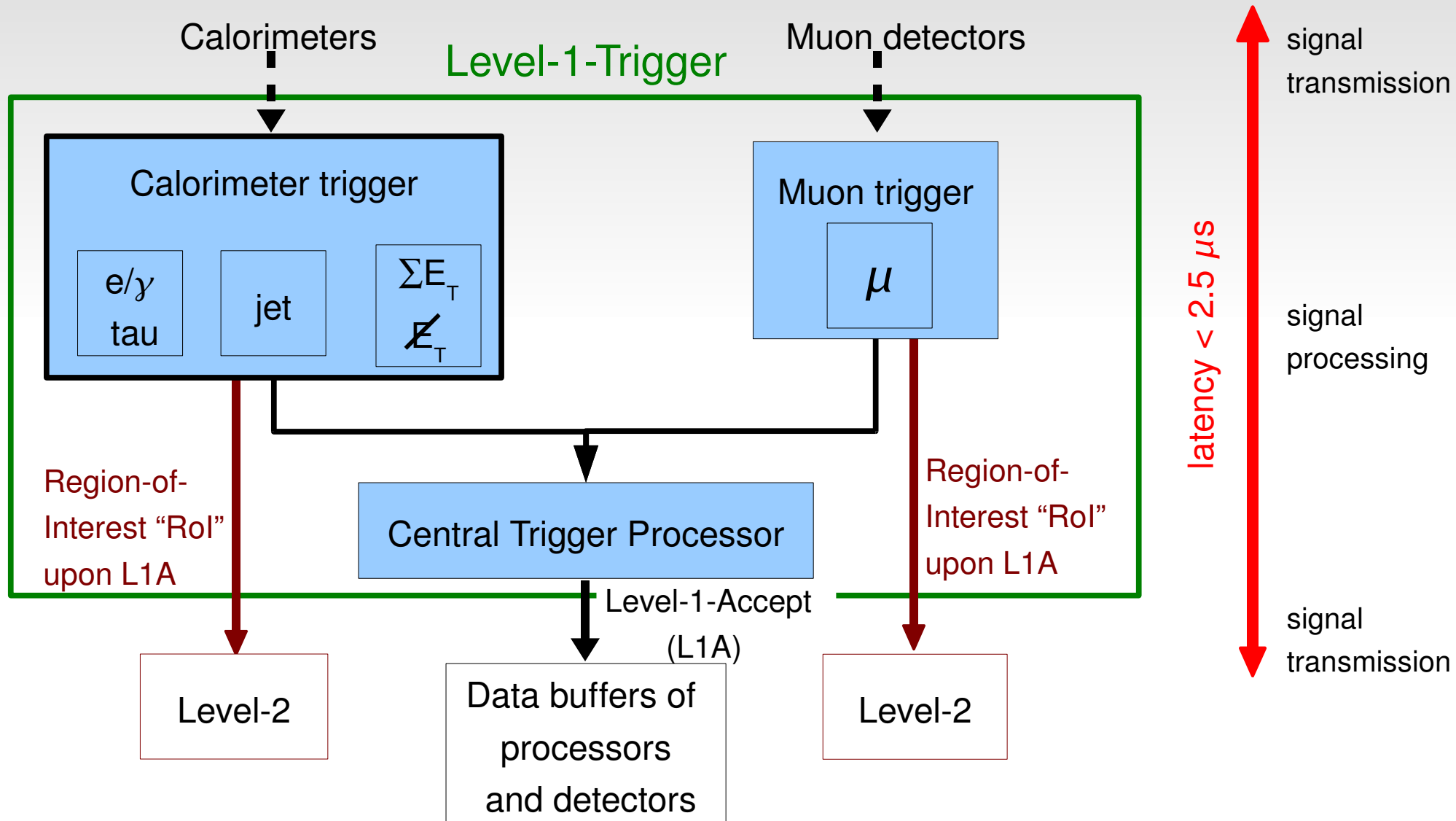JOHANNES GUTENBERG UNIVERSITÄT MAINZ

Outline

- Introduction to the trigger system
- Digital signals in the Level-1 Calorimeter trigger
  - Challenges on data treatment
  - Inter-crate connectivity
  - Inter-module connectivity
  - Readout links
- Conclusions

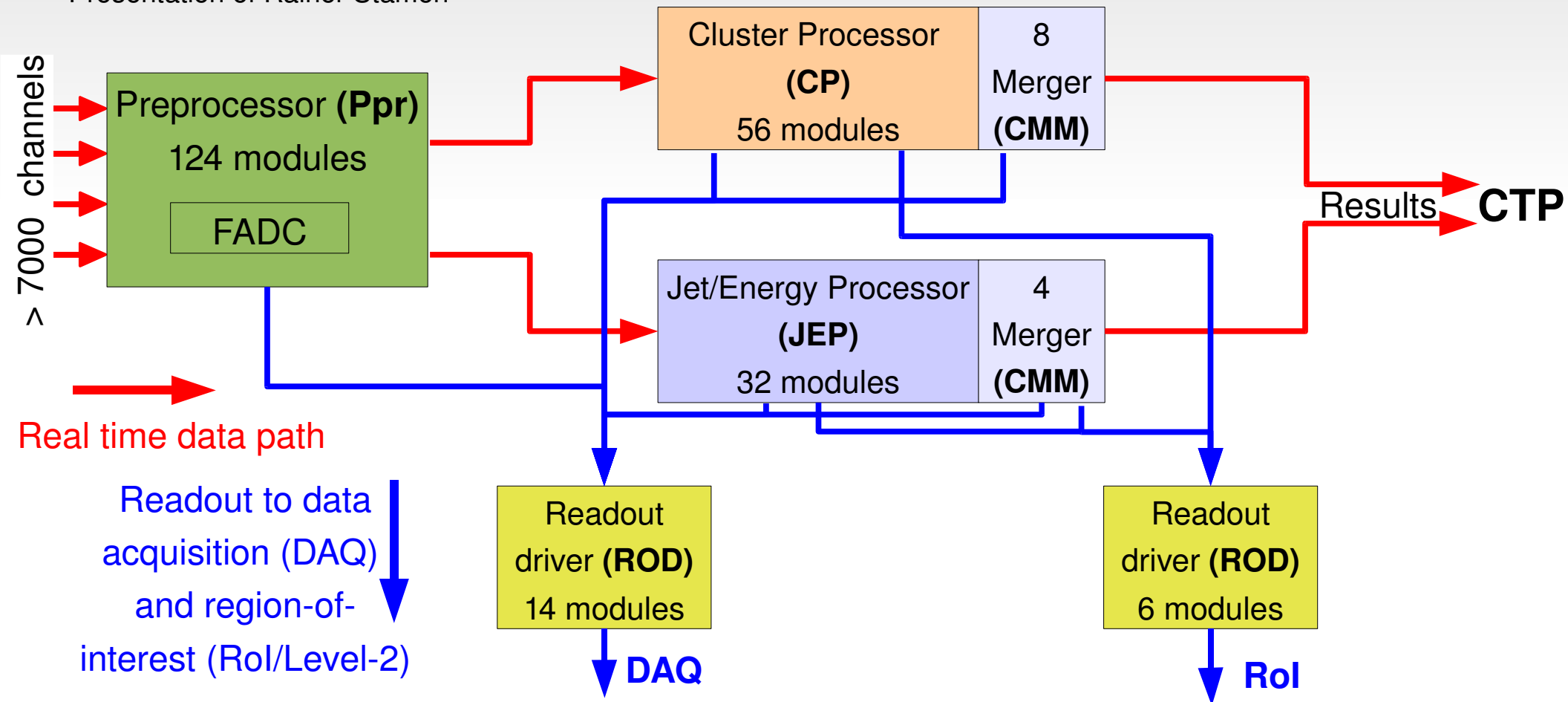# Introduction: Trigger System

Level-1 System

Level-1 Calorimeter Trigger

The Electronic cavern

Analogue cables

Complete installation in the end of 2007

4 out of 8 Preprocessor crates

ROD + JEP + CP

Digital signals in the Level-1 Calorimeter Trigger
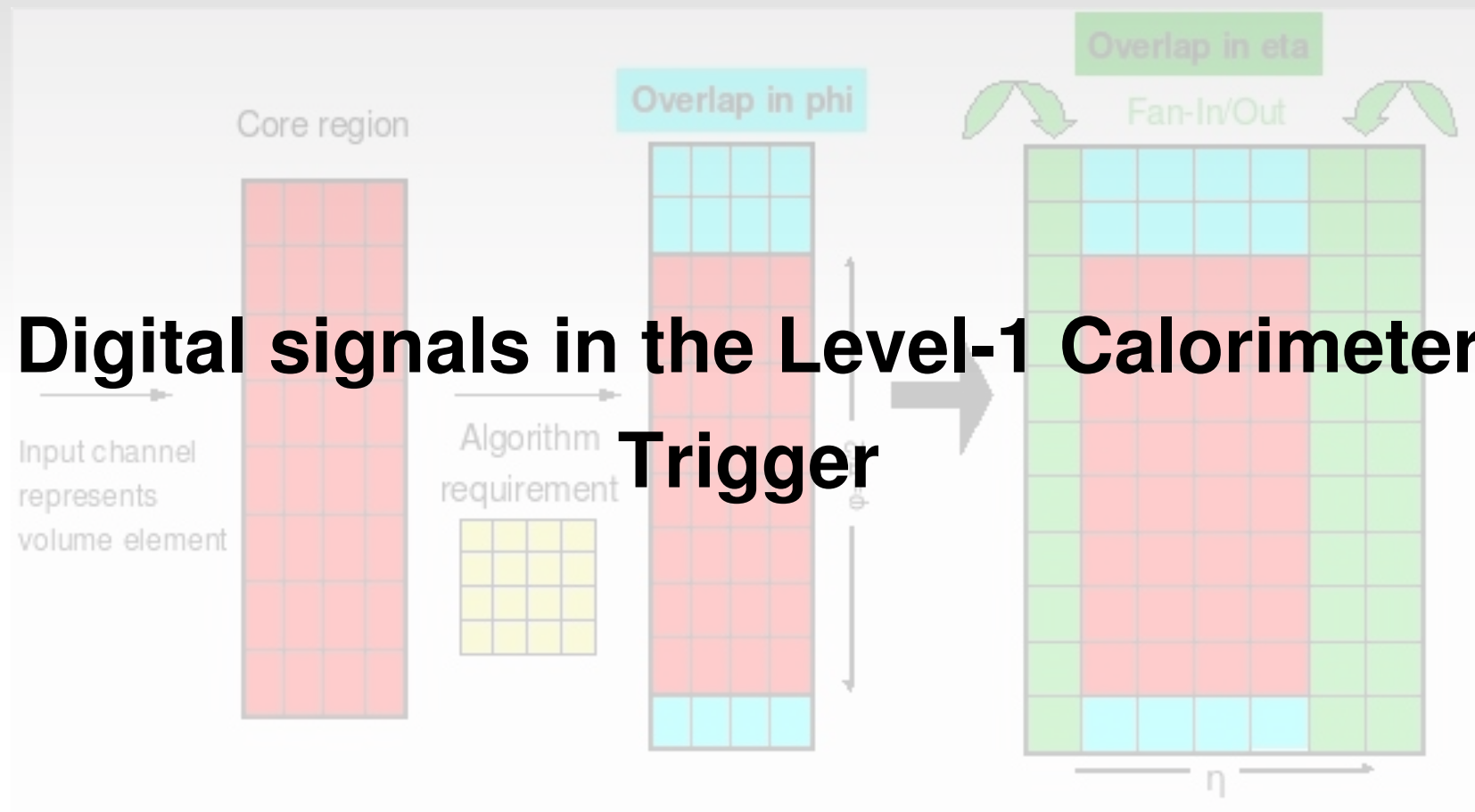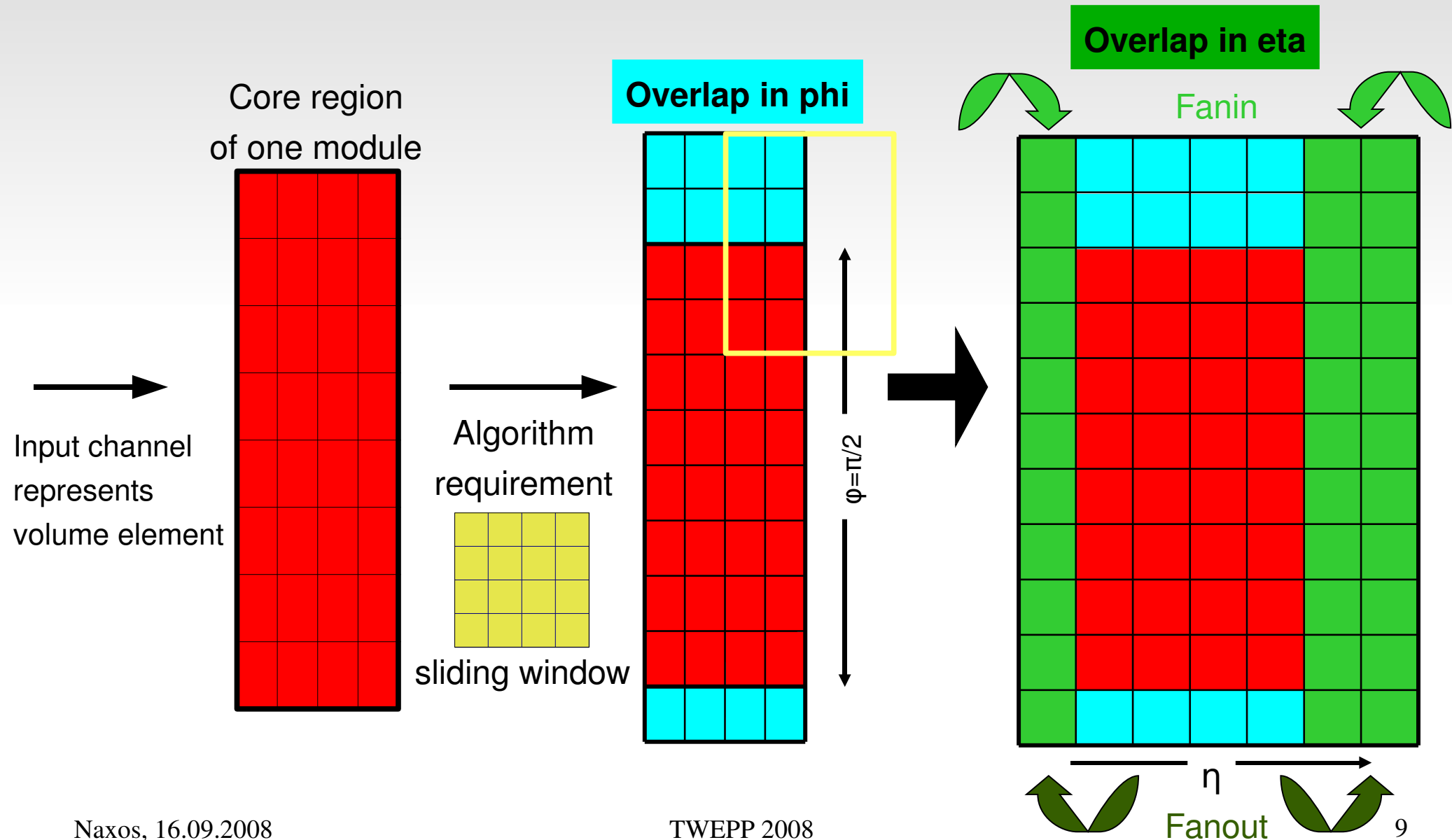
Challenges on data treatment

- Two in parallel working processor systems working with 40 MHz bunch clock rate need:

  - more than 1800 serial cables

  - 22000 backplane connectors in each crate

  - more than 350 optical fibres

- Latency in Calorimeter trigger under 1 μs

- Time is consumed:

  - signal treatment and conversion

  - in each process/algorithm

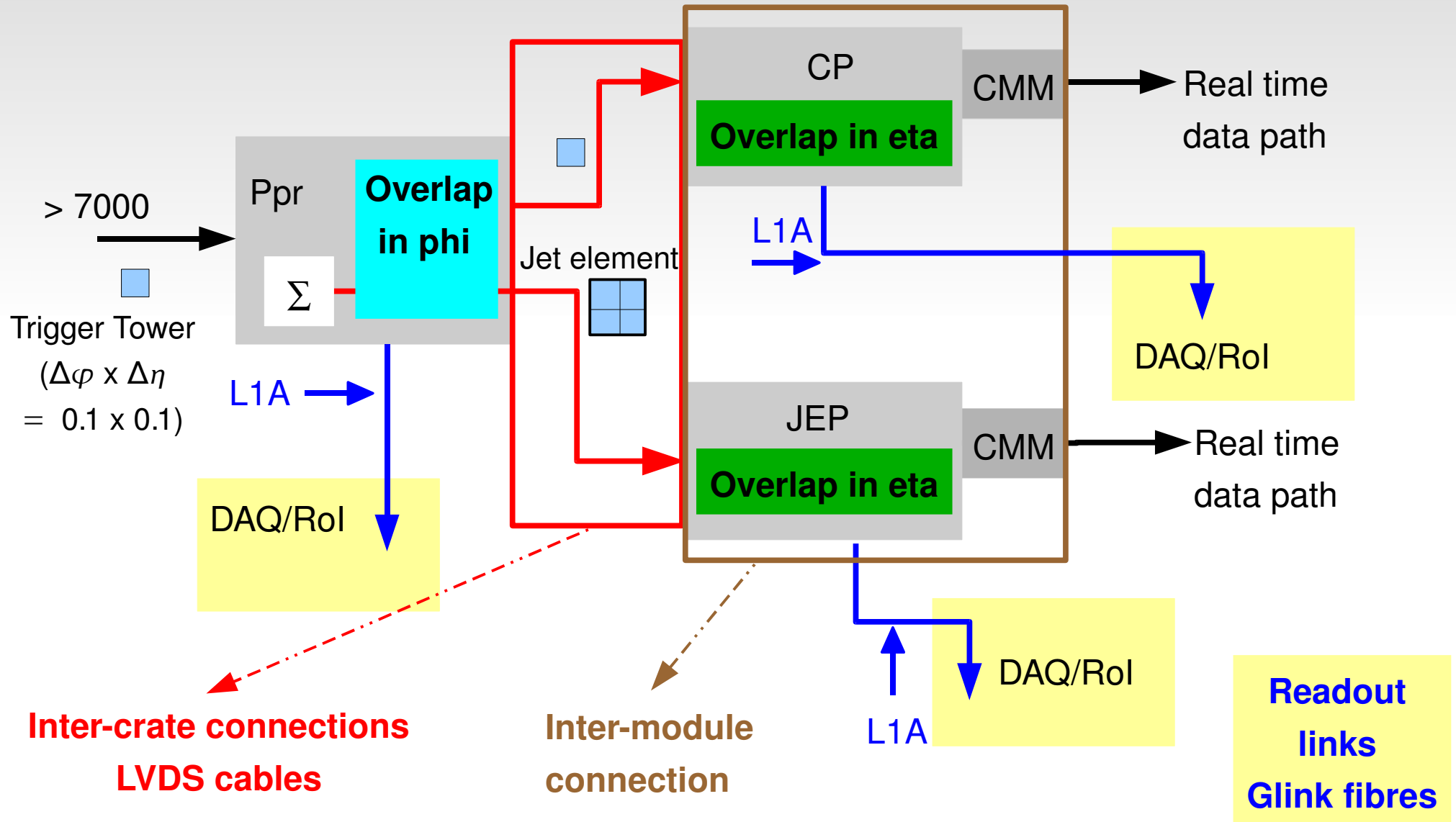 - every transmission

Timing is crucial for performance of system

Processor data environment

Example of JEP system: (CP is similar) for jet, e/γ and tau algorithm

Digital signals

> 7000

Trigger Tower
$(\Delta\varphi \times \Delta\eta = 0.1 \times 0.1)$

Ppr

Overlap in phi

L1A

DAQ/RoI

Jet element

CP

CMM

Overlap in eta

L1A

Real time data path

DAQ/RoI

JEP

CMM

Overlap in eta

Real time data path

L1A

DAQ/RoI

**Inter-crate connections
LVDS cables**

**Inter-module
connection**

**Readout
links
Glink fibres**

Timing issues

- Real time path timing:

  - input data for each processor (input timing scan)

  - sharing data between neighbouring modules (Fanin/Fanout timing scan)

  - connection of merger modules through backplane and cable links (JEP/CP-CMM, CMM-CMM, CMM-CTP) (parity errors)

- Readout timing:

  - settings for readout pointers for every processing stage (alignment of data)

Inter-crate connectivity
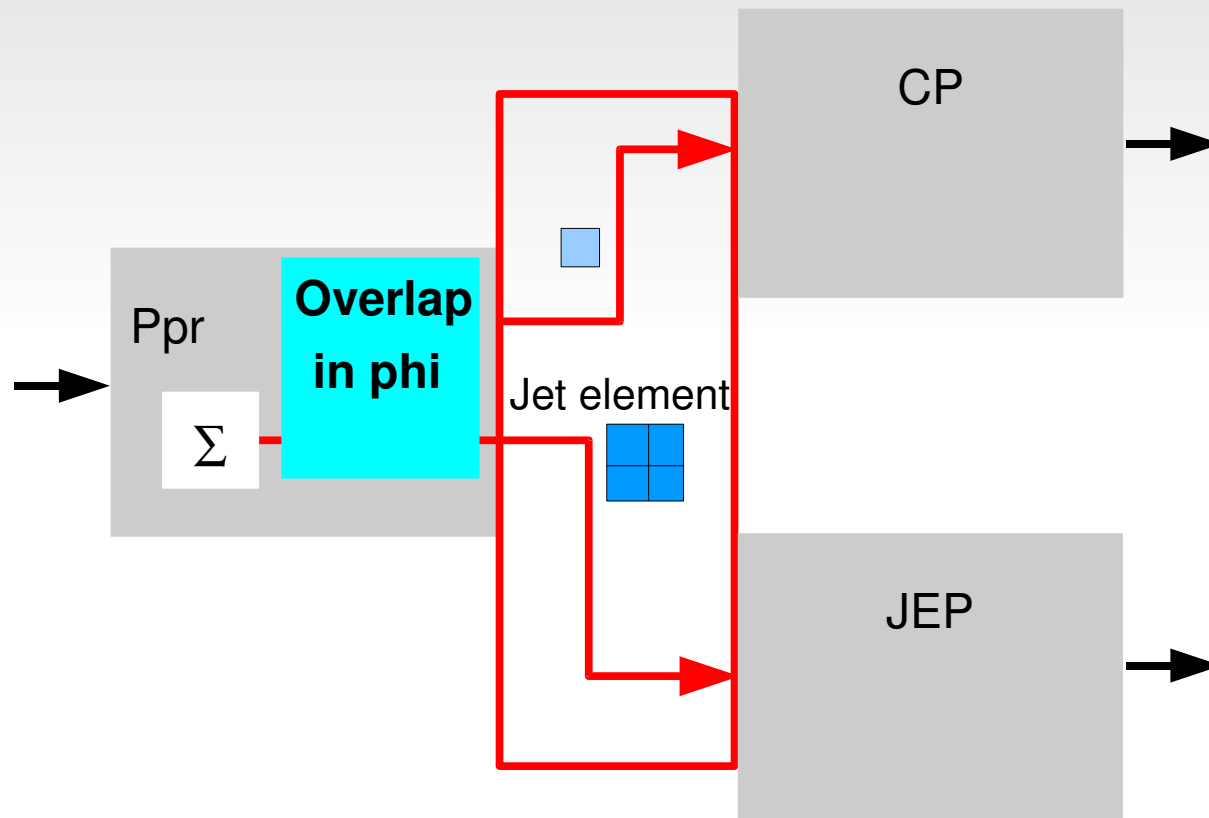
Inter-crate connectivity

- established through serial links (LVDS cables 400 Mb/s)

- transmission of the trigger towers (8-bit digitized transverse energy from PPr to CP) and jet elements (2x2 sums of trigger towers from PPr to JEP)

- timing for all input data is required

Inter-crate connectivity

- Testing of connectivity:
  - firmware integrated status of link
  - firmware integrated parity error counters
  - verifying correct data reception and processing through readout and comparison
  - specific mapping pattern (unique pattern for every channel) checks correct cabling
- This checks on: misconnected cables (very few), hardware problems (cable, source or receiver, backplanes)
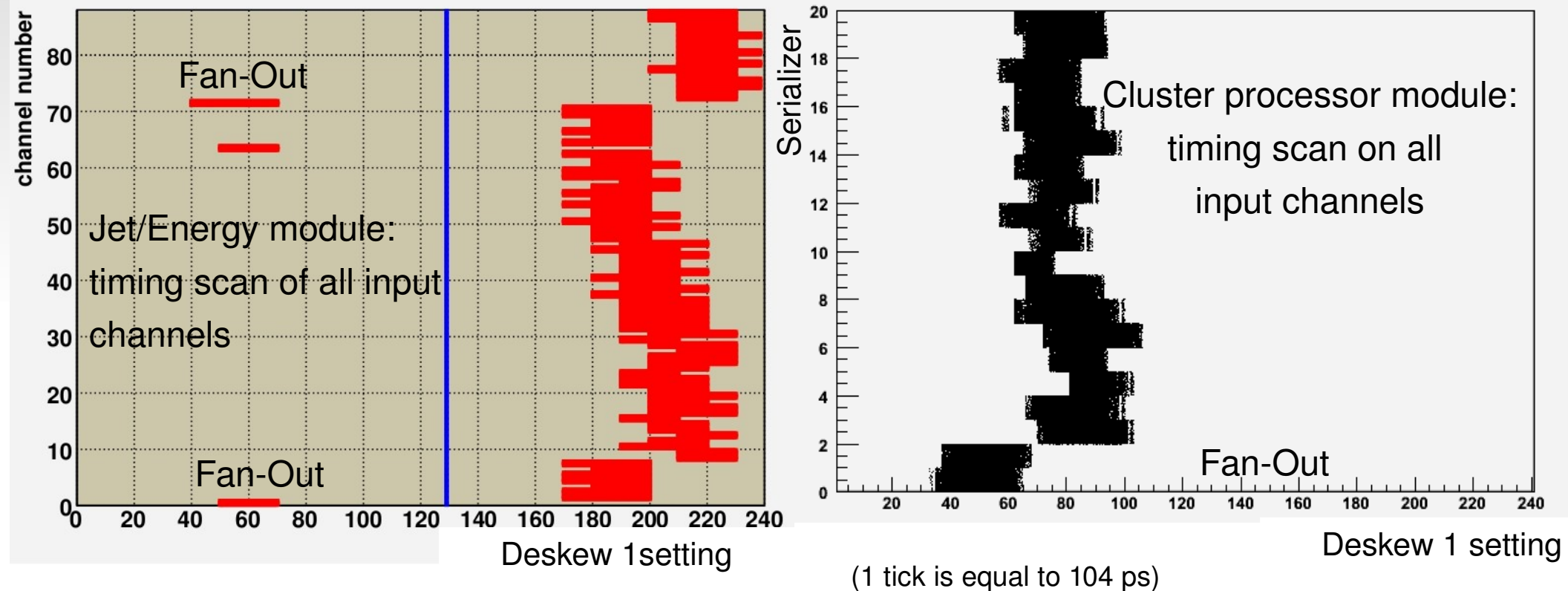
Inter-crate connectivity

- CP and JEP are driven by 2 Deskew clocks derived from the overall bunch clock timing (40.08 MHz): Deskew 1 + 2 (240 steps of 104 ps)

  - Deskew 1: global timing responsible for input timing

  - Deskew 2: time setting for processing shared data in eta for jet, e/γ and tau algorithm

- Adjusting input timing by:

  - 2 phases (through parity errors)

  - delay (analysing synchronous data pattern)
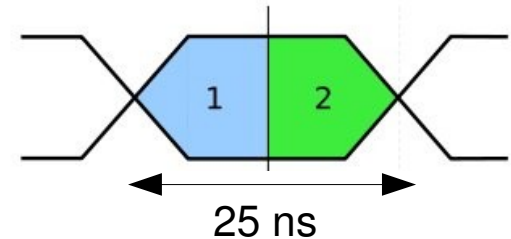
Inter-crate connectivity

Input signal speed 400 Mb/s

→ good time margin 15 out of 25 ns

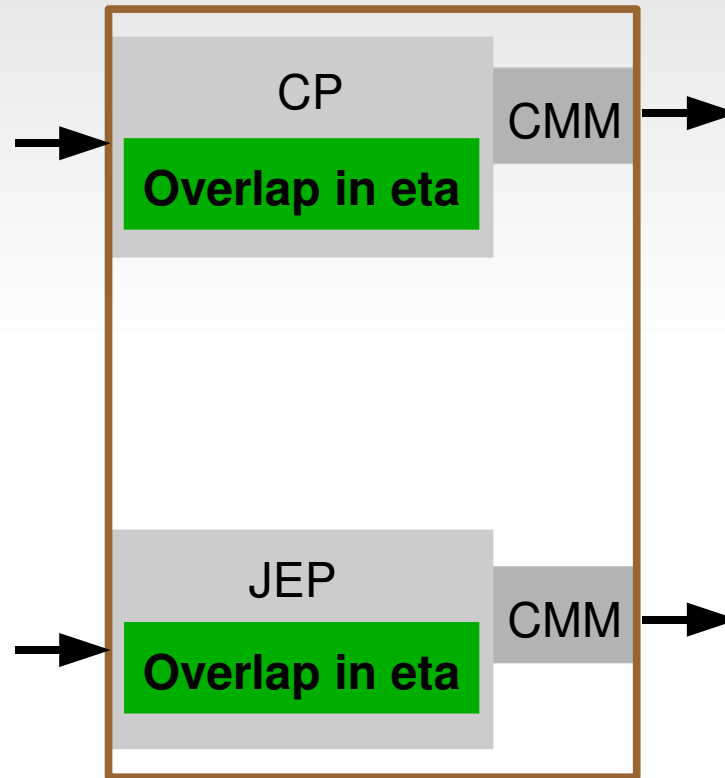- phase with less errors is chosen

- delay aligns all channels

Inter-crate connectivity

- Input calibration needs valid data

- Problems which occurred:

  - link loss and parity errors on processor modules (only a very few)

  - defective source modules (a few)

  - found misconnected cable (about 0.5 %)
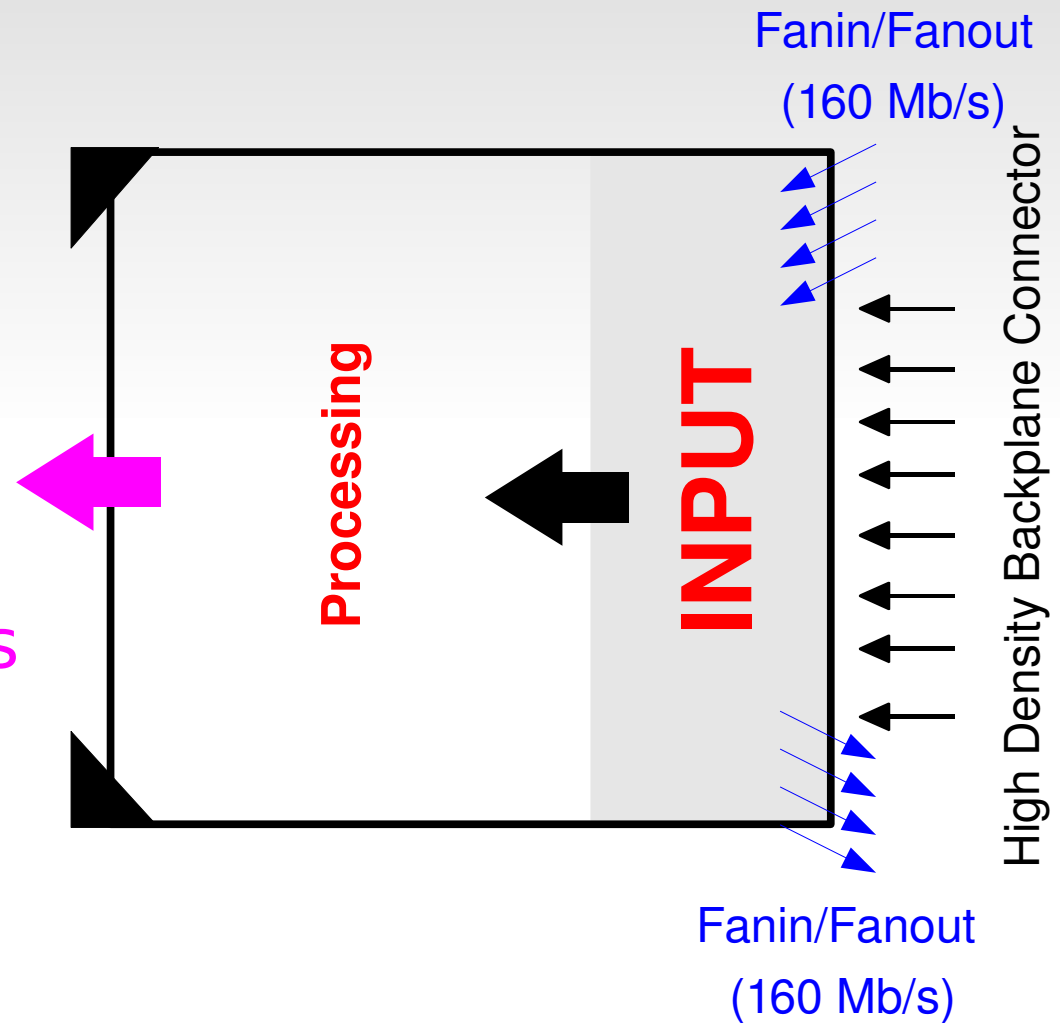
- Problems are all corrected

Inter-module connectivity

Module Design

- many FPGAs for processing data

- connectivity:

  - Backplane input: 400 Mb/s

  - Fanin/Fanout: 160 Mb/s

  - Readout links: 800 Mb/s

- implemented diagnostic memories

Fanin/Fanout (160 Mb/s)

Processing

INPUT

High Density Backplane Connector

Fanin/Fanout (160 Mb/s)

Inter-module connectivity

- Transmission is handled by dense custom

  backplane

- Overlap needs working

  backplane pins

- Every processor needs to be timed in separately

- Each module needs individual time calibration constants (dependent on configuration)
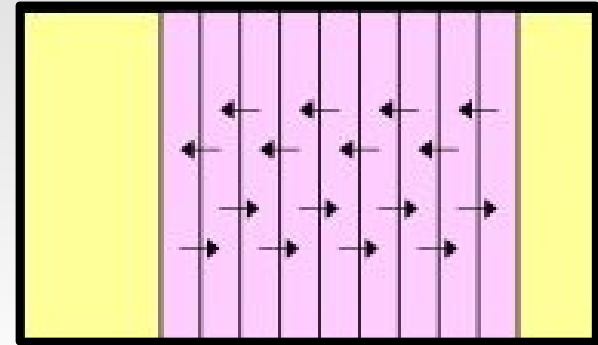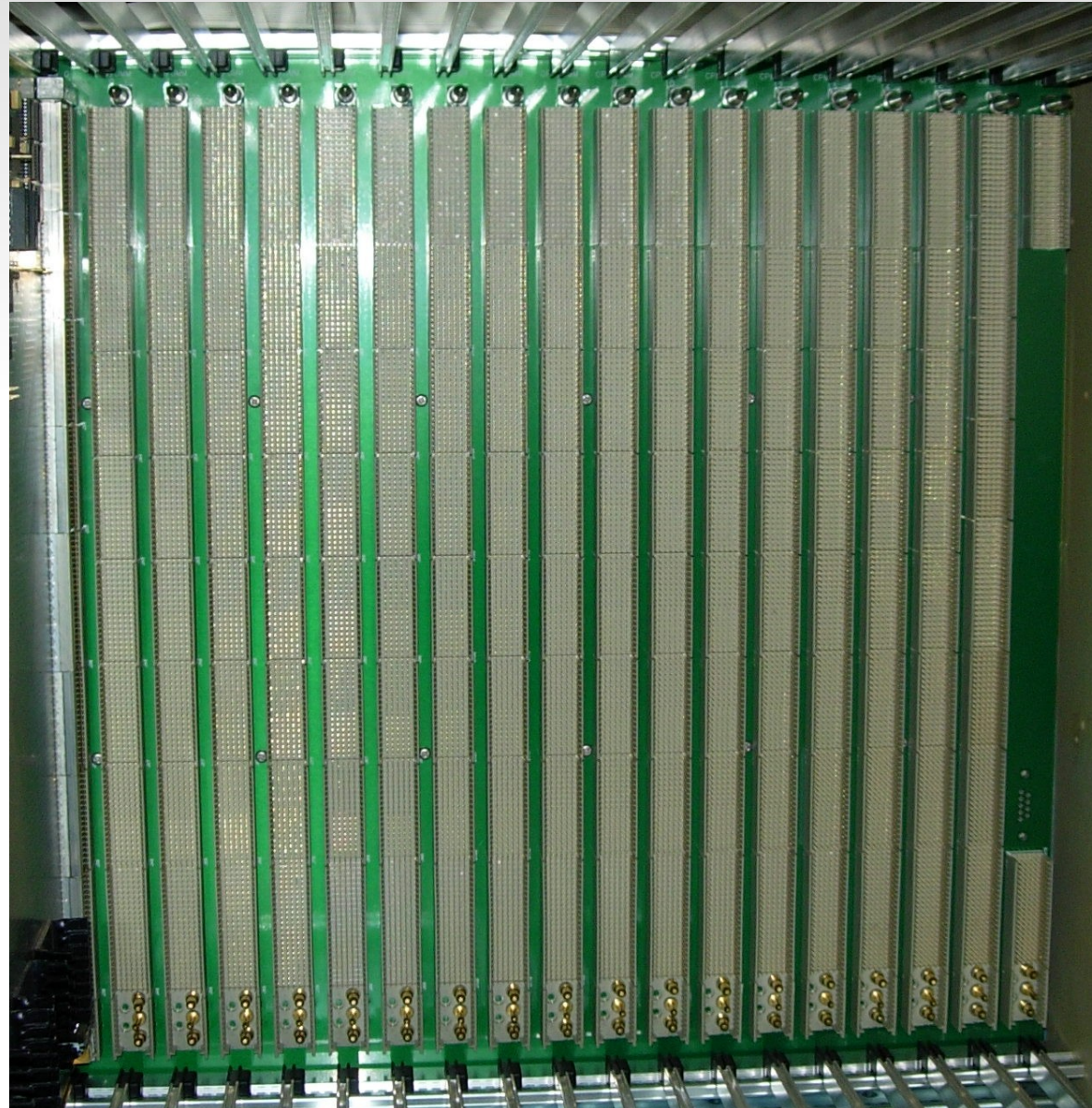
Picture of a CP/JEP backplane

Backplane has 22000 pins:

- 1100 pins per slot:
  - 240 pins input data
  - 330 pins fanin/fanout
  - pins between processor and Merger
  - ground pins for cross talk
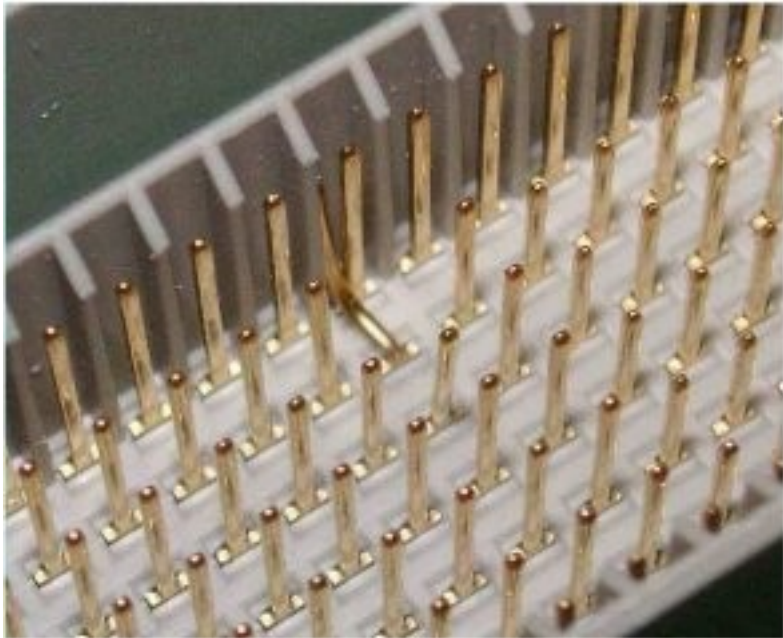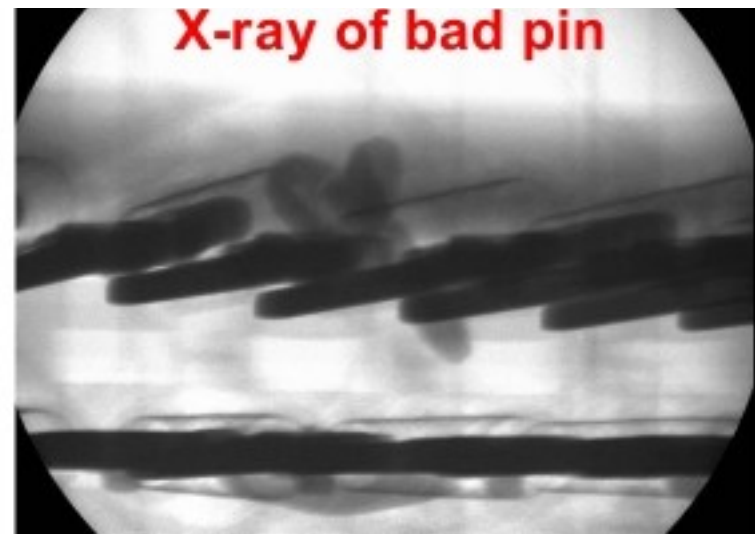 - VMEbus
  - CAN data

Hardware problems

- Backplanes had bent pins after production stage or was damaged during usage
- Every backplane was examined by scanning
- Every problem was corrected last year

(1-2 faults on each backplane)

Bent pin was caused by module insertion

Missing pin: stuck between layers

X-ray of bad pin

Inter-module connectivity

- Calibration procedure to determine Deskew 2 Clock for Fanin/Fanout:
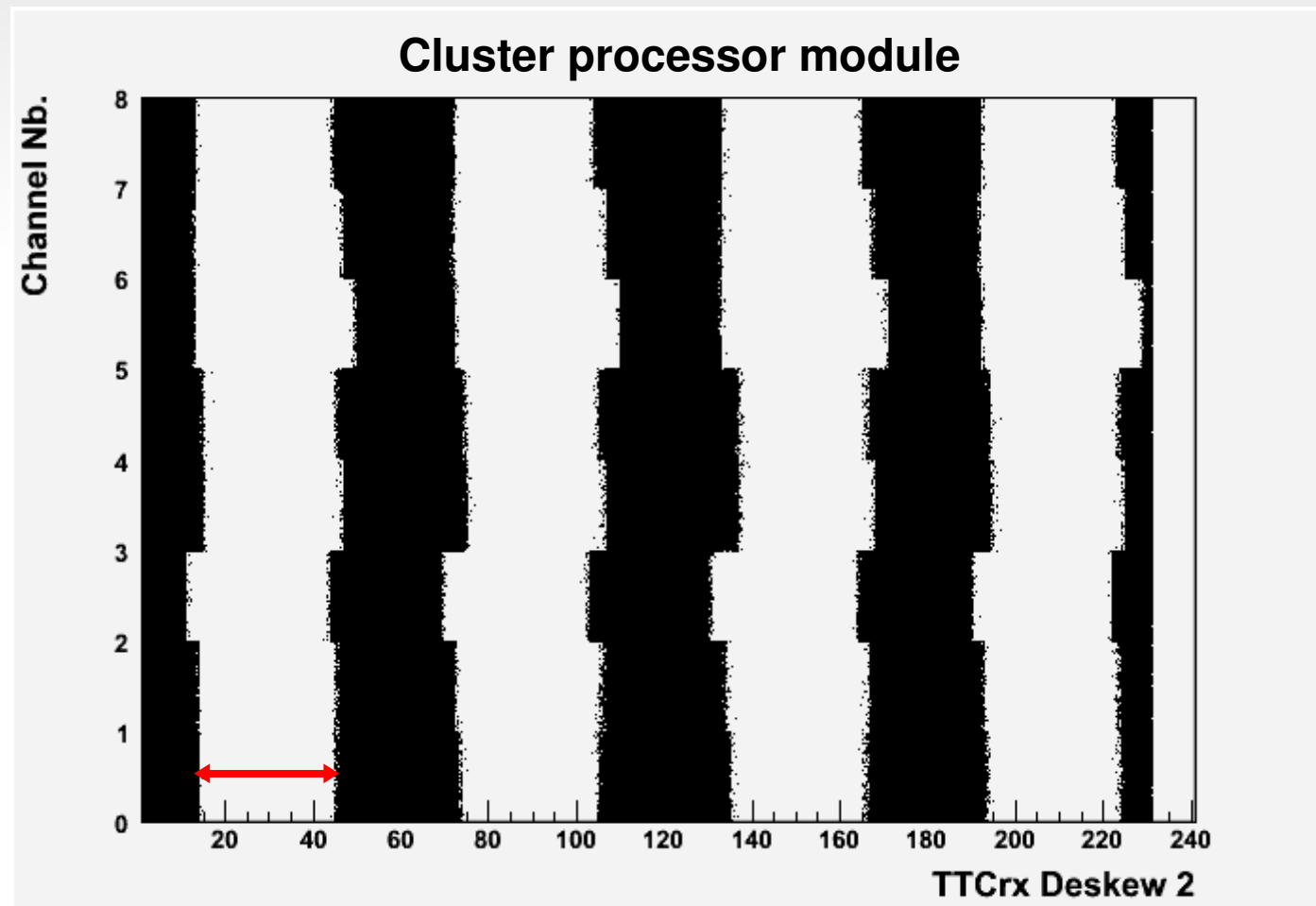
  - On input channels 10-bit counter is enabled

  - Stepping through time settings

  - Parity errors are sampled for each time setting

  - Find valid time setting (5-7 ns)

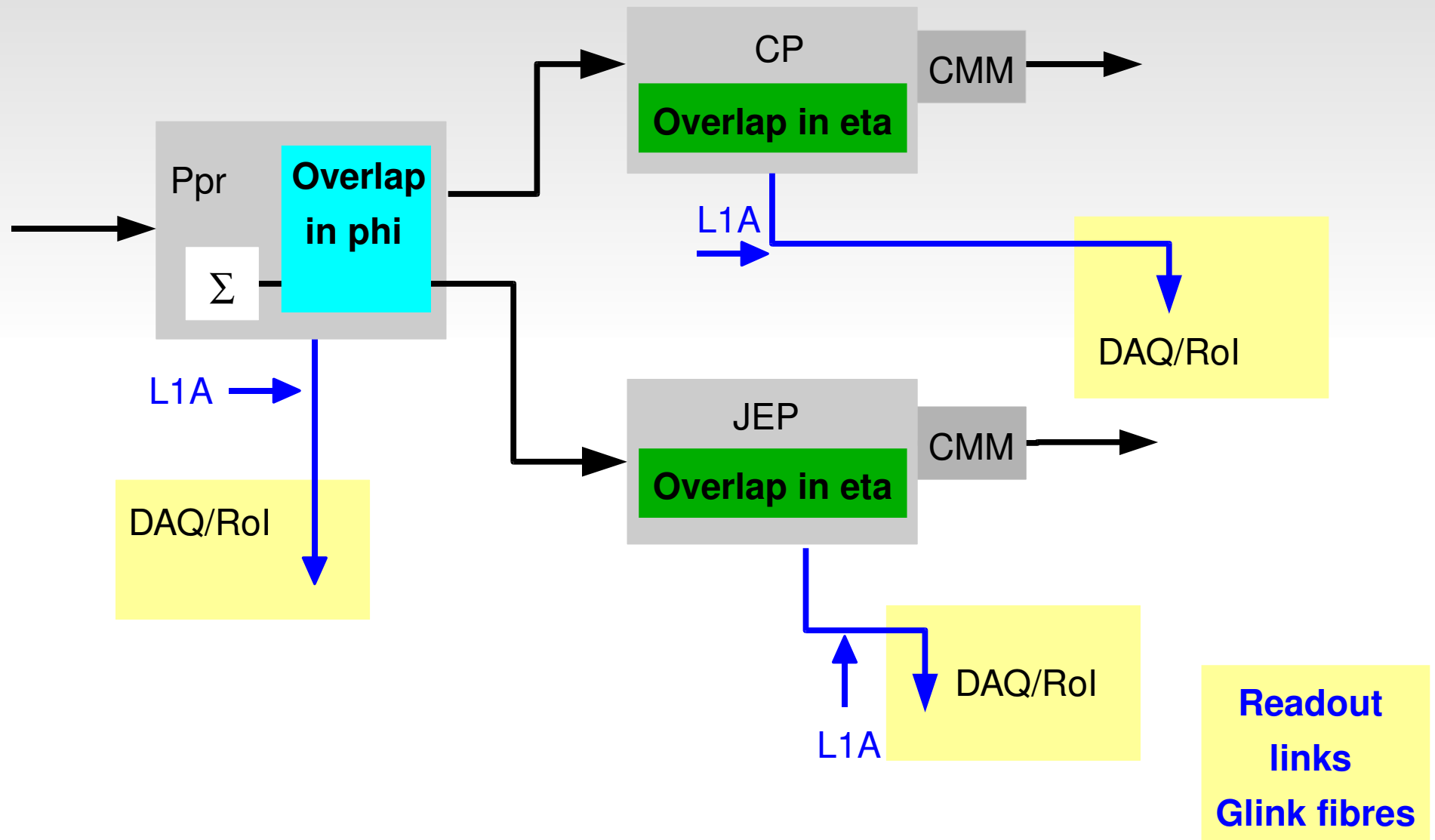JEP system: speed 80 Mb/s

JEM number

Deskew 2 settings

(one tick is 104 ps)
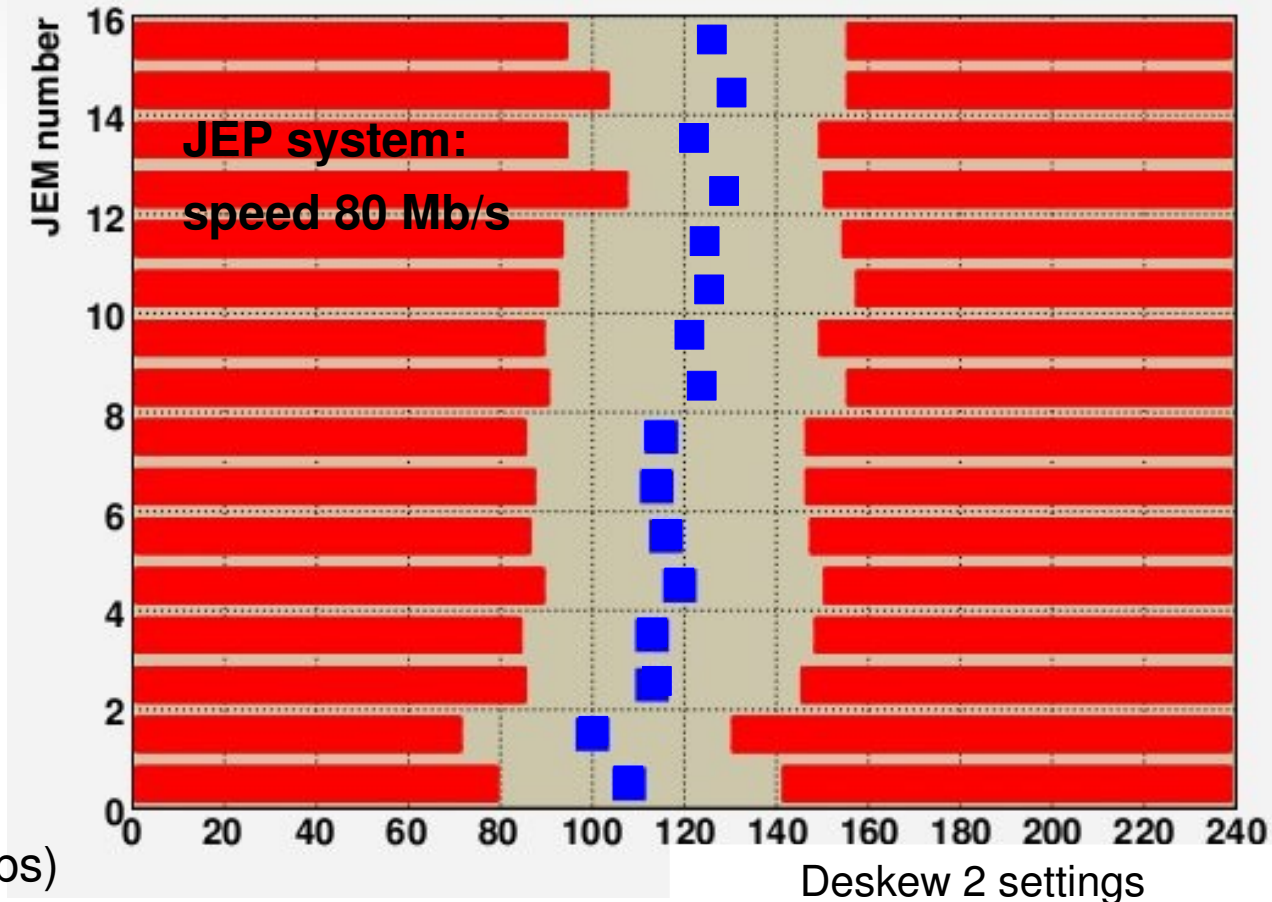
Inter-module connectivity

- Similar timing procedure in the CP system for signal speed of 160 Mb/s

valid data in window of 2-3 ns

Cluster processor module

Channel Nb. / TTCrx Deskew 2

Readout links

Readout links

Data buffer in processor

n bunch crossing deep

Address for one event

time to create a L1A

Readout for DAQ and RoI is initiated
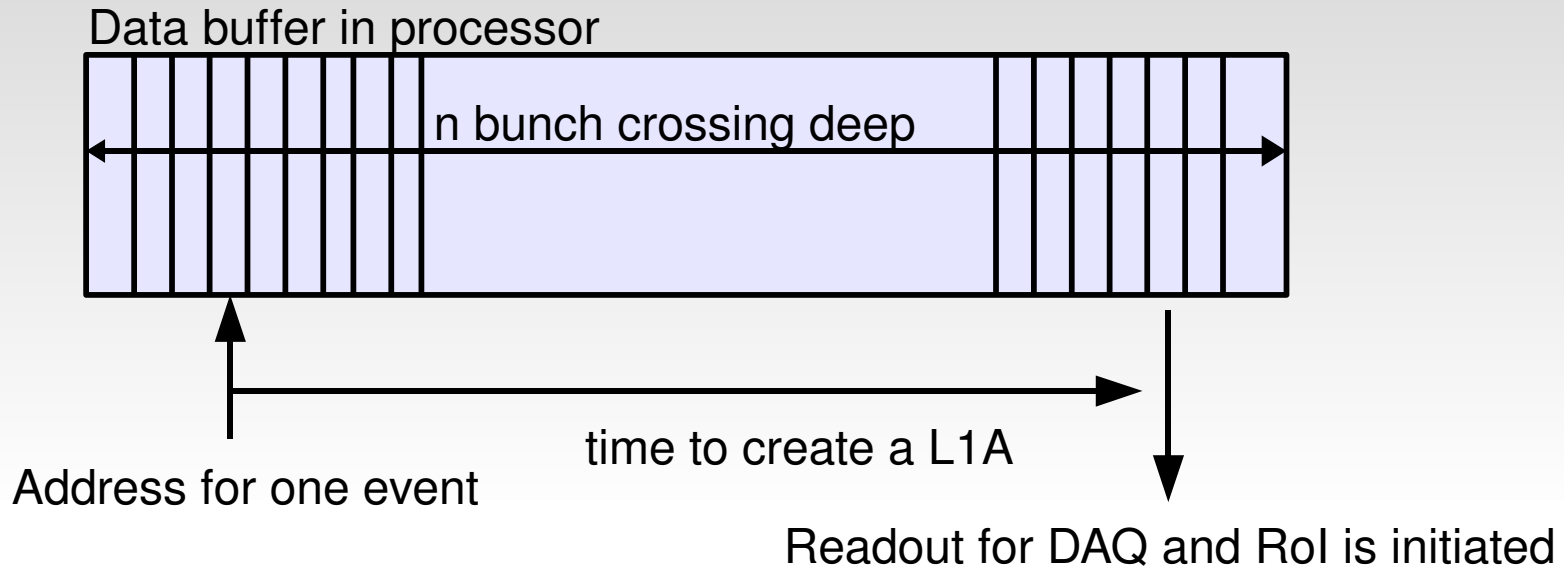
- Need to determine readout pointers to fetch the correct event for each subsystem
- Offline analysis of data and its alignment

Readout links

- Determining the readout pointers with fake L1A rate in standalone testing

- Only one event has data

- 5 subsequent time slices are read out

- Looking at the DAQ and RoI data in the data stream determines the necessary delays

  For example:

Default	0	0	23	0	0
Output	0	23	0	0	0

- Bunch crossing is checked in readout path

Readout tested up to 60 kHz with random triggers and event sychronisation is stable

Conclusions

- Installation finished in December 2007

- Signal integrity is proven:

  - Inter-crate connectivity: cabling and processors have been completely tested

  - Inter-module connectivity: backplane connectivity is fully functional

  - Readout links: readout pointers for the system established

- Every subsystem is calibrated with respect to input data and duplicated data

- System is being prepared for taking first data*

* Further presentations from Rainer Stamen, Damien Prieur and Murrough Landon