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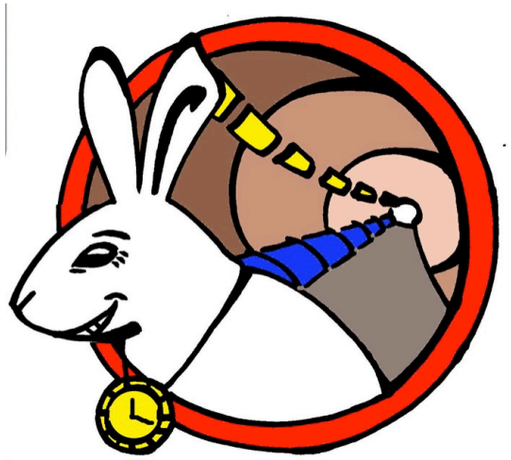

White Rabbit Protocol - Reloaded

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Preemption and it‘s issues

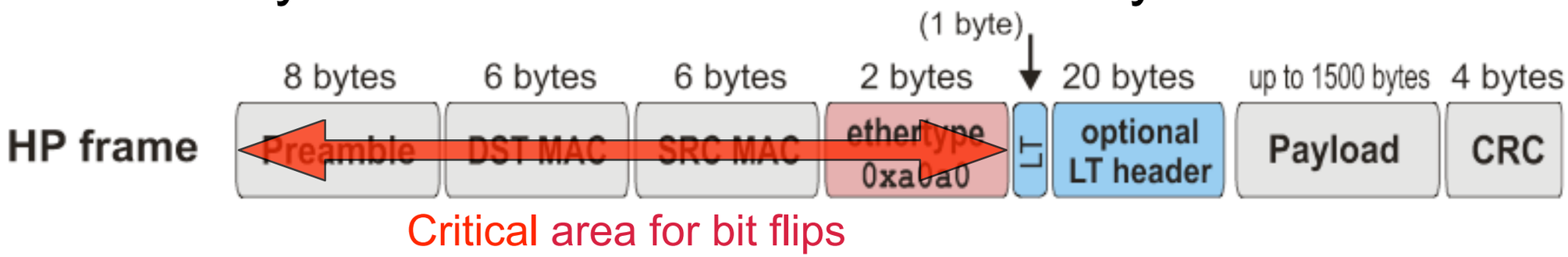
- Is preemption really necessary?
  - WRP specifies a time-triggered approach, so why not just allow non-RT traffic in a special slot (like POWERlink)?
  - If we need event-triggered messages, why not just discard the frame and retransmit later?
    - discarding introduces max. 160 ns (min. 100 ns) delay per level and has to ensure incorrect FCS at frame end
- Current problems
  - How do we reassemble segments, if they are not linked to each other (loss, wrong sequence, etc.)?
  - Reassembling needs a lot of other measures to be safe and efficient. Normally done at layer 3 (see IP!)
  - TCP flow control relies on lost packets ...

High Priority Frames (HP)

- How often will they be sent?
  - Time- or event-triggered, both
  - Equally spaced over one cycle, or collected?
    - Collect on layer 3?
  - Broadcast only or Multicast
    - Multicast would allow subscribing and without large overhead
  - What about HP collision on upstream?
- Introduce traffic classes
  - like TTE?
    - Time-triggered – highest priority, predefined and guaranteed delay
    - Rate-constraint – predefined bandwidth, delays have defined limits
    - Best-effort – lowest priority, uses the remaining bandwidth
  - Event-Triggered, Time-Triggered, Best-Effort?

Ensuring delivery of HP frames

- XOR only of data does not ensure delivery!



- Insert FEC before CRC that covers the whole frame
  - must be checked and corrected in each switch (HP end nodes)
  - Smaller MTU to keep FEC in the same frame
  - Transparent for non-WRP nodes, can be done in SW as well, if frames with wrong CRC are accepted by HW

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Other Protocol Standards

- What about upstream traffic?
  - Is RT communication between slaves really out of scope?
  - Organized by master or best effort?
- Master redundancy
  - Why exactly two and not a group of masters?
  - Switching or democratic algorithm

Thanks for your attention and ...

... I hope, I could trigger a benefical discussion!

Please send suggestions, ideas, and explainations to
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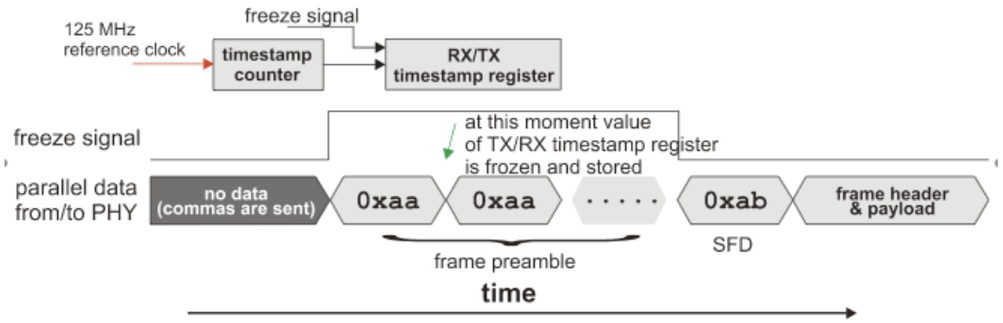
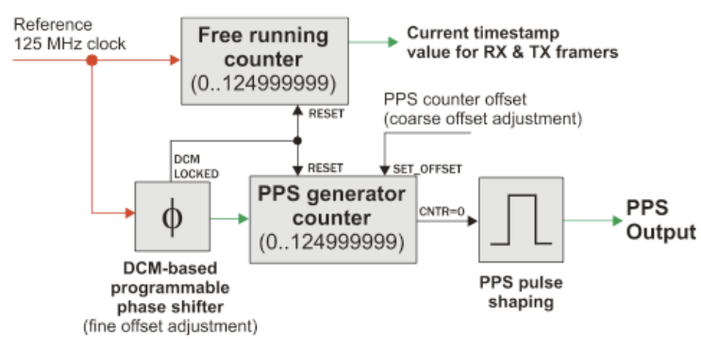
System Issues

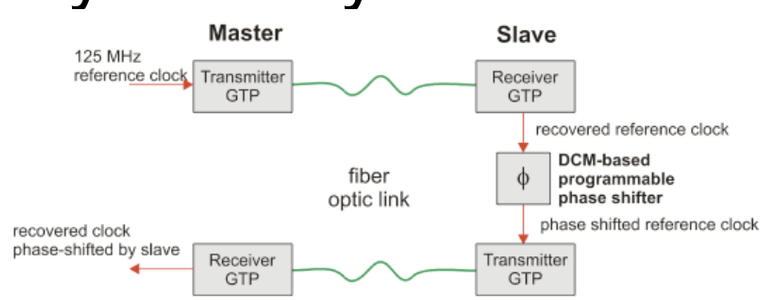
- Time stamping (fig.2) doesn‘t satisfy IEEE 1588 standard



- Setup-time violation in „Timestamp source / PPS generator“ (fig. 3), free running counter has to run with double the frequency in oder to keep setup-time for second clock domain



- Fig. 5 gives actually link asymmetrie instead of fine delay ...



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System Issues (cont.)

- What about the phase shift within the switch between RX downstream port (from node) and TX upstream port (to master)?
- Asymmetry has to be lower than half of the clock period
- How does the comma alignment work and what is the result?