xTCA projects (HW and SW) related to ATLAS LAr

xTCA interest group - CERN

07/03/2011

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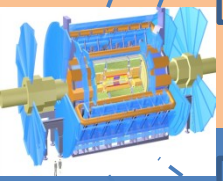
ATLAS LAr Context



Today

Calibration

FRONT END ELECTRONIC

Analog Pipeline (SCA)

ADC 5MHz 16x12-bits

Σ

128 cells/FEB

FEB

x1600

L1 Trigger

100kHz max

1

Optical Link 1.6 Gbit/s

BACK END ELECTRONIC

ROD

800 Optical Links

ROS

x192

$E = \sum a_i (S_i - PED)$

$E\tau = \sum b_i (S_i - PED)$

$\chi^2 = \sum (S_i - PED - E g_i)^2$

8 ROD/FEB

Upgrade

Calibration

FRONT END ELECTRONIC

ADC 40MHz 128x18-bits

Mux / Serializer

128 cells/FEB

FEB

x1600

Optical Link 100 Gbit/s

BACK END ELECTRONIC

ROD

?? Optical Links

ROS

$E = \sum a_i (S_i - PED)$

$E\tau = \sum b_i (S_i - PED)$

$\chi^2 = \sum (S_i - PED - E g_i)^2$

14 ROD/FEB ?

L1 Trigger

> 100kHz

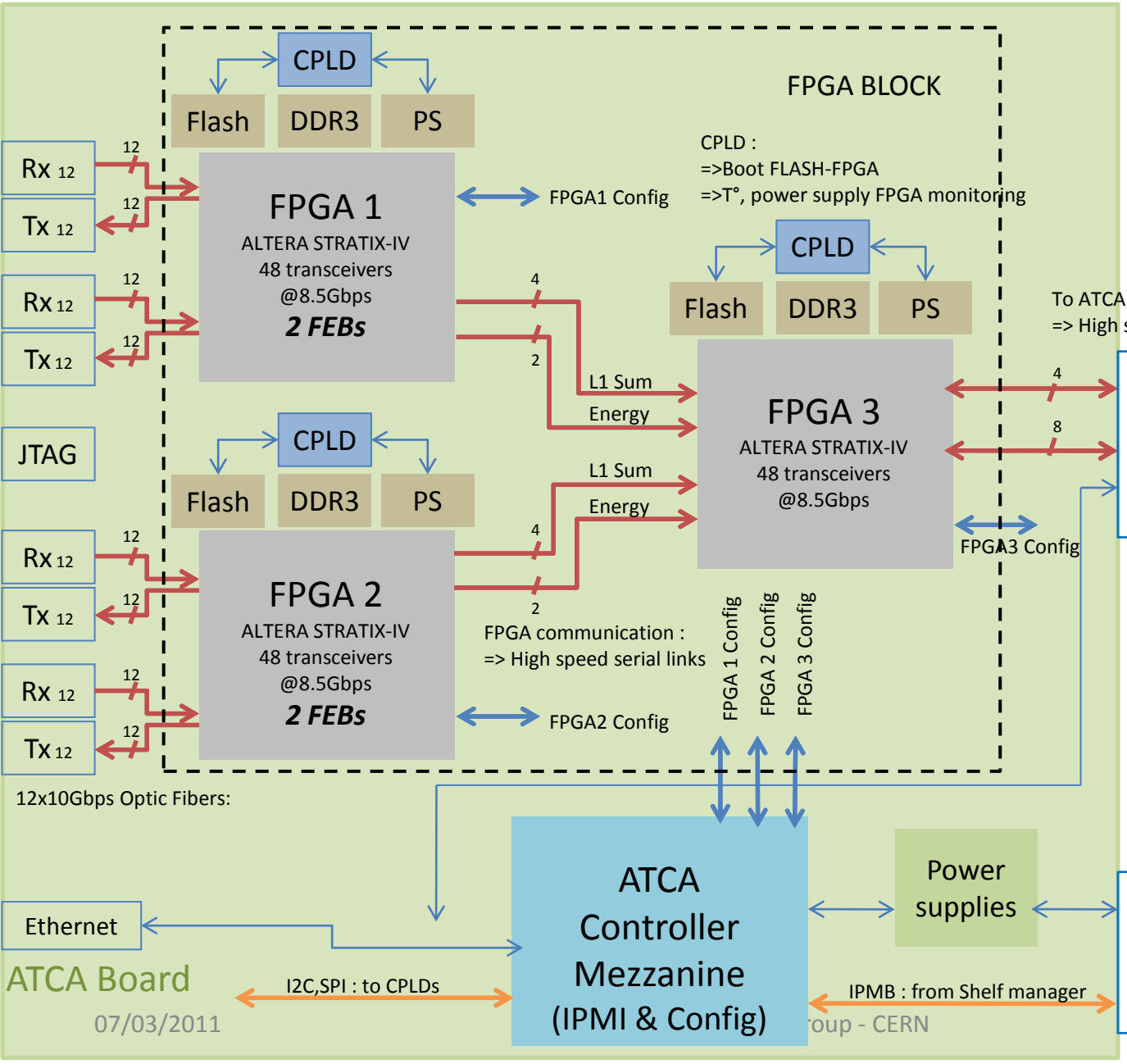
BNL & Univ. of Arizona contribution

- BNL
  - Readout Driver Board in ATCA plateform
    - Receive 12x6.25Gbps parallel optical link
    - Process data in a Xilinx Virtex 5 FXT FPGA
  - Design of a Readout Driver Processing Unit in AMC plateform
    - Receive four 12x10Gbps parallel optical links (from Avago receiver)
    - Process data in a Xilinx FPGA
- University of Arizona
  - Readout Driver Injector in ATCA plateform
    - Transmit data through 12x6.25Gbps parallel optical link
    - Based on a Altera Stratix IIGx FPGA
  - Developpement of an AMC PU Injector
    - Transmit data through four 12x6.5Gbps parallel optical link (from ReflexPhotonics)
    - Based on Altera FPGA

LAPP contribution

- ROD Evaluator
  - ATCA Board size
  - High speed and high density links to read data from FEB
  - High processing power
- ATCA Test Board
  - ATCA Board size
  - Validate ATCA IPM Controller with the ATCA Controller Mezzanine
  - Validate ATCA Board management with the ATCA Controller Mezzanine
  - Validate ROD Evaluator parts (Power Supplies, DDR3 interface, DSP computing in FPGA)
- ATCA Controller Mezzanine
  - FMC (FPGA Mezzanine Card) format
  - ATCA IPM Controller
  - User defined ATCA Board management (board configuration etc..)

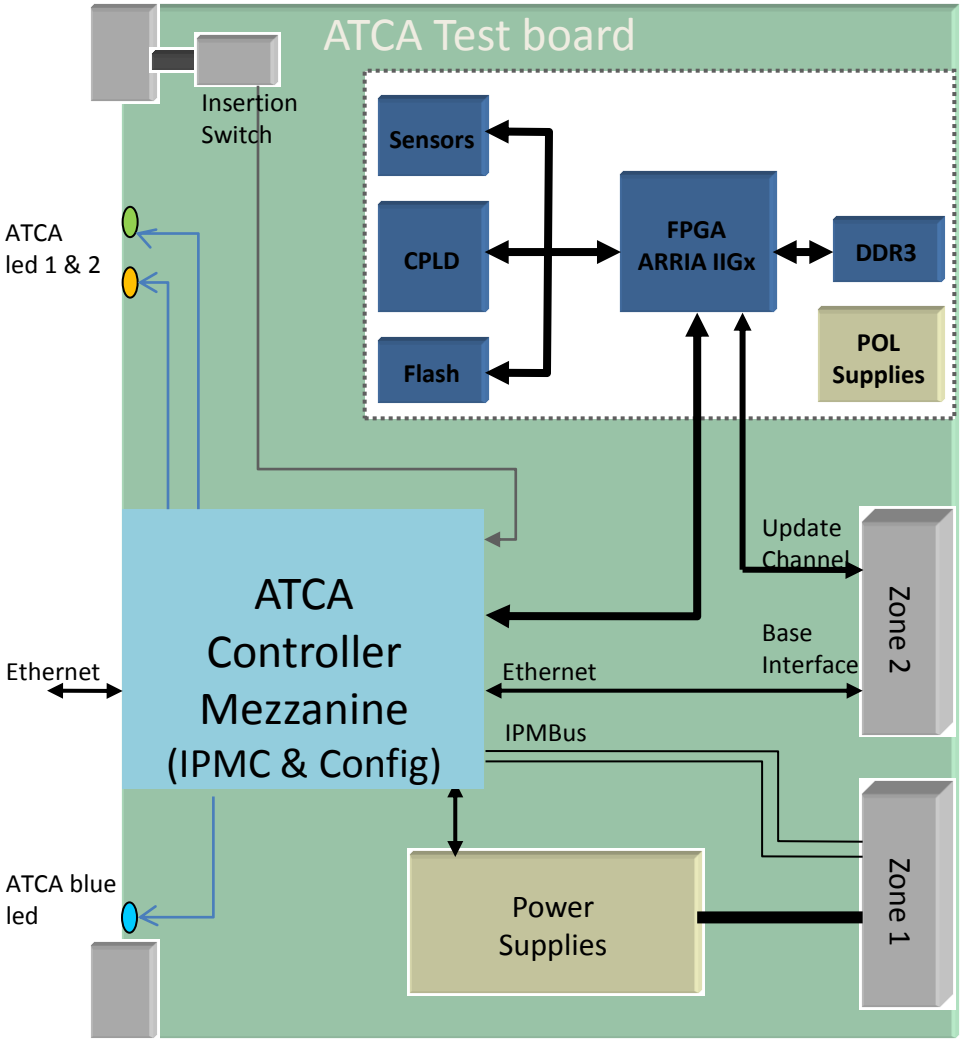
ROD Evaluator



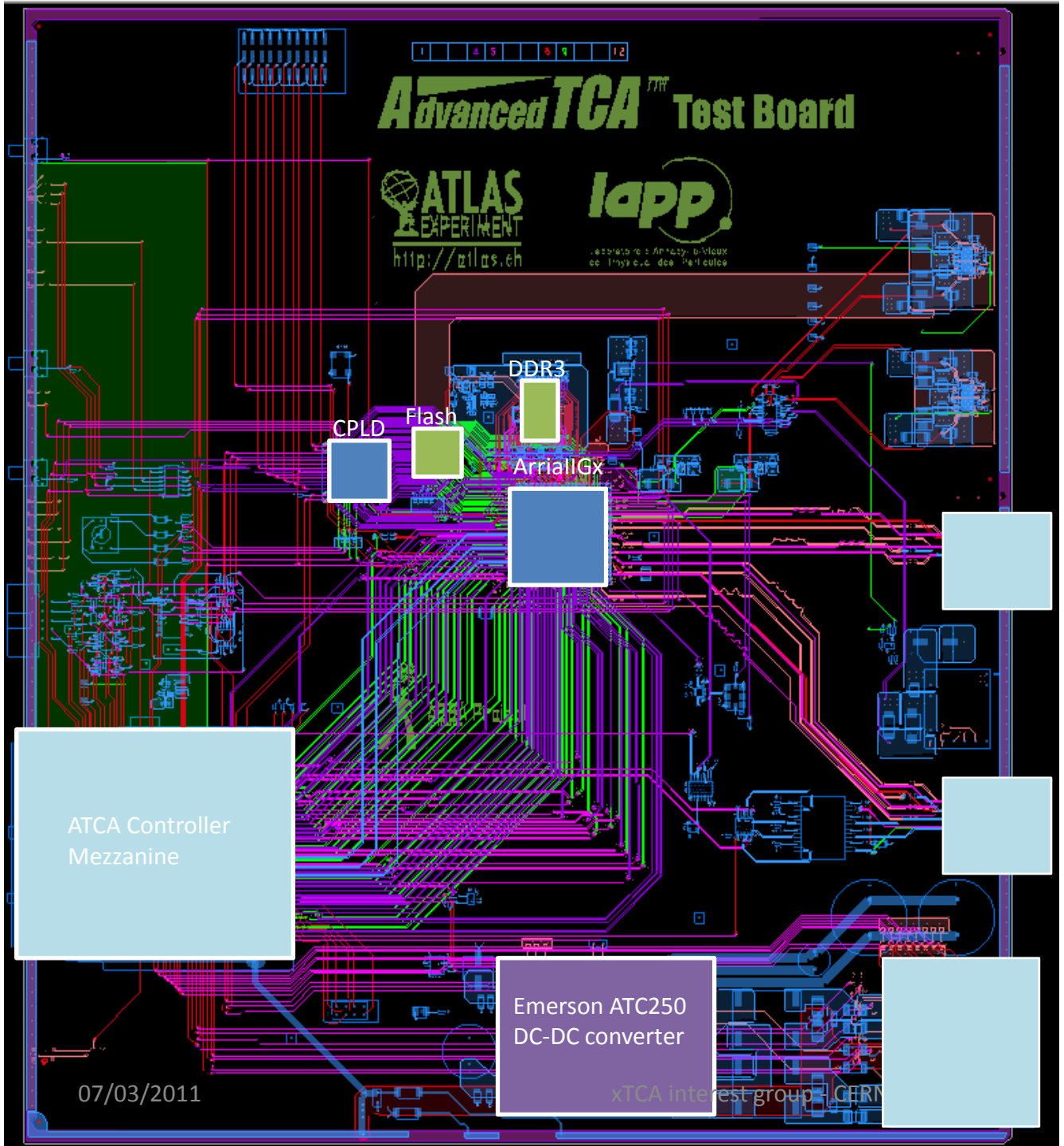
- 48 optical Rx links @8.5Gbit/s
- 48 optical RTx links @8.5Gbit/s
- High DSP computation BW for Energies and L1 Trigger computation

- Links to ATCA backplane (to send data to a ROS?)
- ATCA Controller Mezzanine to configure and manage the board

ATCA Test Board



- **ROD demonstrator tests**
  - Check Board configuration with the ATCA Controller Mezzanine (Firmware upgrade, Configuration upload etc..)
  - Test ATCA compliant power supplies
  - Check FPGA Design (communications with DDR3, Flash, configuration with Flash)
- **ATCA Controller Mezzanine tests**
  - IO connections (JTAG boundary scan tests)
  - IPMI management with the Shelf manager
  - Ethernet communication through ATCA Base Interface



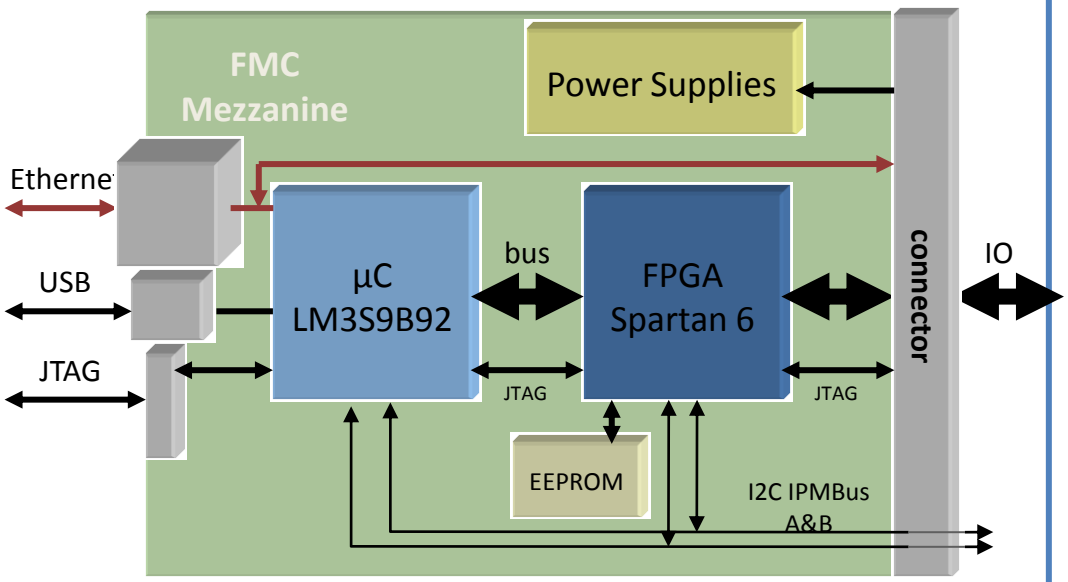
- PCB already ordered
- The board will be available end of March

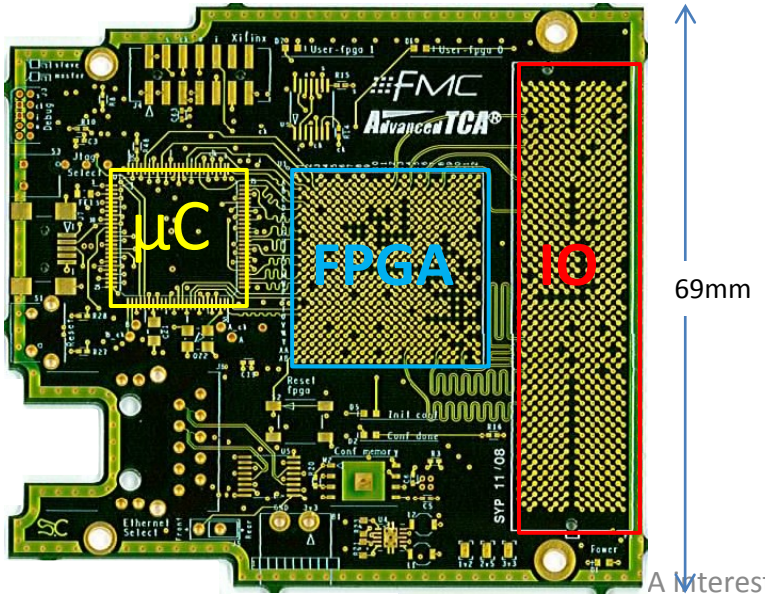
J2
Update Channel

J2
Fabric Interface
Base Interface

J1
Power &
IPMBus

ATCA Controller Mezzanine





- **IPM Controller**
  - Communication with Shelf manager through IPMBus A & B
  - Hot Swap, Power management etc..
- **ATCA board management**
  - Communication via Ethernet (front panel or ATCA Base Interface)
  - User functions
    - Firmware Upgrade
    - ATCA board monitoring & configuration
    - Users stuffs….
- FMC (FPGA Mezzanine Card) compliant
  - up to 160 customizable links(including 74 differential links)
  - Low cost
- Features:
  - ARM cortex M3 processor
  - Xilinx Spartan 6 for highly configurable user IO
  - Ethernet / USB / JTAG interfaces

=> We will receive the board this week

Tests with commercial board

- Hardware setup (Adlink 6900 + Vadatech AM210):

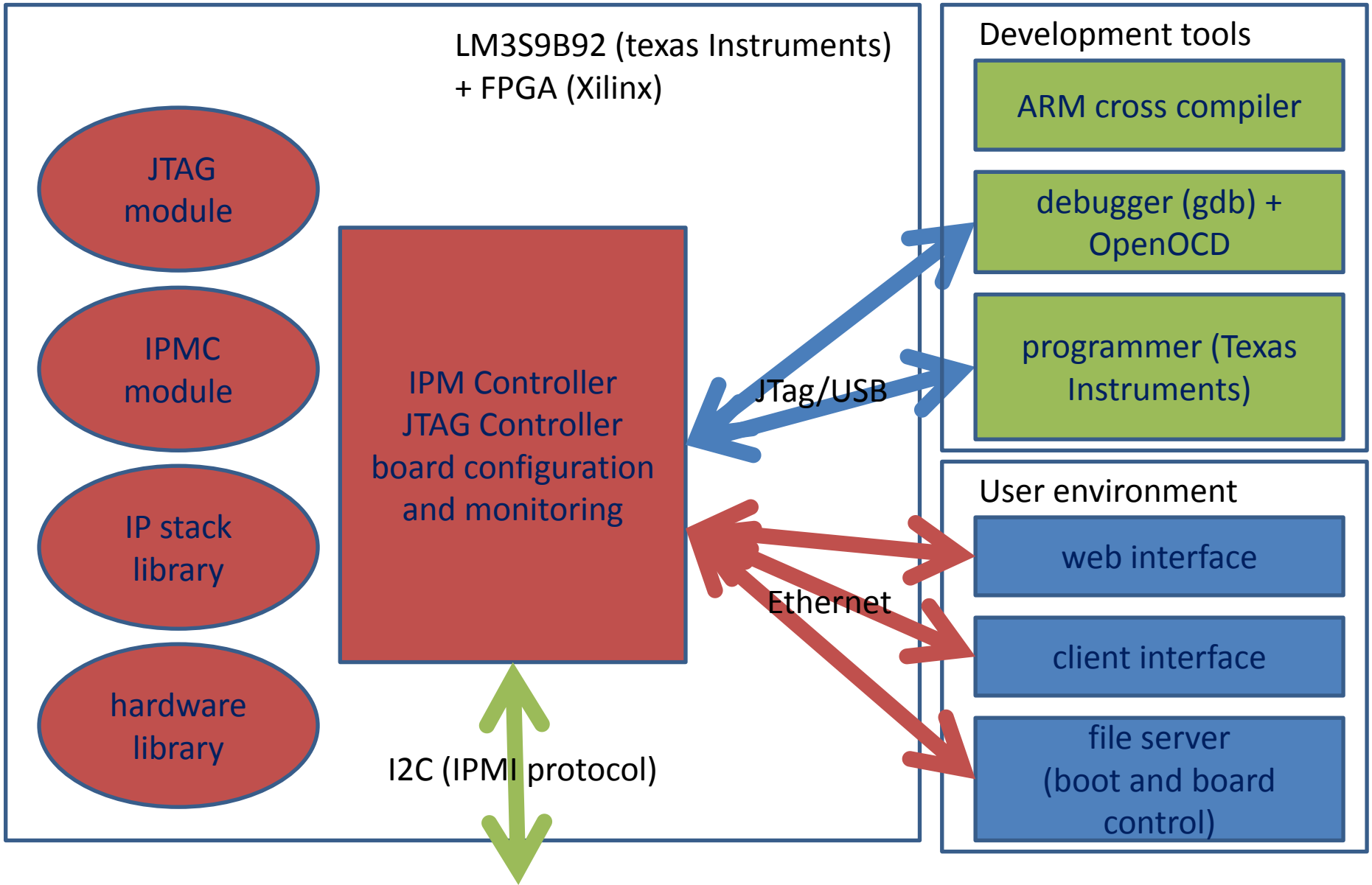
  OS: Scientific Linux CERN SLC release 5.4 (Boron) 64bits
  KERNEL: 2.6.18-194.3.1
  CPU: Intel Xeon L5408 (Quad Core)
  NETWORK BENCHMARKING TOOL: netperf version 2.4.5

- Communication 10GbE between two blades
  - Front (i.e. via AMC) : **done**
    - **TCP=5.4 Gb/s (message 1 GB)**
    - **UDP=5.6 Gb/s (message 64 KB)**
  - Zone 3 (RTM) : to be done...
  - Zone 2 (fabric interface): **done**
    - **TCP=8 Gb/s (message 1GB)**
    - **UDP=6.8 Gb/s (message 64 KB)**
- Lossless data compression algorithms: to be done

ATCA Controller Mezzanine Software

- Specification compliant
  - PICMG 3.0 R3.0 – AdvancedTCA base specification
  - IPMI v1.5 and relevant subset of IPMI v2.0
- control of the board :
  - program the FPGAs
  - monitor of the working conditions
  - remotely driven

ATCA Controller Mezzanine Software



ATCA Controller Mezzanine Software

- Development tools (operational)
  - OS : Linux
  - Compiler GNU GCC for ARM Cortex-M3
  - Specific drivers (TI Luminary LM3S9B92)
  - Debugger GNU GDB + OpenOCD
- IPM (**I**ntelligent **P**latform **M**anagement) Controller software
  - Implementation of IPMI 2.0 specification
    - Library ported and hardware dependent interface written and compiled
    - Test foreseen as soon as we have the hardware

ATCA Controller Mezzanine Software

- JTAG control
  - allows for initial programming of the FPGAs on main board
  - xsvf interpreter tested in simulation
  - JTAG connector on front of the board allows for control of the whole JTAG chain or for microcontroller debugging
  - the JTAG chain can be controlled either by the microcontroller or by an external device
- Board control and monitoring (via Ethernet interface) (in development)
  - FPGA firmware upgrade
  - Board configuration (e.g. coefficient for physics algorithms)
  - Board monitoring (temperature, voltage …)