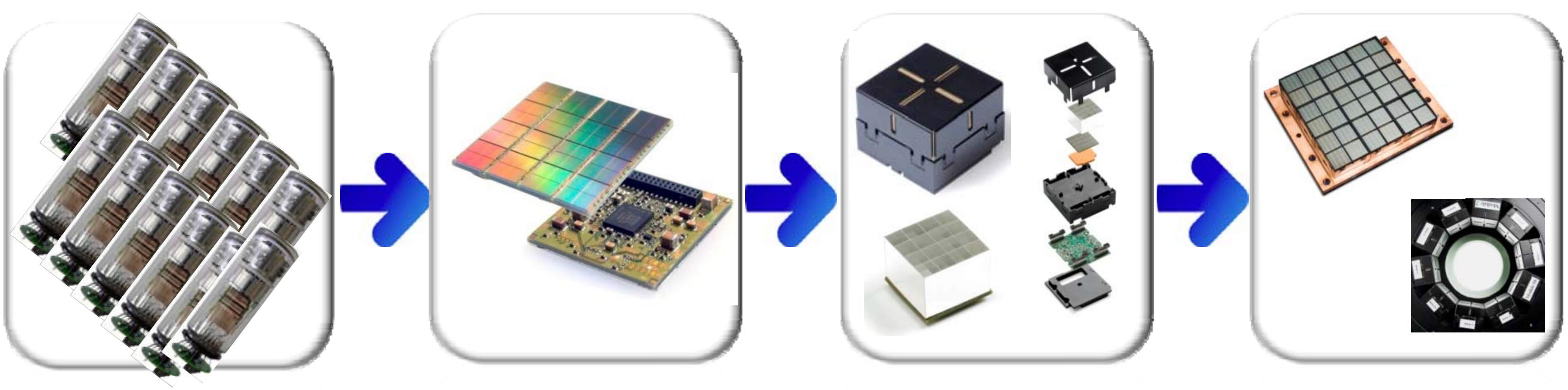
PHILIPS

Digital Photon Counting (DPC) Technology – lateral integration of SPAD & CMOS providing high timing performance and scalability

York Haemisch

Philips Digital Photon Counting, Aachen, Germany



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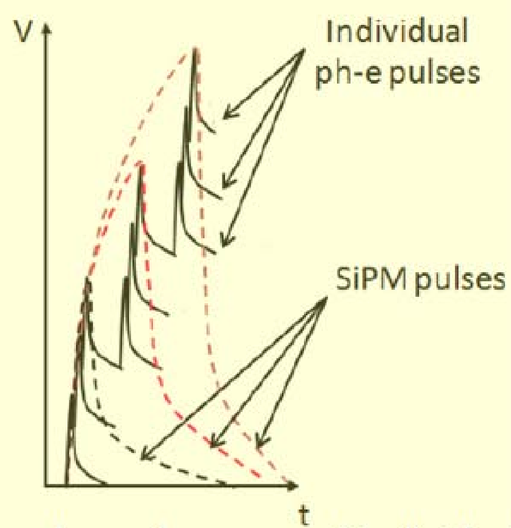
OUTLINE

- SiPM: analog vs. digital
- Digital implementation and layout
- Intrinsic advantages of DPC technology
- DPC technology systems concept
- Application examples PET & FARICH
- Summary/Outlook

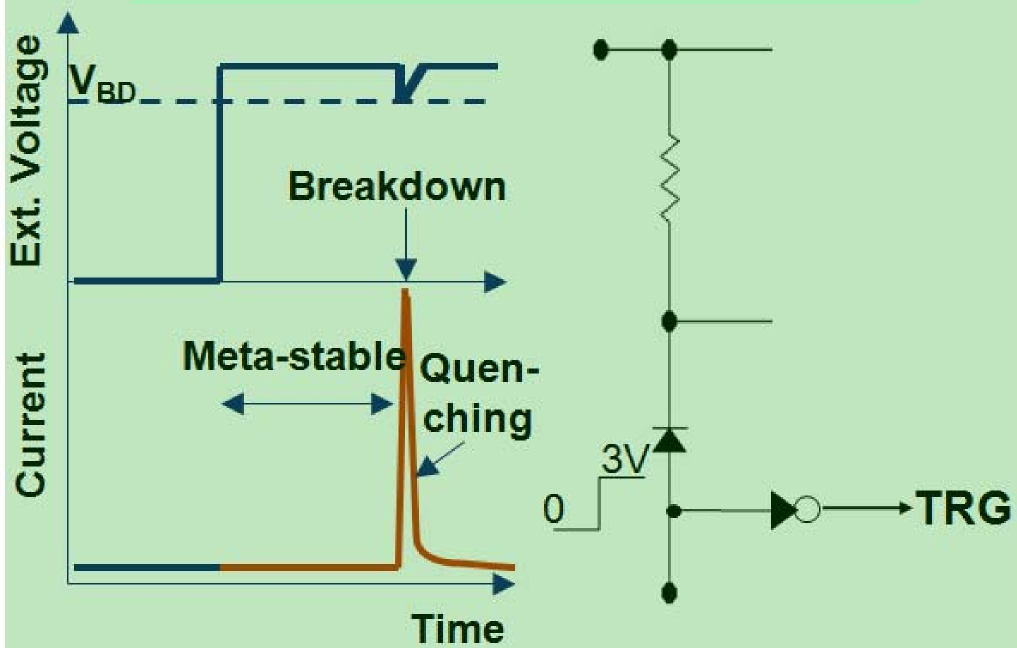
DPC Takes Advantage of the Binary Nature of the Geiger-Mode APD

Analog SiPM



- Signal: analog sum of individual pulse amplitudes
- amplitudes depend on gain
- gains depend on temperature
- temperature drifts: 2-8%/K

Digital Photon Counter (DPC)

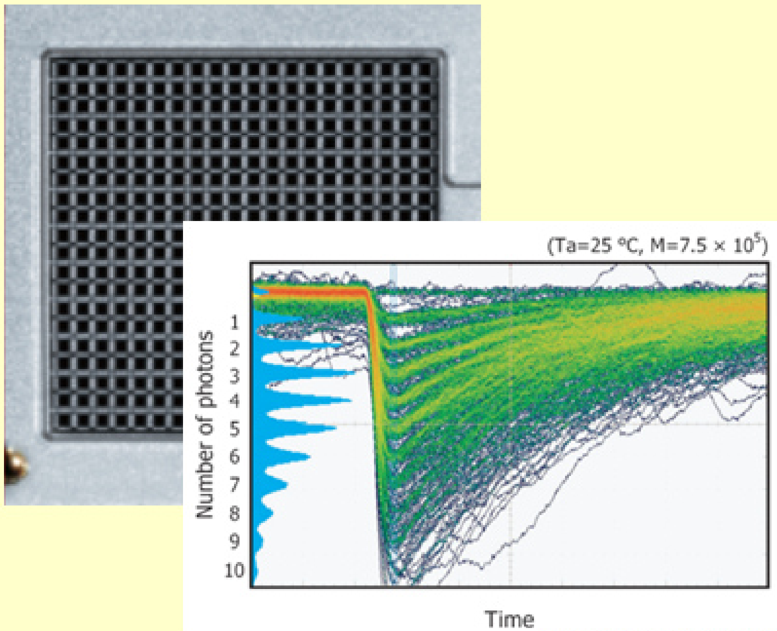


- Signal: digital sum of trigger bins & digital time stamp from TDC
- amplitudes are not relevant
- no gain dependency, reduced temp. drift: 0.33%/K

"Therefore, while the APD is a linear amplifier for the input optical signal with limited gain, the SPAD is a trigger device so the gain concept is meaningless."
(source: Wikipedia)

DPC: Front-end Digitization by Integration of SPAD & CMOS Electronics

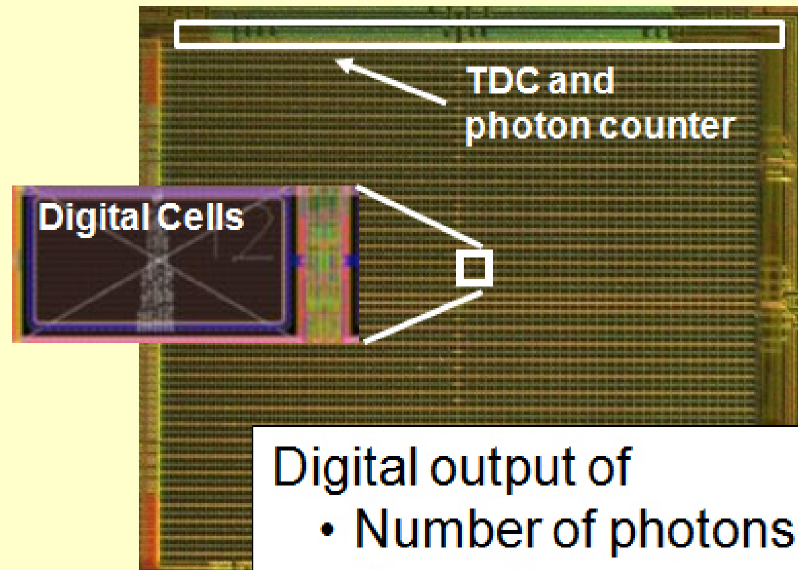
analog SiPM



www.hamamatsu.com

Summing all cell outputs leads to an analog output signal and limited performance

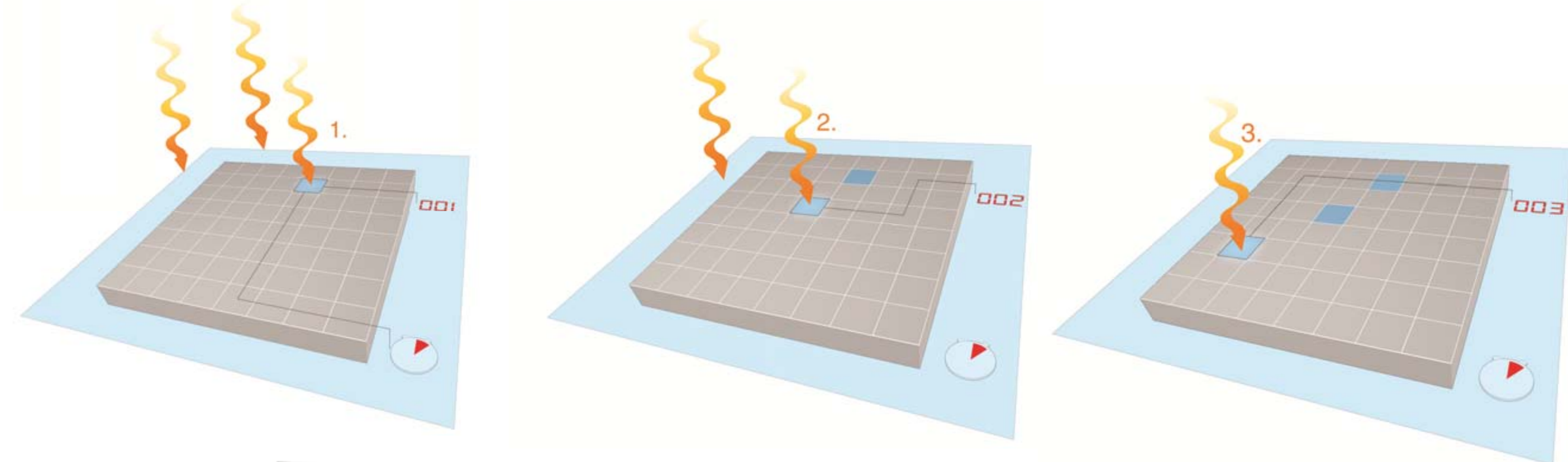
Digital Photon Counter (DPC)

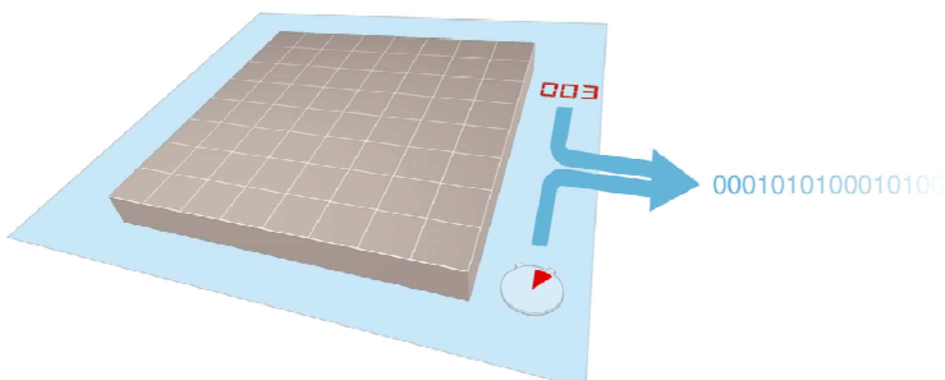


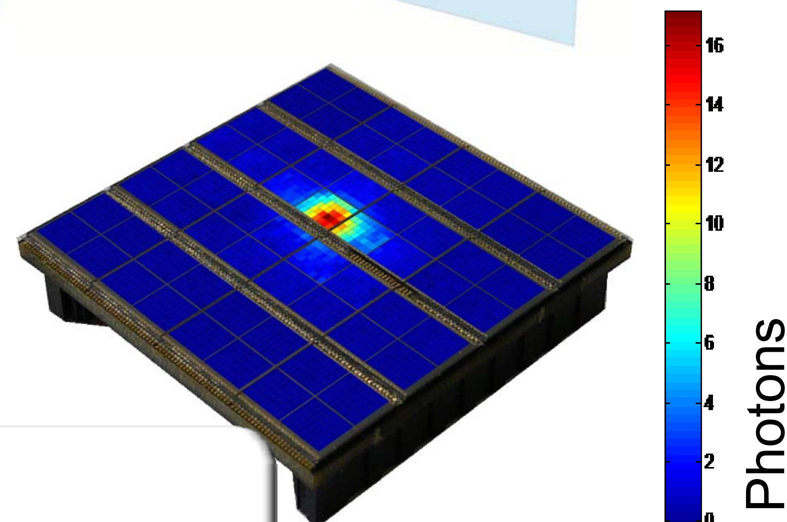
Digital output of
- Number of photons
- Time-stamp

Integrated readout electronics is the key element to superior detector performance

DPC: Now Photons are Counted Directly



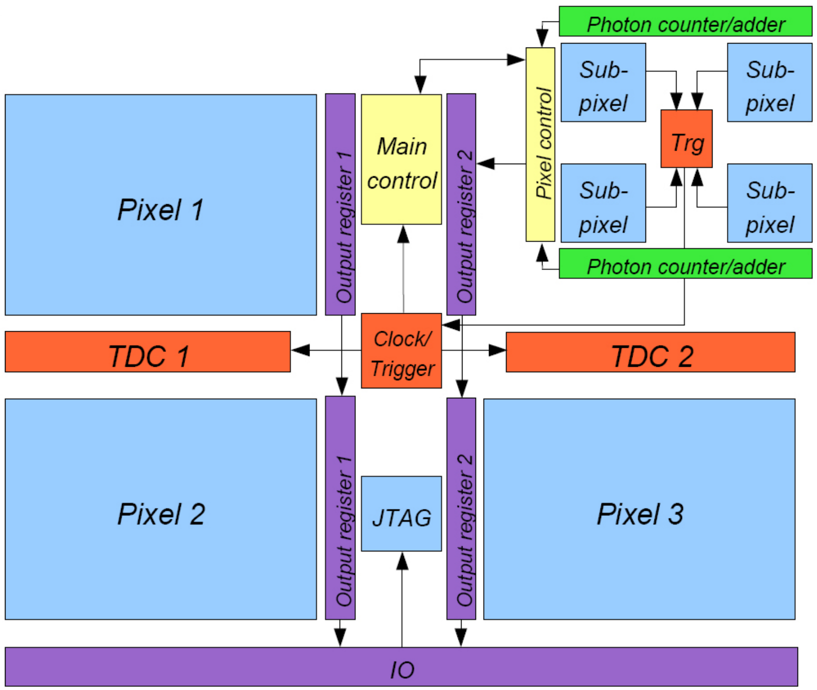


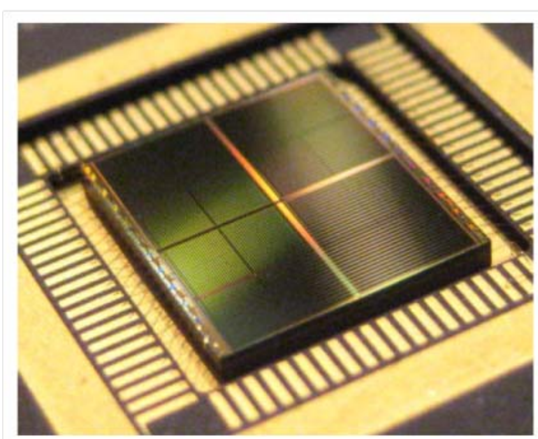


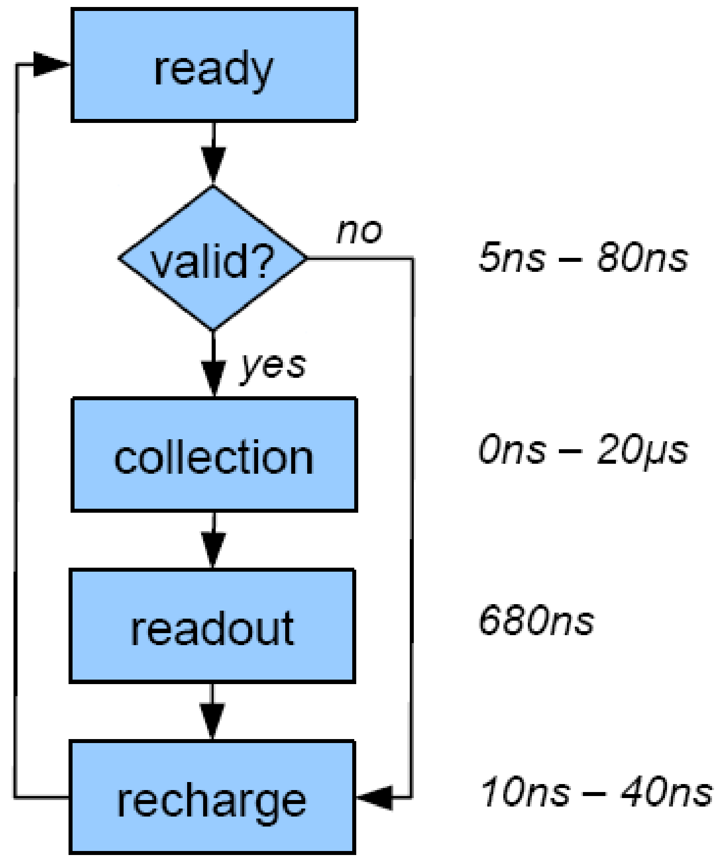
Output: - no. of photons/pixel
- time stamp(s)

No analog post-processing necessary!

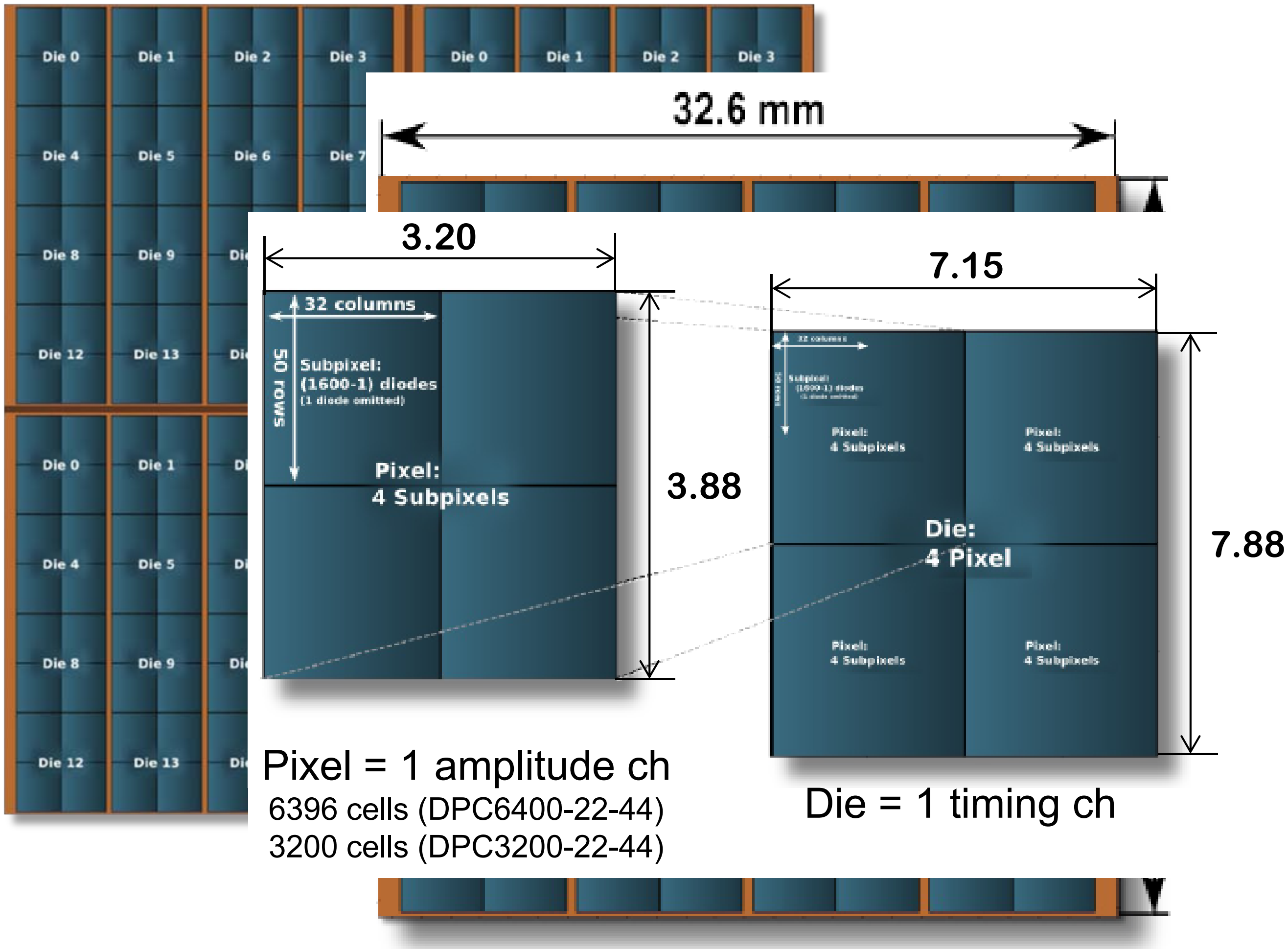
DPC sensors: Die Architecture and State Machine







DPC sensors: geometrical layout

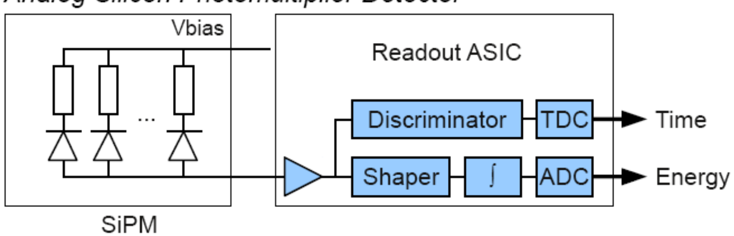


Pixels in module packing density ~70% PF

DPC is an Integrated, Scalable Solution

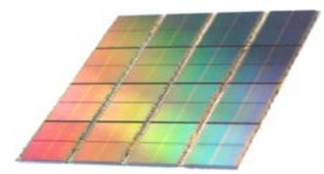
Analog SiPM

Analog Silicon Photomultiplier Detector

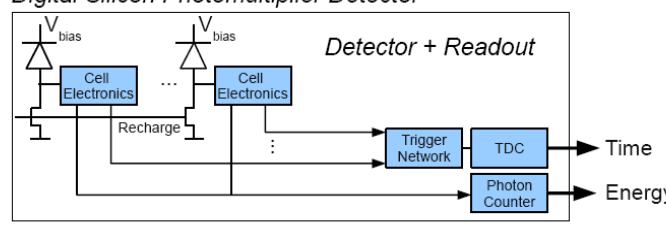


- discrete, limited integration
- analog signals to be digitized
- dedicated ASIC needed
- difficult to scale

Digital SiPM



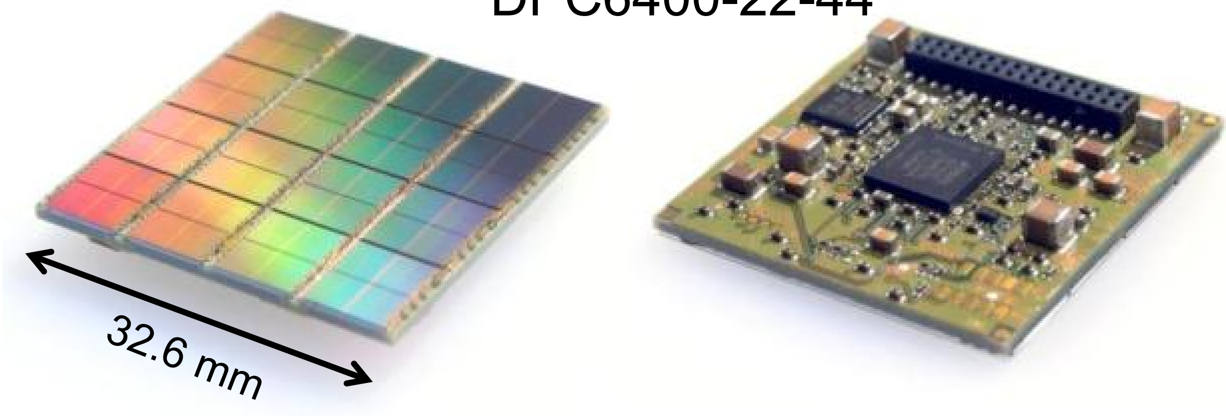
Digital Silicon Photomultiplier Detector



- fully integrated
- fully digital signals
- no ASIC needed
- fully scalable

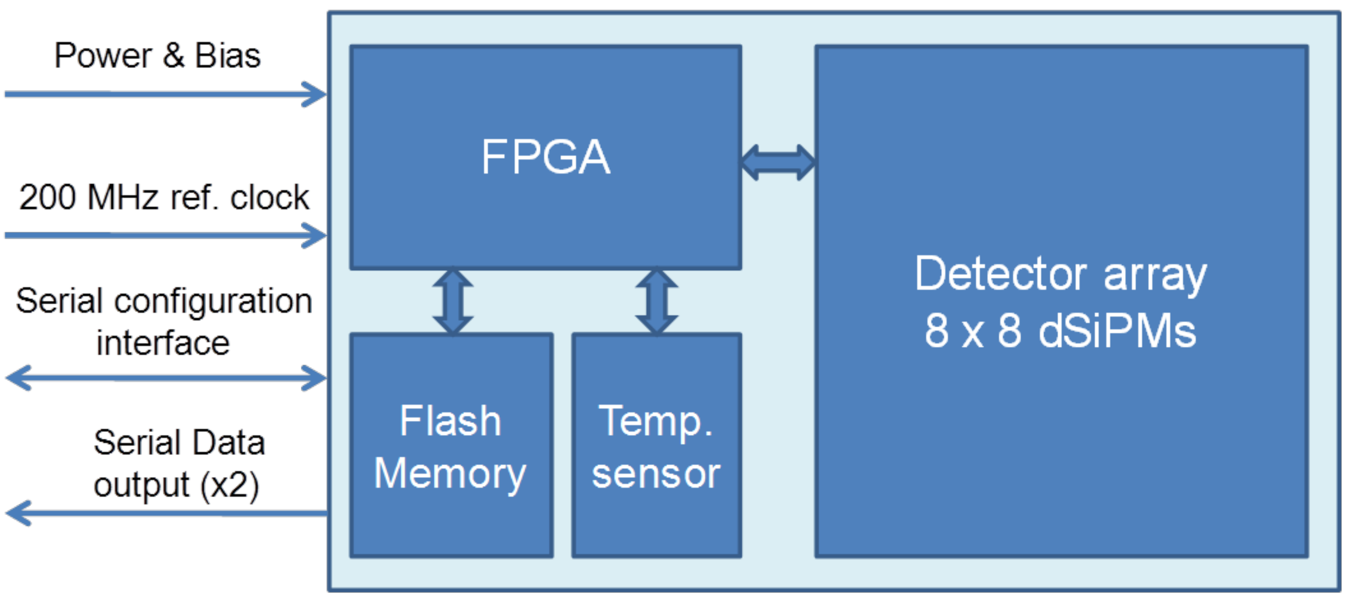
DPC is an Integrated "Intelligent" Sensor

DPC3200-22-44
DPC6400-22-44

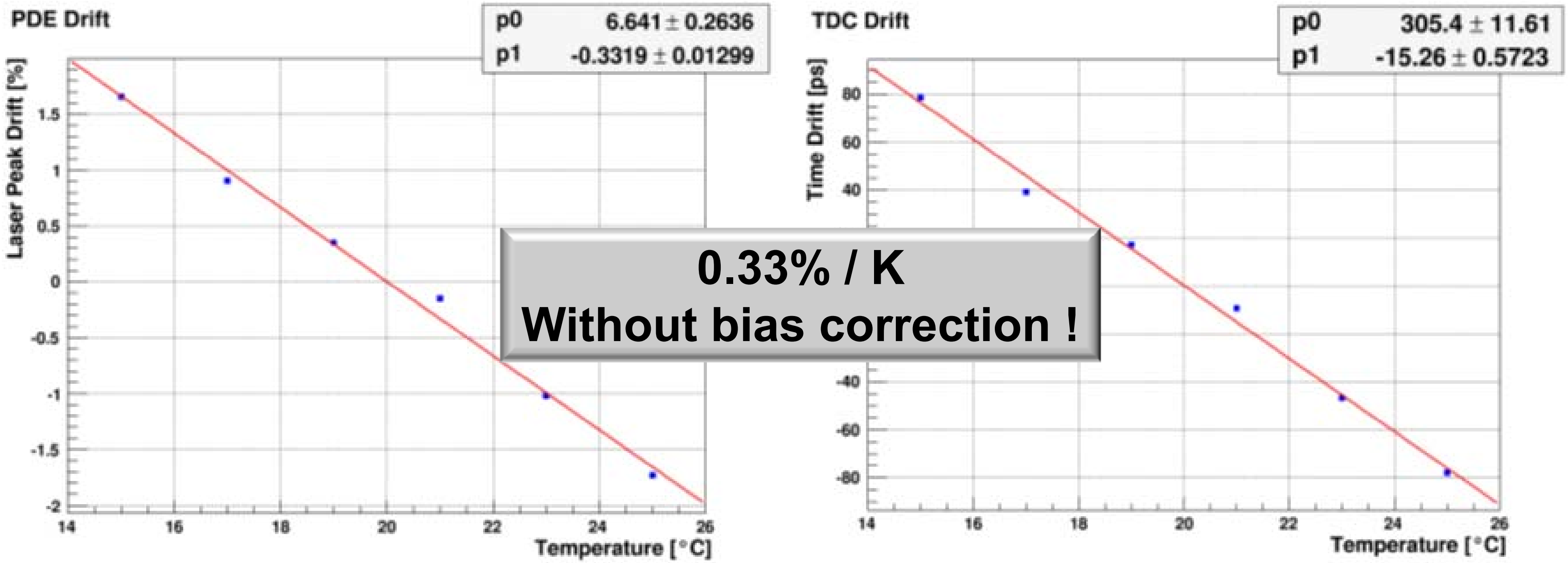


FPGA
- Clock distribution
- Data collection/concentration
- TDC linearization
- Saturation correction
- Skew correction

Flash
- FPGA firmware
- Configuration
- Inhibit memory maps

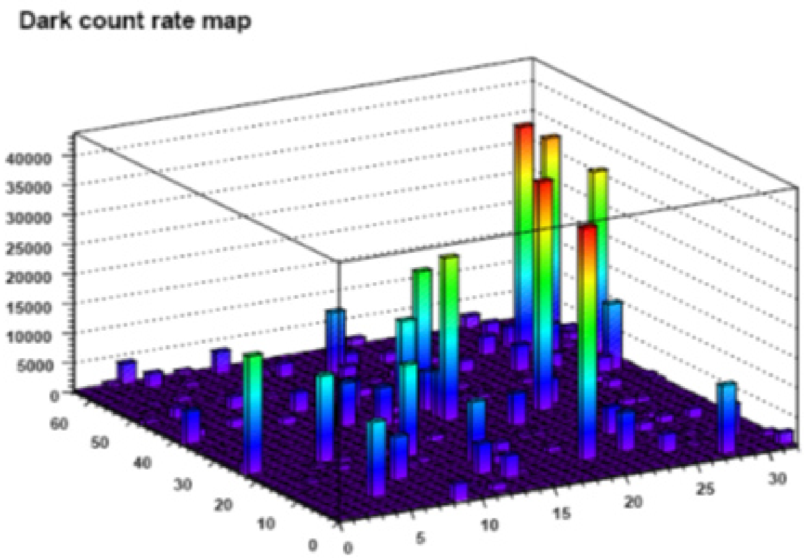


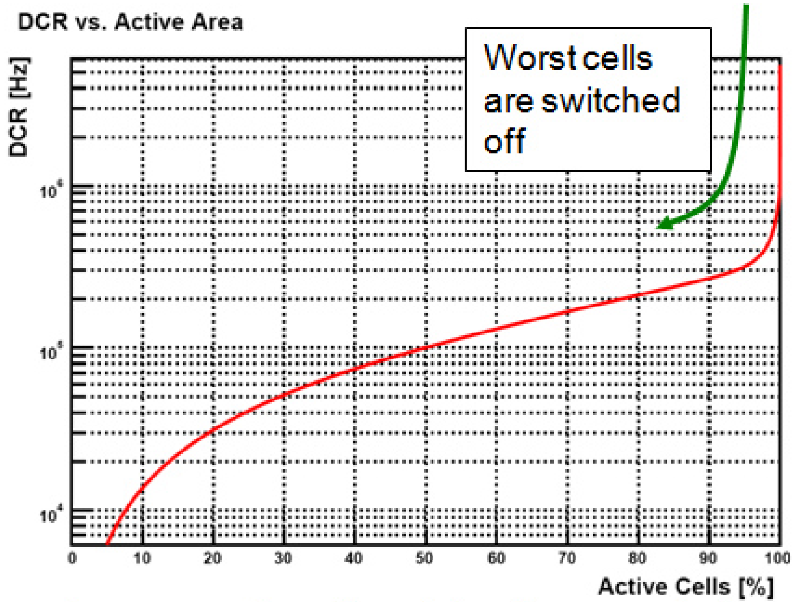
DPC: Front End Digitization Significantly Reduces Temperature Sensitivity



- **24 ps** full-width at half-maximum timing resolution of ps-laser
- Photopeak changes **0.33%** per degree C due to changing PDE **(values of analog SiPM's are ranging from 2-8%)**
- Time changes **15.3 ps** per degree C (TDC + trigger network drift)

DPC: CMOS Integration Allows Active Control of Dark Count Rate (DCR)





- Silicon based light sensors have background noise (dark counts), varying with temperature.
- In digital SiPMs every cell can be addressed individually.
- Cells with high dark counts can be switched off.
- A few cells switched off (1-5%) reduces dark count levels by orders of magnitude.

DPC: Superior Intrinsic Timing Resolution of Digital Arrays

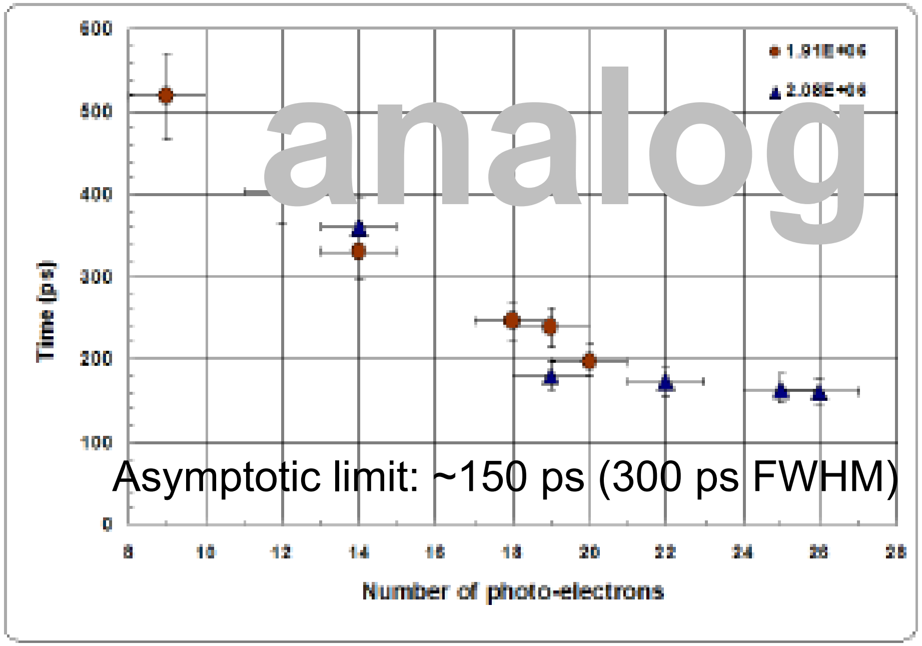
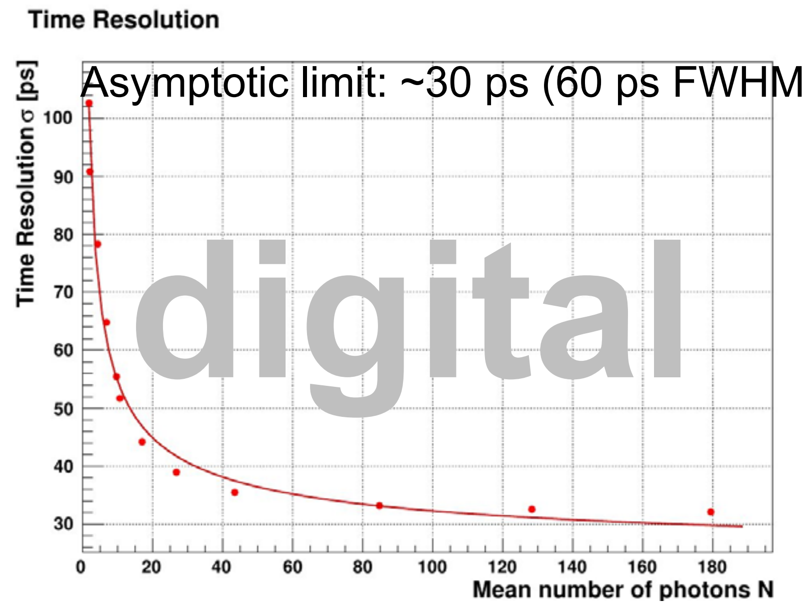


Figure 6. MPPC3, Time resolution as a function of the number of simultaneous photoelectrons for two amplifications.

Ahmed et.al., JINST, Sept. 2009

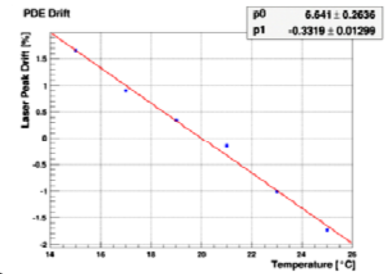


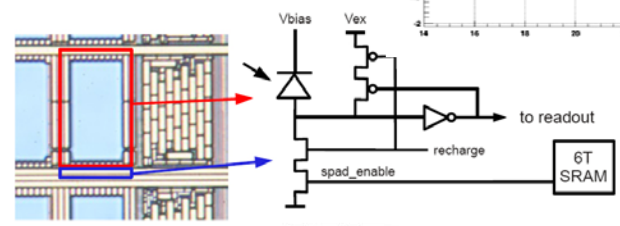
- shorter wiring
- no dependency on external A/D electronics

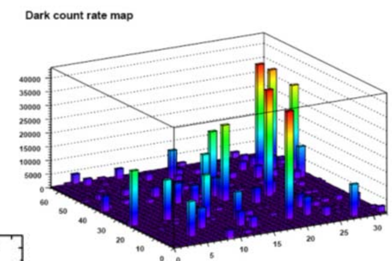
Frach et.al., PDPC, 2009-2011

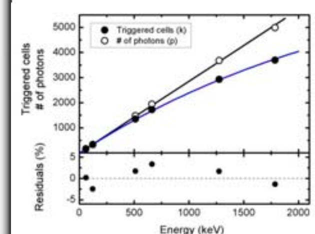
Sub-Summary: Advantages of Philips' DPCs

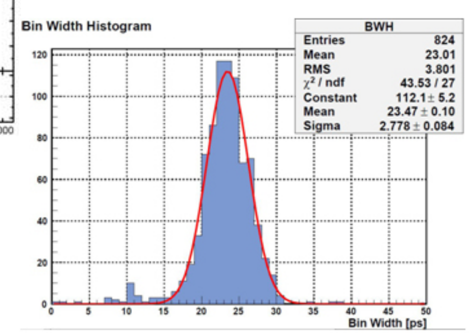
- significantly reduced temperature sensitivity ($\sim 10^{-1}$)
- active quenching reduces afterpulsing & crosstalk ($\sim 10^{-1}$)
- individually addressable cells enable DC control ($\sim 10^{-2}$)
- better linearity (&correction)
- better intrinsic timing resolution due to integrated TDCs (~ factor 5)
- no analog electronics, no ADCs, no ASICs





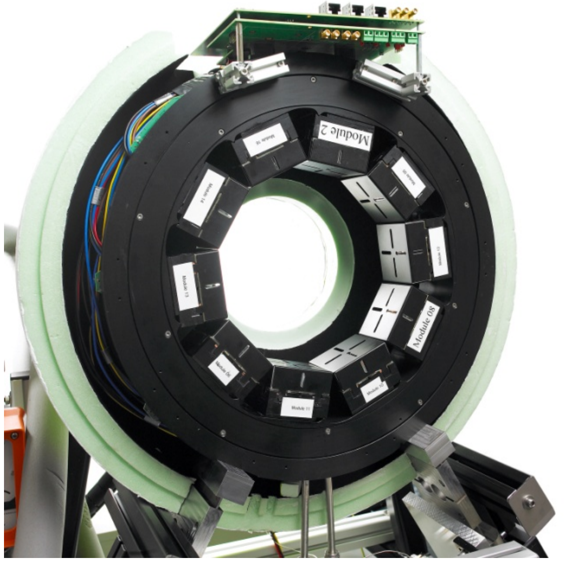




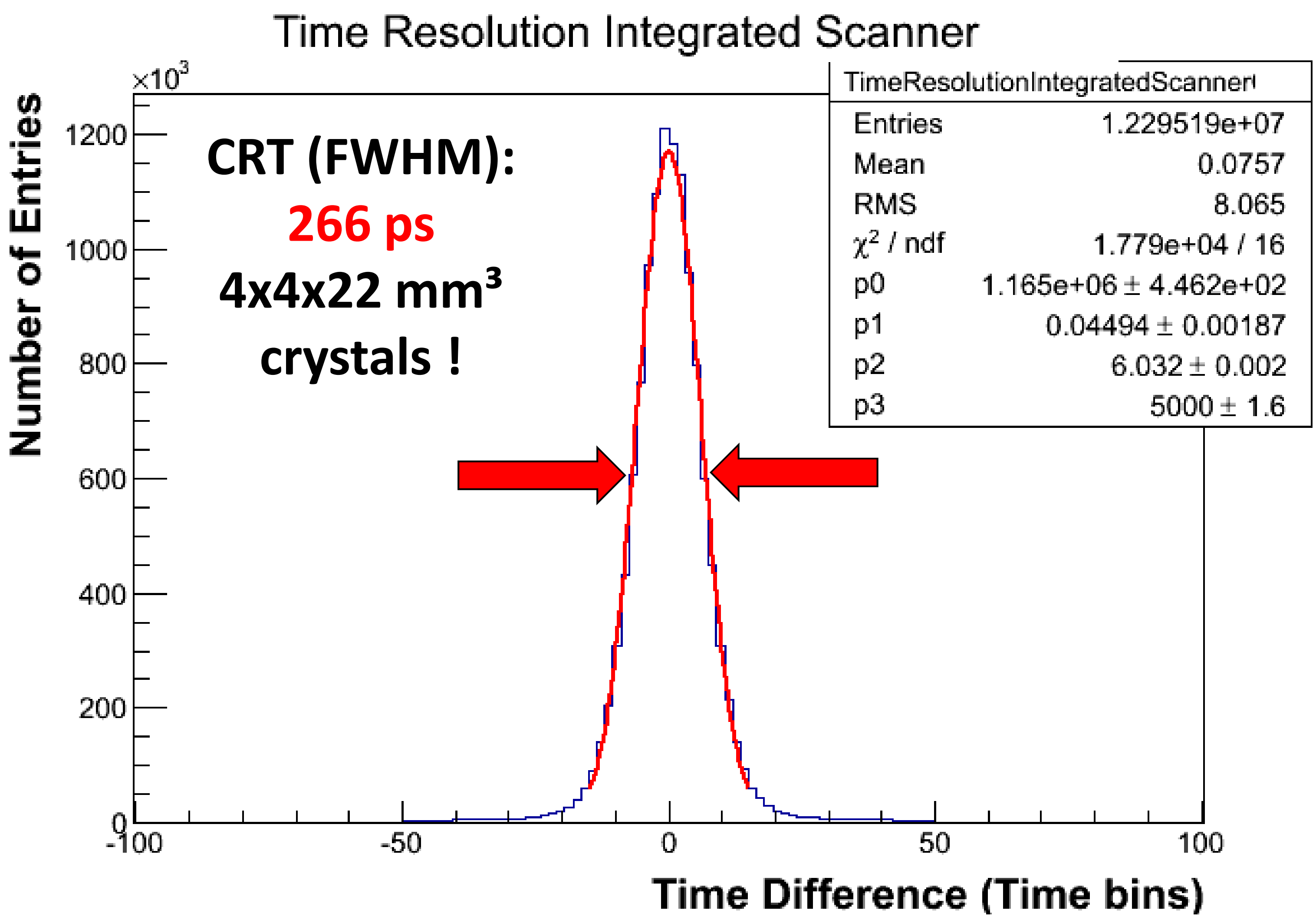


DPC Technology proof: Test PET-Ring (@FZ Juelich)

- Inner Diameter (face-to-face): 20 cm
- 10 modules a 4 sensors
- LYSO 4 x 4 x 22 mm²
- Coolable down to -5°C
- Sensor temp. : ~ 5-10°C



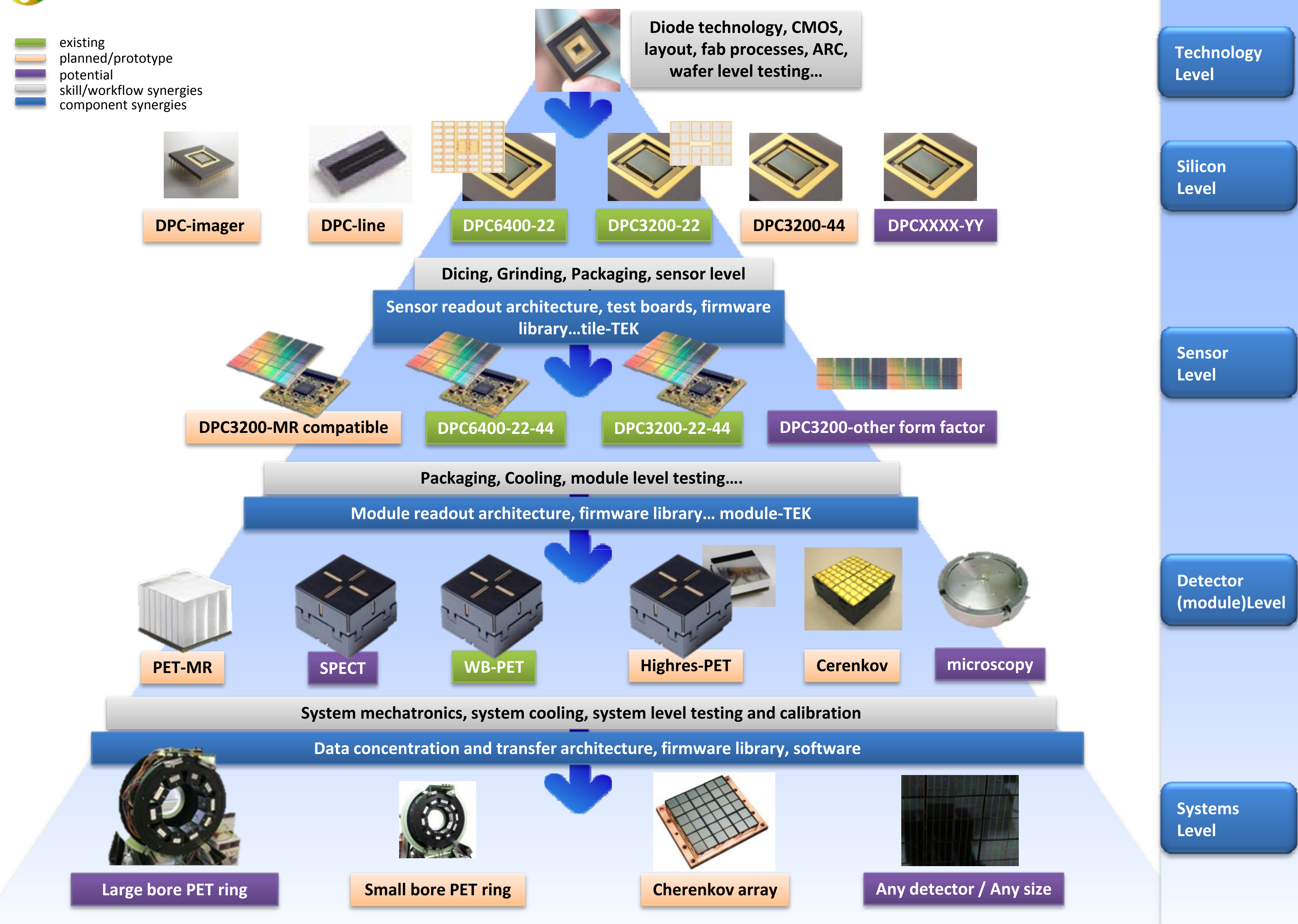
DPC Technology Test PET-Ring: Same CRT as with single pixel & array



DPC Technology: Detector Modules

- **4 DPC sensor arrays (tiles)**
- **~ 6.6 x 6.6 cm²**
- **usable with or w/o scintillator crystals**
- **variable scintillator geometries**
- **Module board with FPGA, pre-processing capability & simple interface**
- **experimentally coolable to - 40°C**

The Philips tree of scalable DPC technology



First test of DPC in High Energy Physics: FARICH Detector @ CERN, June 2012

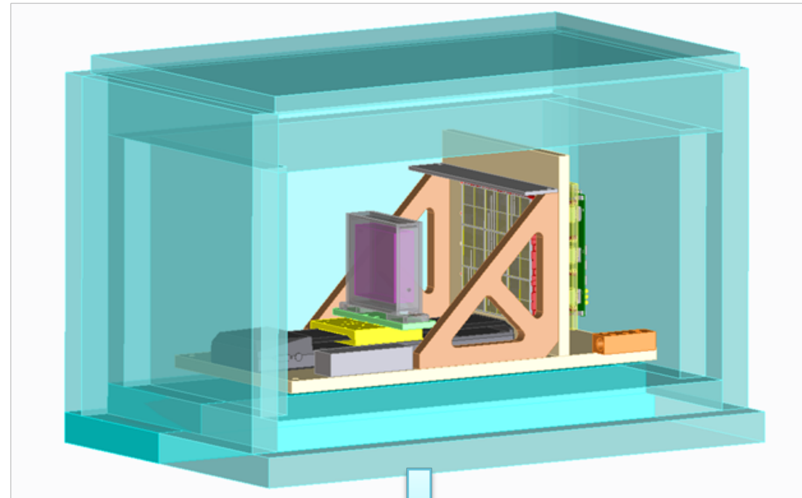
Main objective:

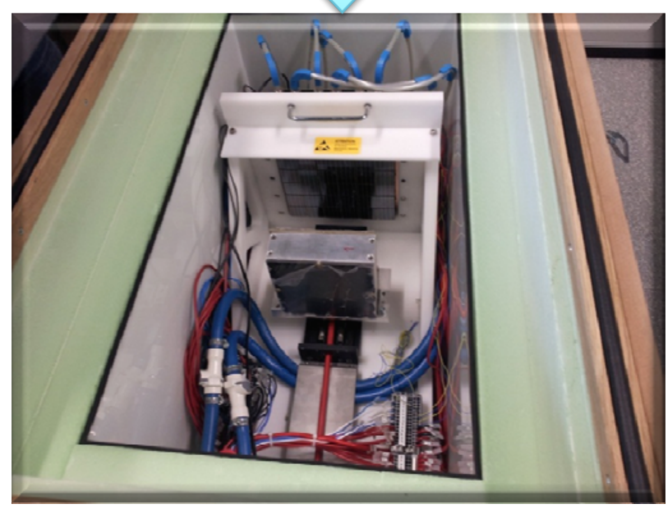
Proof of concept: full Cherenkov ring detection with DPC array

Timeline:

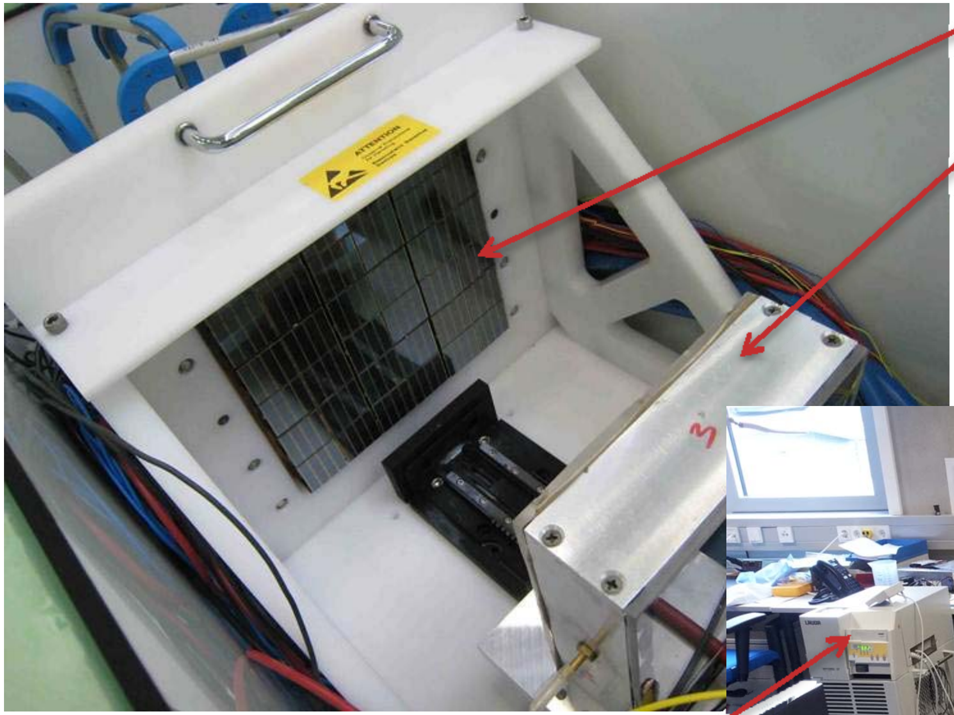
- Started to envisage: **28/02/12**
- Requirements for the FARICH prototype test setup fixed: **30/04/12**
- Prototype operational @ Aachen Labs: **03/06/12**
- Installed @ CERN: **12/06/12**
- Subsequent beam runs for 12 days until **25/06/12** with smooth setup operation

DPC allows for fast prototyping!





First Fully Digital FARICH DPC Detector Prototype



DPC detector 20x20 cm²

Aerogel sample container on movable table

Operation at -40°C to suppress dark counts: DCR ~ 100 kcps/die. Blow dry N_2 to avoid condensation.

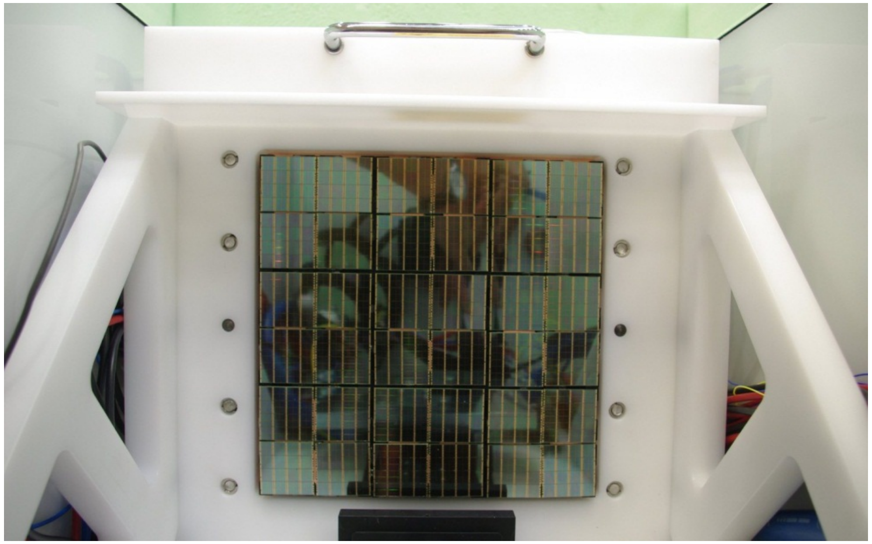
Process thermostat
LAUDA Integral XT

Thermal insulation:
10 cm styrofoam

First fully digital FARICH DPC Detector Prototype

4-layer aerogel

- n_{max} = 1.046
- Thickness 37.5 mm
- Calculated focal distance 200 mm
- Hermetic container with plexiglass window to avoid moisture condensation on aerogel



DPC detector: 20x20 cm^2

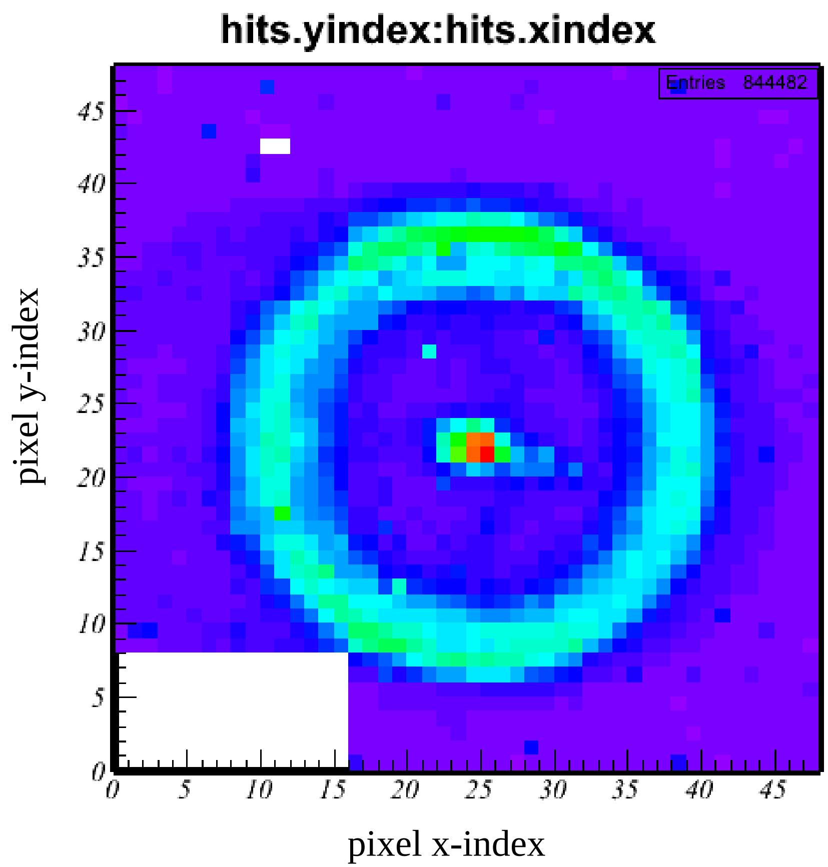
- Sensors: DPC3200-22-44
- 3x3 modules = 6x6 tiles = 24x24 dies = 48x48 pixels in total
- 576 time channels
- 2304 amplitude (position) channels
- 4 levels of FPGA readout: tiles, modules, bus boards, test board

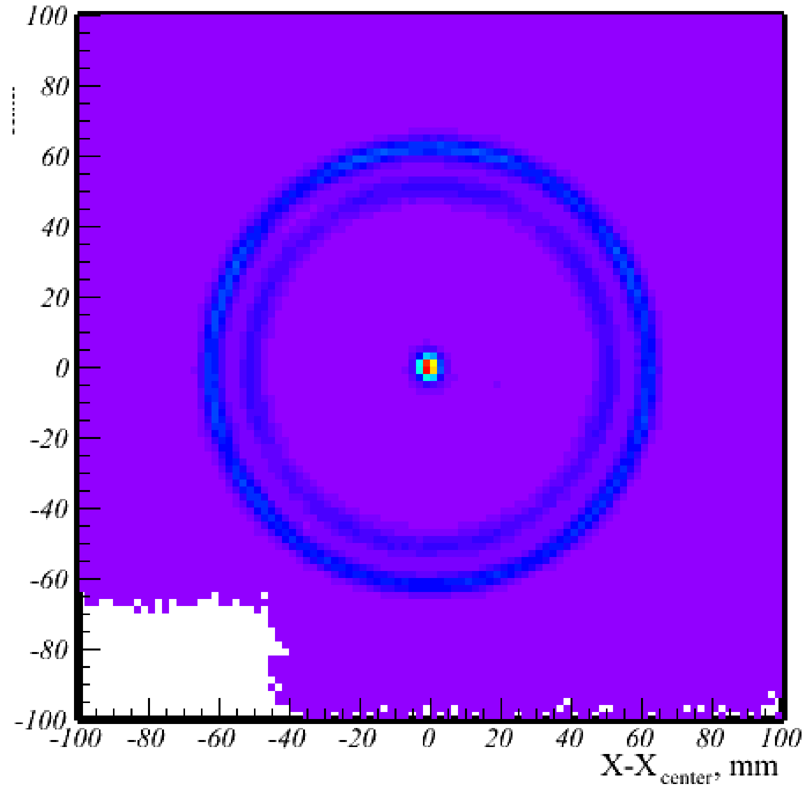
FARICH DPC: observation of Cherenkov ring

Pixel hit map

Test

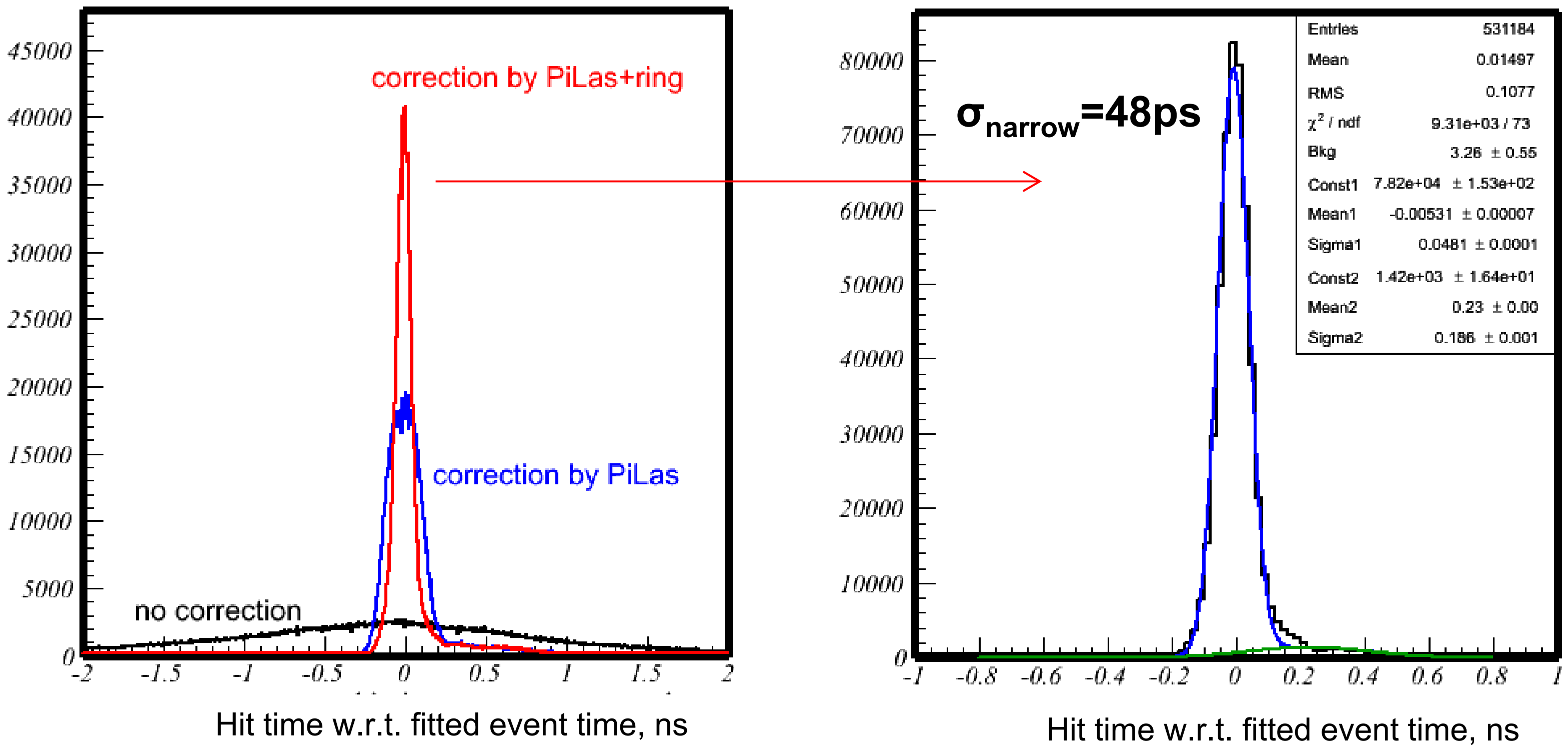
Hit positions





A.Yu. Barnyakov et.al.: submitted to Nucl. Instr. Meth. A

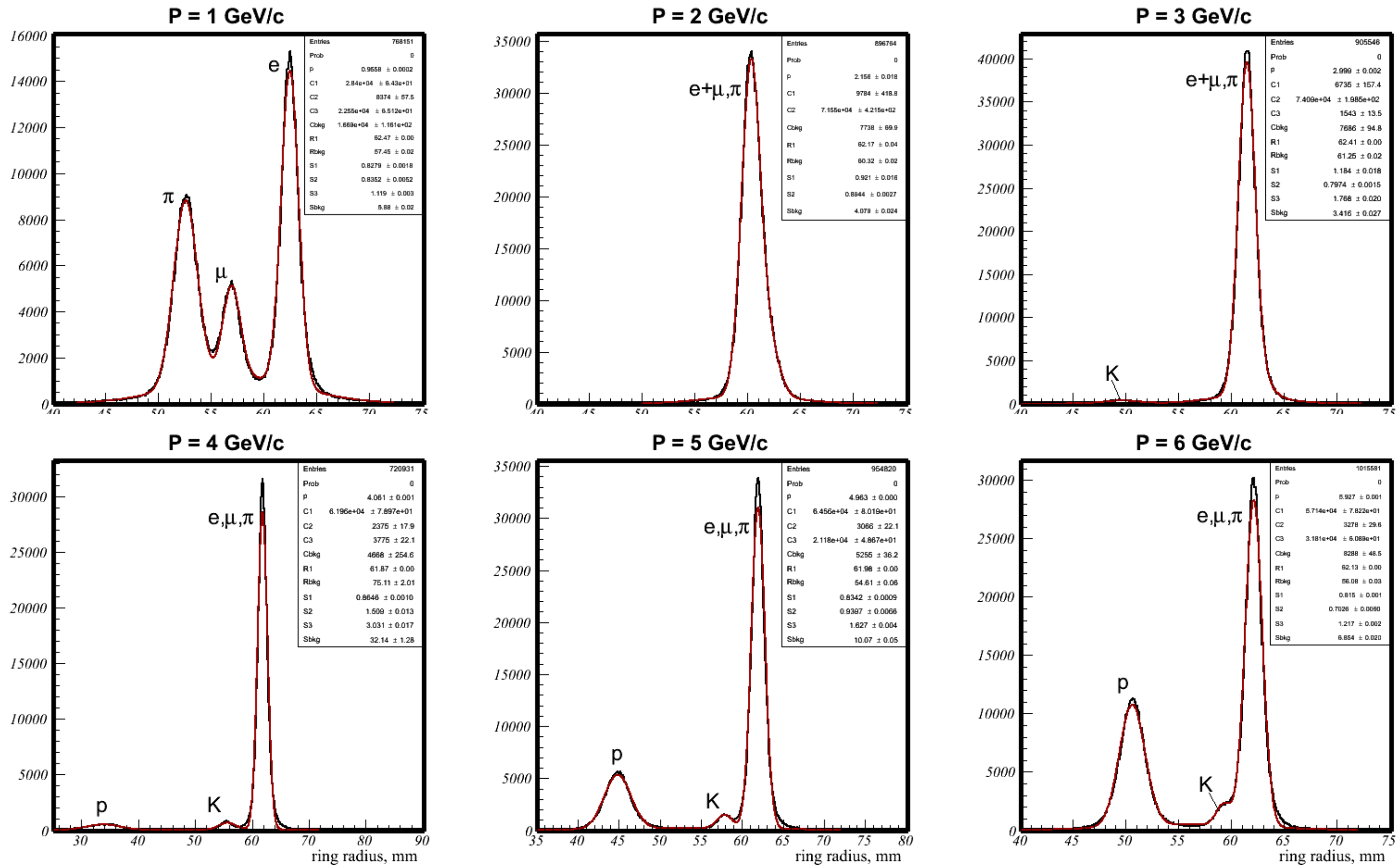
FARICH DPC: timing resolution for Cherenkov photons



Fit two gaussians plus constant. 90% of area is contained in the narrow gaussian.

A.Yu. Barnyakov et.al.: submitted to Nucl. Instr. Meth. A

FARICH DPC: momentum dependence (6 data points)



Not more than 3 particle peaks are fit in each point

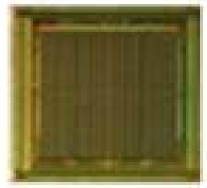
A.Yu. Barnyakov et.al.: submitted to Nucl. Instr. Meth. A

π /K: 3.8 σ @ 6 GeV/c
μ/π: 4.5 σ @ 1 GeV/c

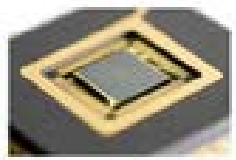
DPC: Scalable Technology Maintains Intrinsic Performance

DEMONSTRATOR:
single pixel

CRT= 280 ps*



CHIP:
2 x 2 = 4 pixels



CRT= 280 ps*

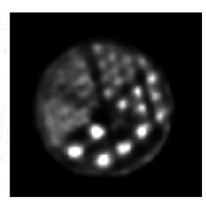
ARRAYS (TILES):
8 x 8 = 64 pixels

CRT= 280 ps*

MODULES:
256 pixels

CRT= 280 ps*

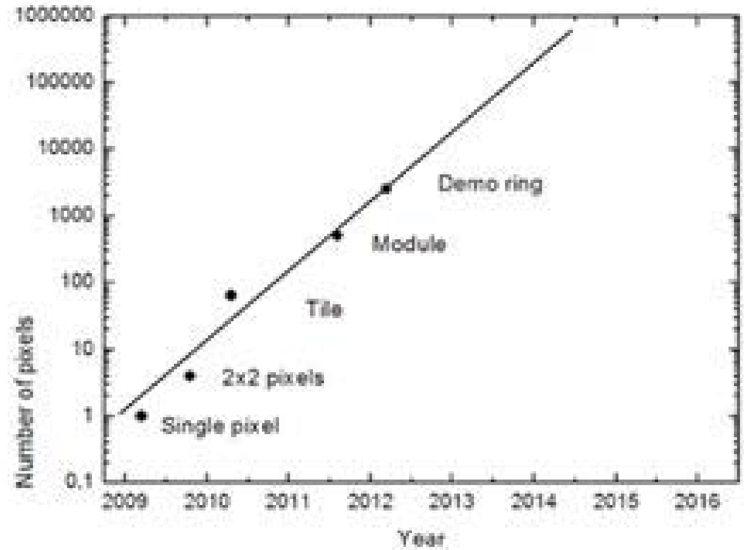
DEMO RING:
2560 pixels



CRT= 280 ps*

Many first time rights

PDPC-Moore‘s law



2.4 mm spatial resolution using 4x4x22 mm³ crystals!

PDPC Technology Evaluation Kit (TEK)

23 kits installed so far

Summary/Outlook

- **Demonstrated scalability of Philips DPC technology by maintaining intrinsic performance in POC devices:**
  - ***PET test ring***
  - ***FARICH detector prototype***

Next:

- **Expansion of Scale of technology:**
  - ***detectors with larger number of pixels***
  - ***additional building blocks of scalable architecture***
- **Improved performance of DPCs (2nd generation):**
  - ***higher PDE (>40%)***
  - ***less dead time (factor 5)***
  - ***better intrinsic timing resolution (factor 2)***
  - ***sub-pixel (2 mm^2) readout***
- **New designs for new applications**
  - ***line- and spectroscopy sensors***
  - ***Lidar, FLIM, Spectroscopy***

Thank you very much for your attention!

Thanks also to:

PET

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