GBLD

Sezione di Torino

A 5 Gb/s Radiation Tolerant Laser Driver in CMOS 0.13 µm technology

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Outline

Sezione di Torino

- The GBT project
- The GBLD laser driver
- Modulator architecture
- Test results
- Conclusions

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GBT Chipset

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Radiation tolerant chipset :

- GBTIA : Transimpedance optical receiver
- GBLD : Laser driver
- GBTx : Data and Timing Transceiver
- GBT-SCA : Slow control ASIC

Target Applications :

- Data readout
- TTC
- Slow control and monitoring links

Supports :

- Bidirectional data transmission
- Bandwidth :
  - → Line rate : 4.8 Gb/s
  - → Effective : 3.36 Gb/s

Radiation Tolerance :

- Total dose
- Single Event Upset

GBT architecture

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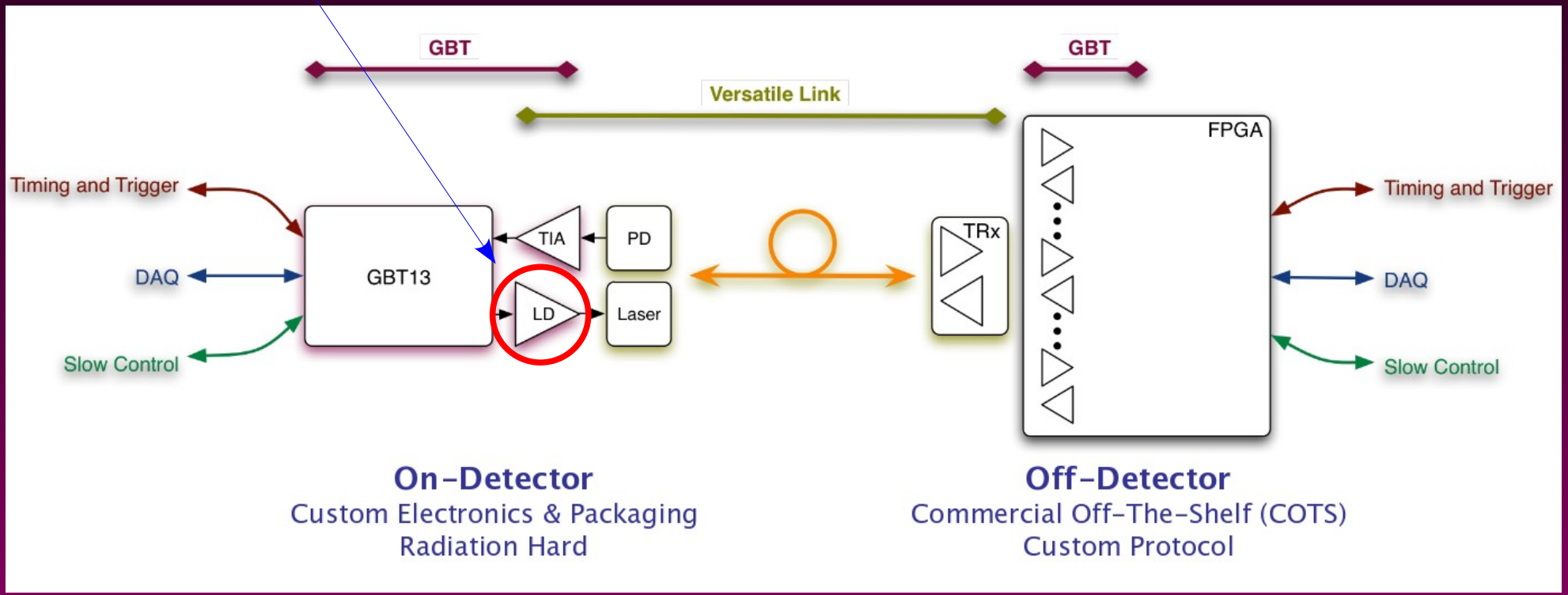
GBLD



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GBLD specifications

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- Max bit rate : 5 Gb/s
- Possibility to drive both edge emitting lasers and VCSELs
- Differential and single ended driving
- Modulation current : 2÷24 mA
- Bias current : 2÷43 mA
- Pre-emphasis/de-emphasis current : 0÷12 mA
- Independently programmable rising and falling edge pre/de-emphasis
- I^2C digital control with SEU protection

Challenging items

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- EE lasers I_{ON} ~ tens of mA, R_D ~ Ω
- VCSEL I_{ON} ~ mA, R_D ~ tens of Ω
- Big devices needed to drive high currents

  → big parasitic capacitance
- 2.5 V power supply needed for proper laser bias
- Commercial transceivers normally :

  → are based on (SiGe) BiCMOS technology

  → address only one type of lasers

GBT block diagram

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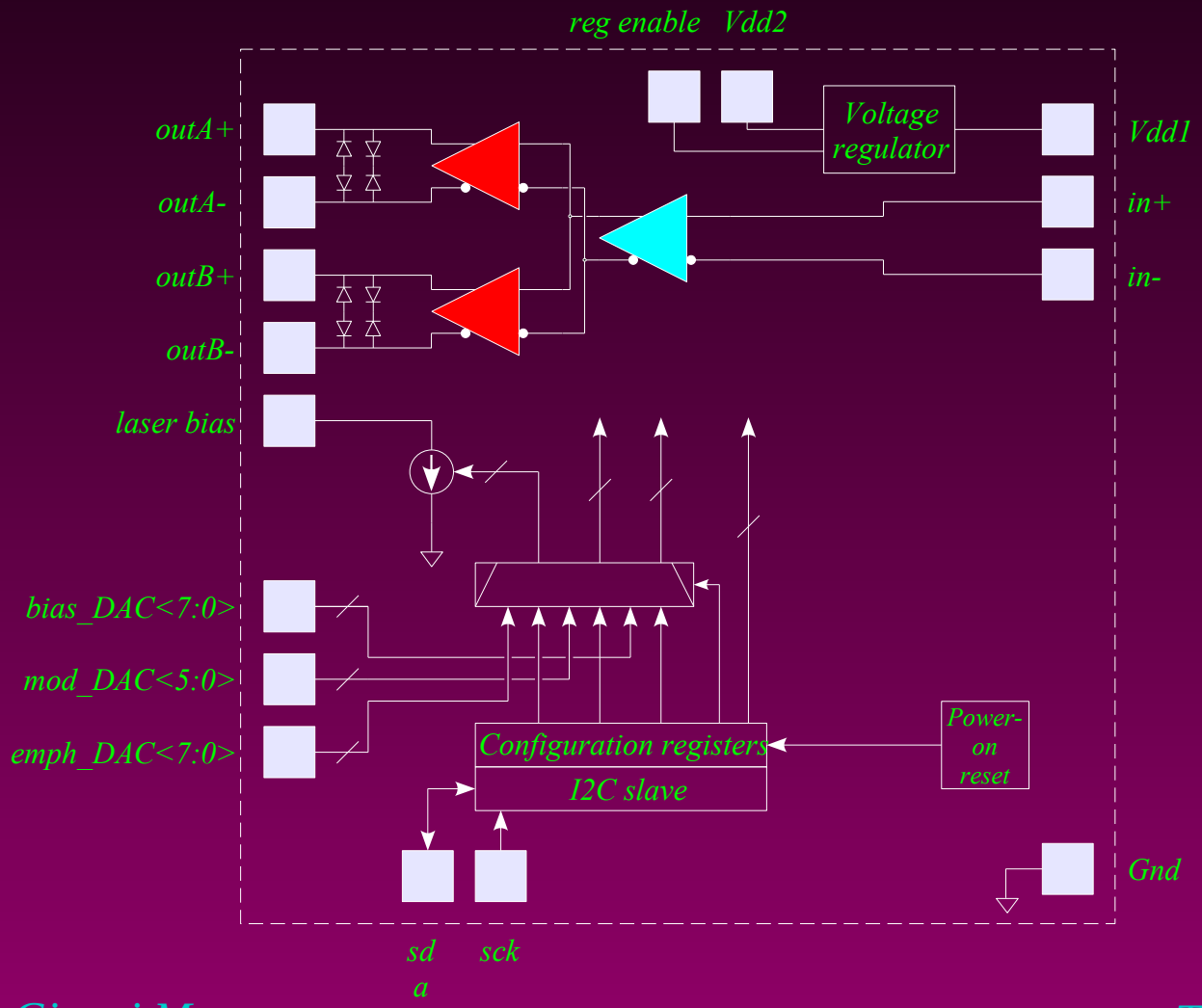

- Two drivers architecture
- Same driving signal
- Same control DAC
- Range 1 : one driver - 2÷12 mA and 50 Ω termination
- Range 2 : two drivers in parallel - 4÷24 mA and 25 Ω termination

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Modulator scheme

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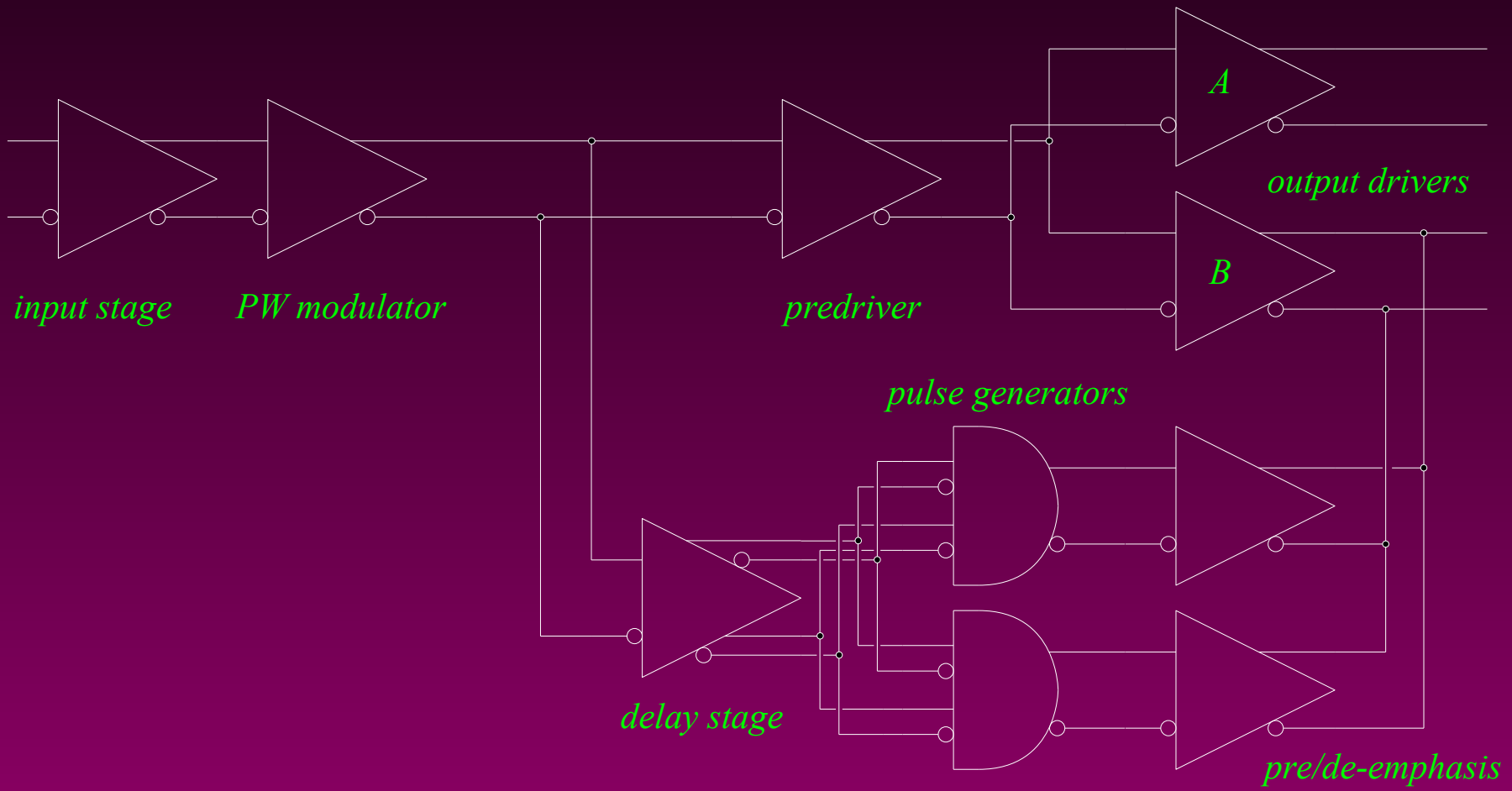

Output drivers

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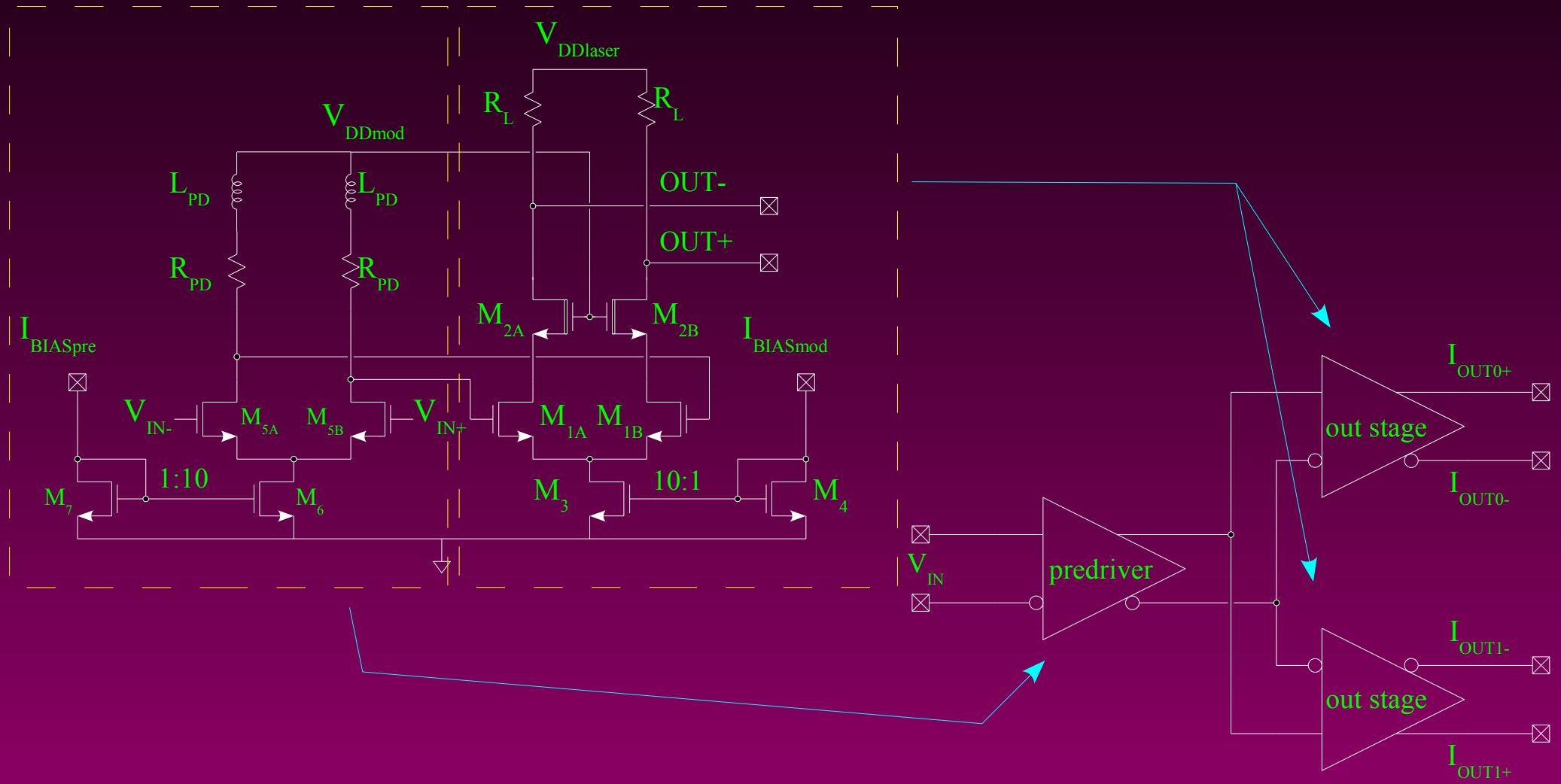
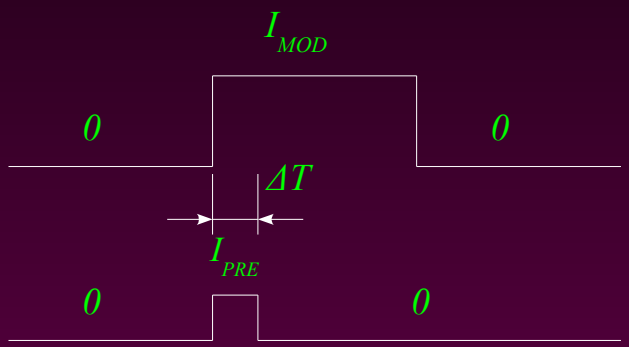
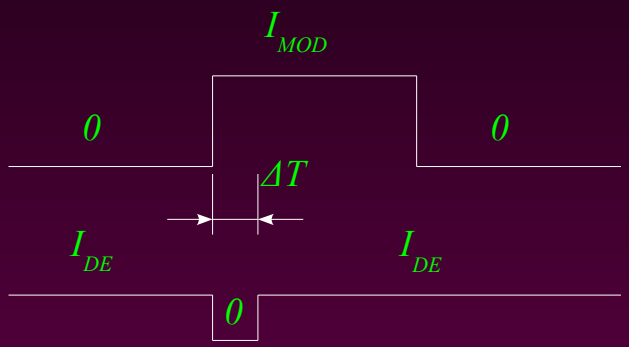
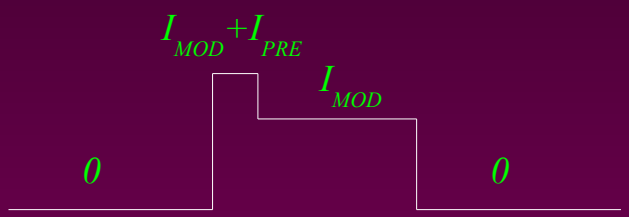


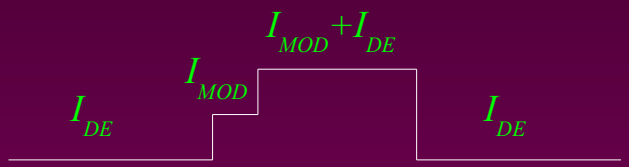
Pre/de-emphasis - 1

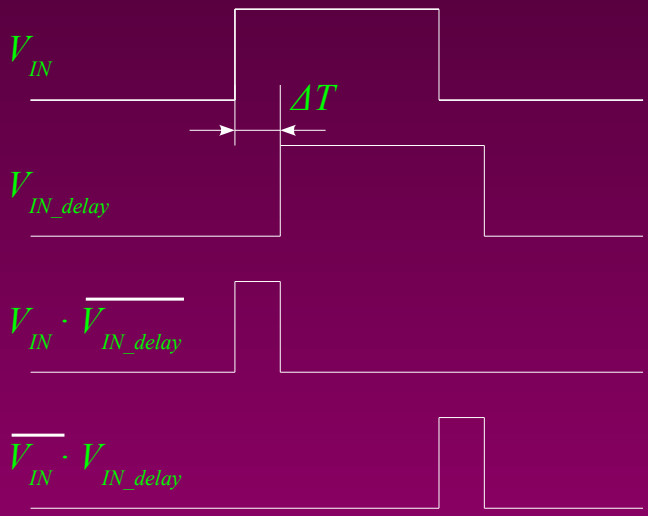
Sezione di Torino





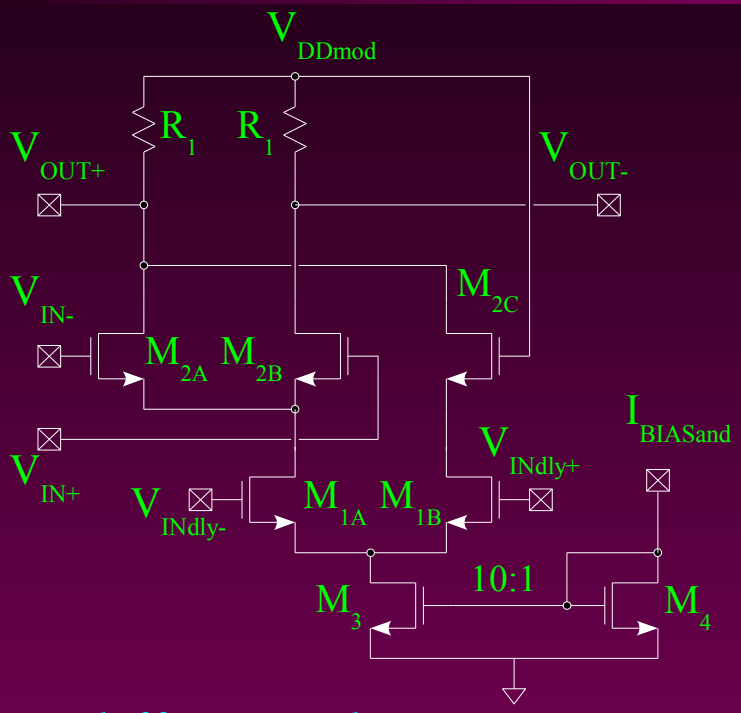






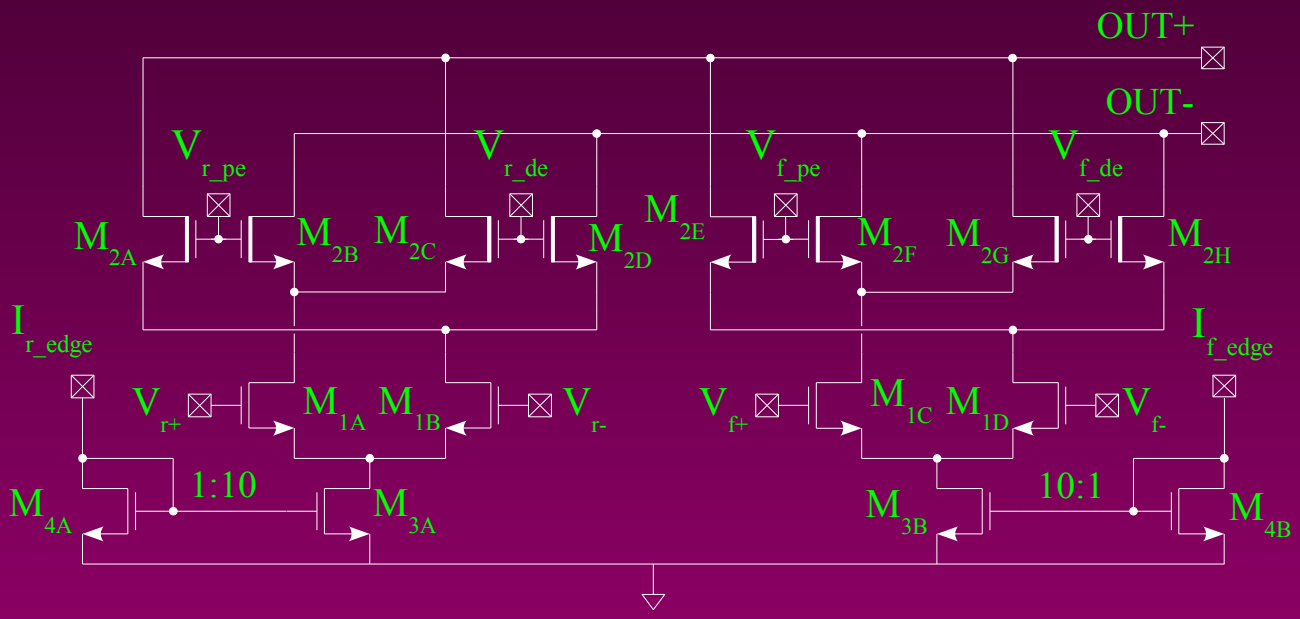
Pre/de-emphasis - 2

Sezione di Torino

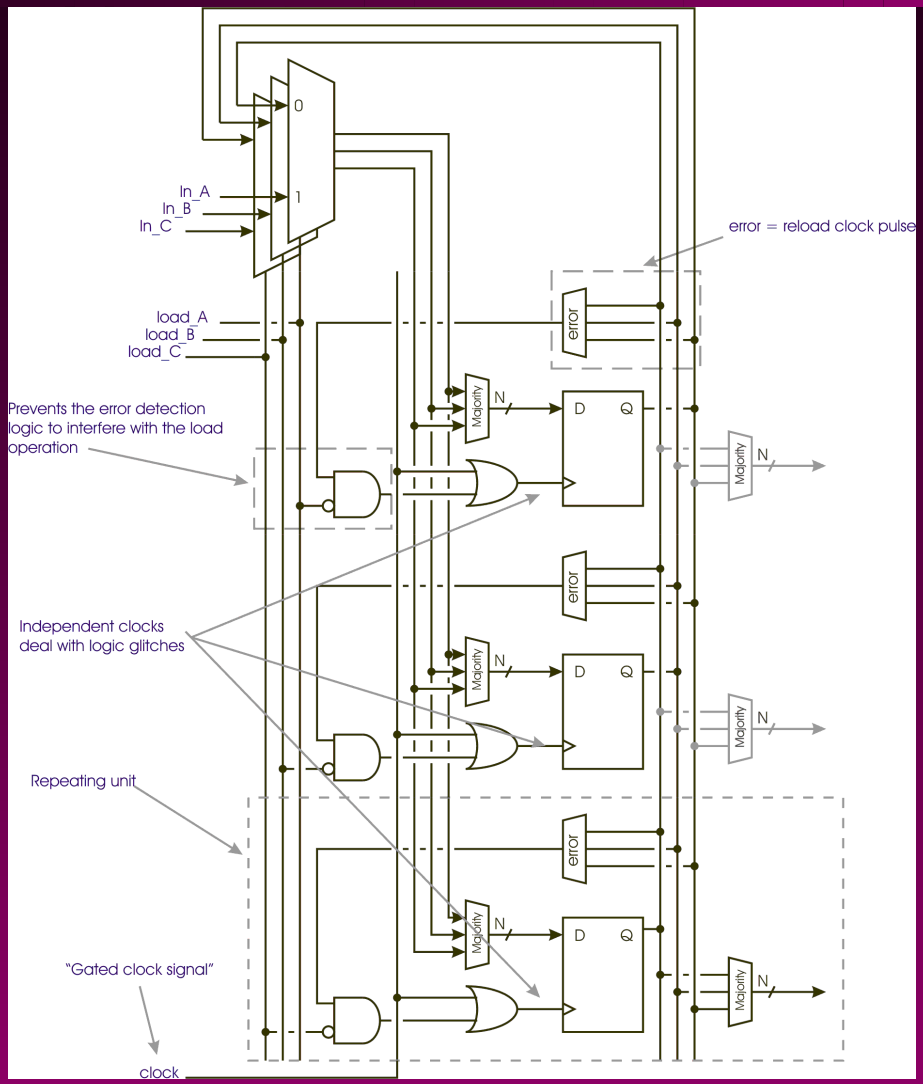


differential AND gate

Pre/de emphasis output driver



SEU protection



- Triple modular redundancy with self correction
- I^2C clock is not continuous → asynchronous circuit required
- A clock rising edge is generated when :
  i. a corrupted bit is detected,

  and

  ii. there is no load signal
- Once the bit is corrected, the clock signal is automatically cleared

Chip layout

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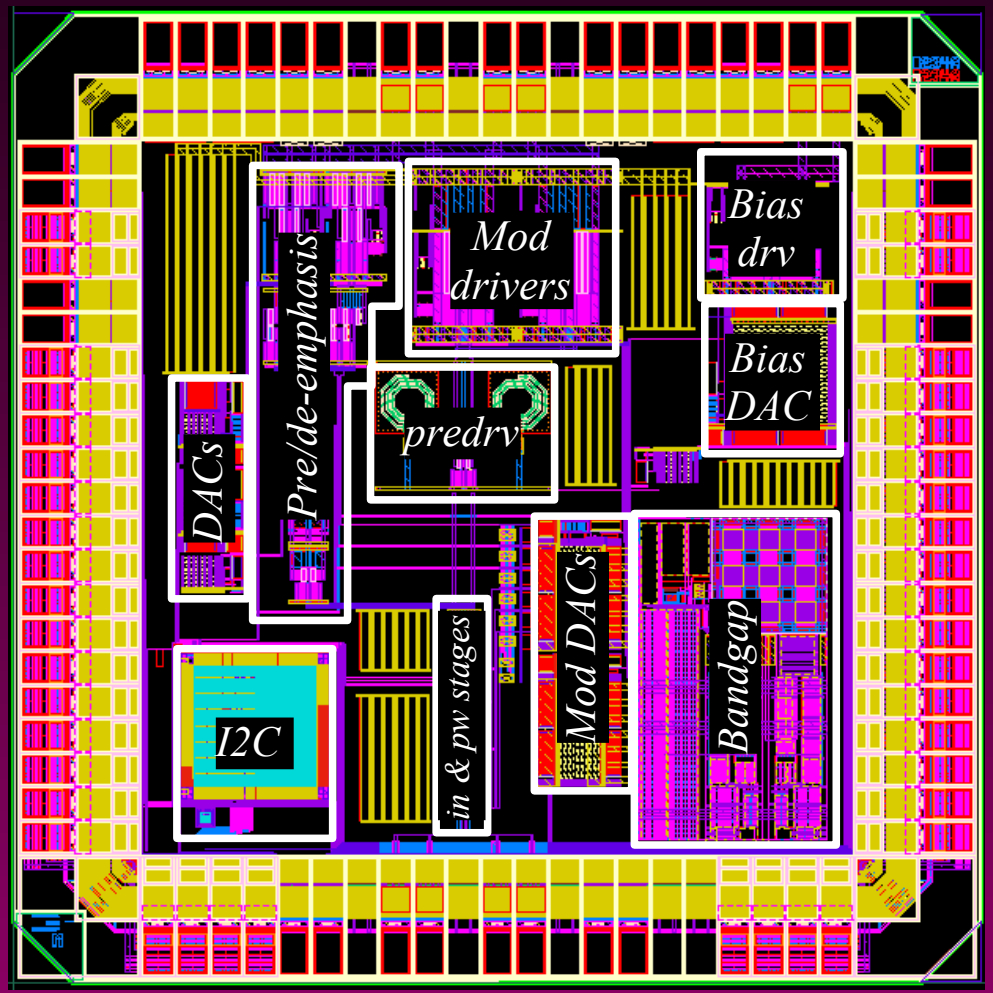

- CMOS 0.13 μm technology
- 6+2 metal layers
- Area : 2×2 mm^2
- 2 power supplies : 1.5 V and 2.5 V
- Power consumption : max 460 mW
- ~750 pF filter capacitor/supply
- Package : QFN28 5×5 mm^2

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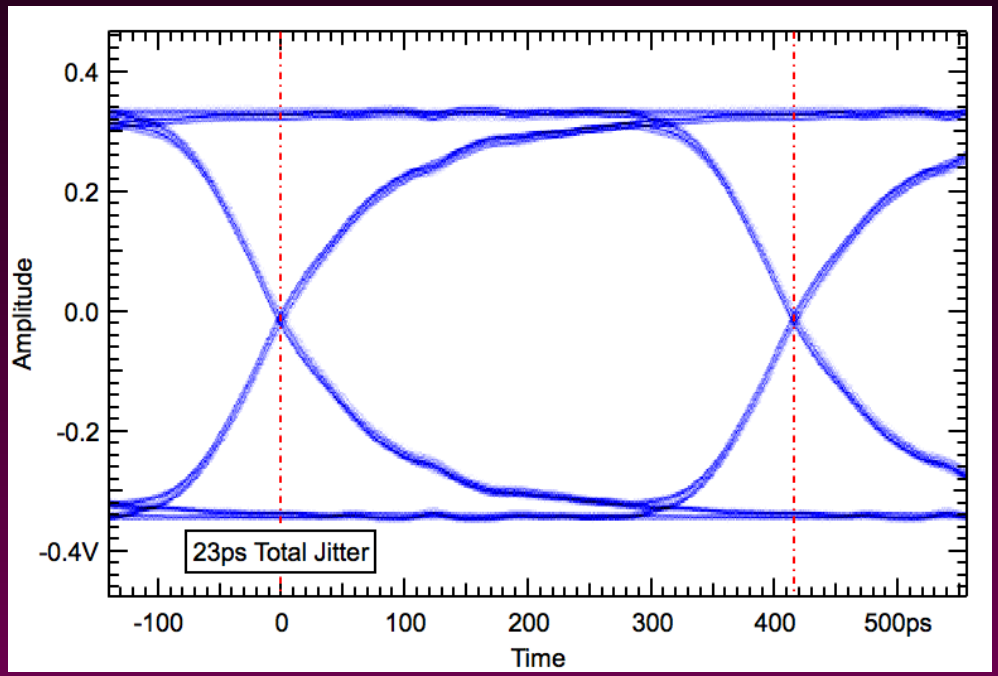
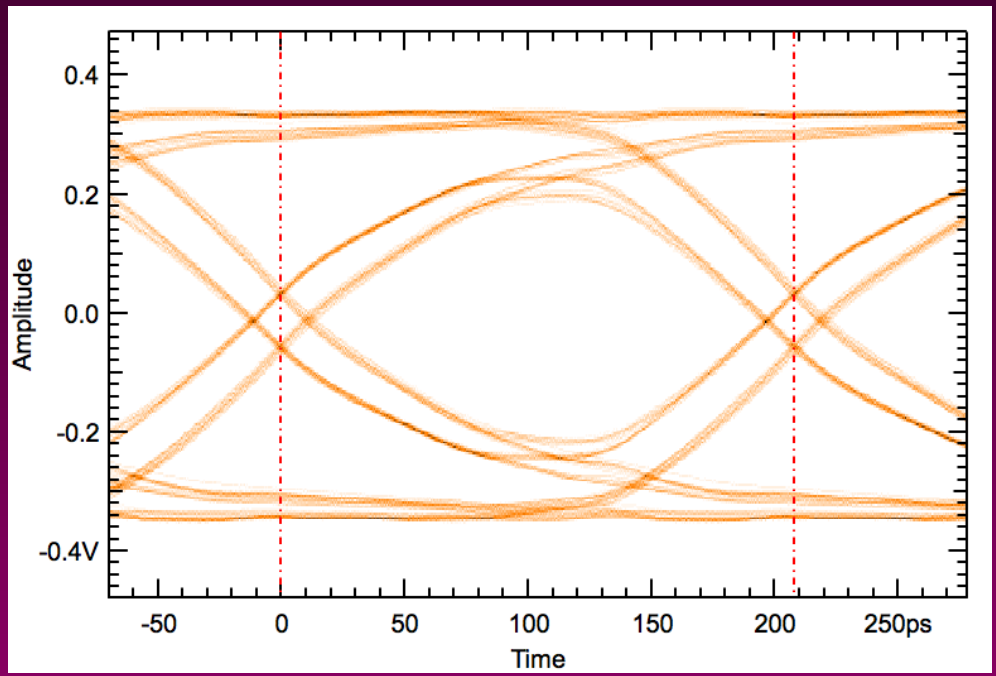
Eye diagram

Sezione di Torino



@ 2.4 Gb/s

@ 4.8 Gb/s



Rise/fall time

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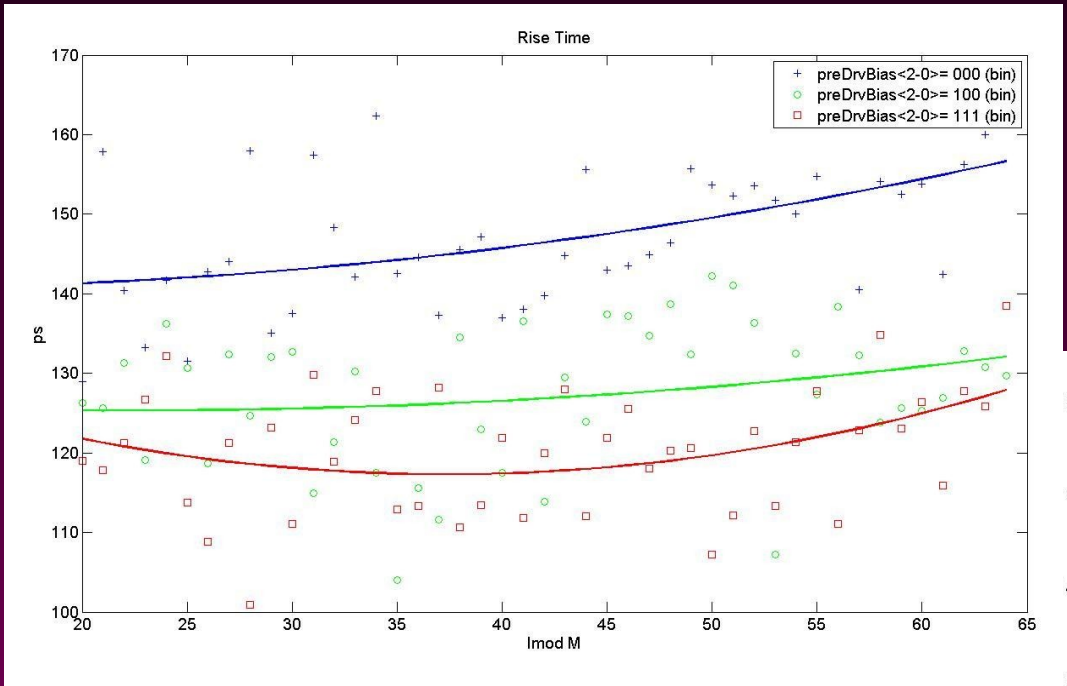
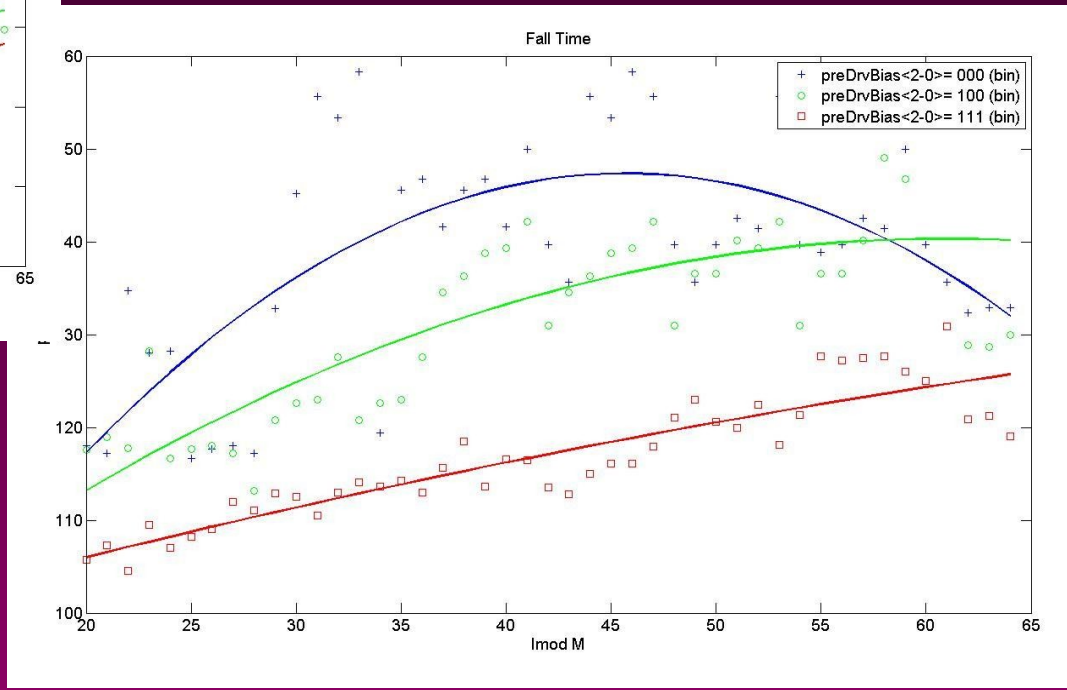


@ 5 Gb/s



Predriver biased at :
6 mA (blue)
10 mA (green)
14 mA (red)

Jitter

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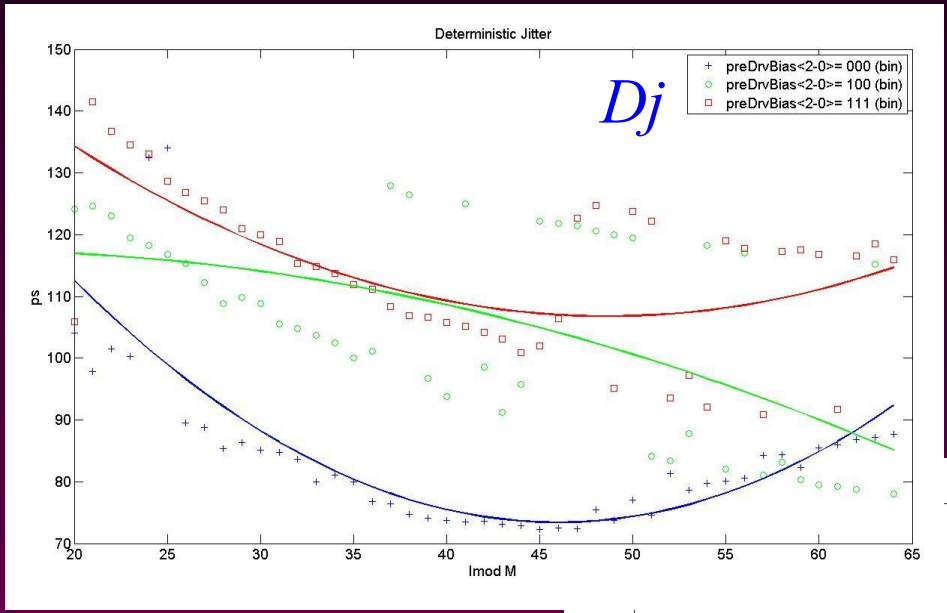
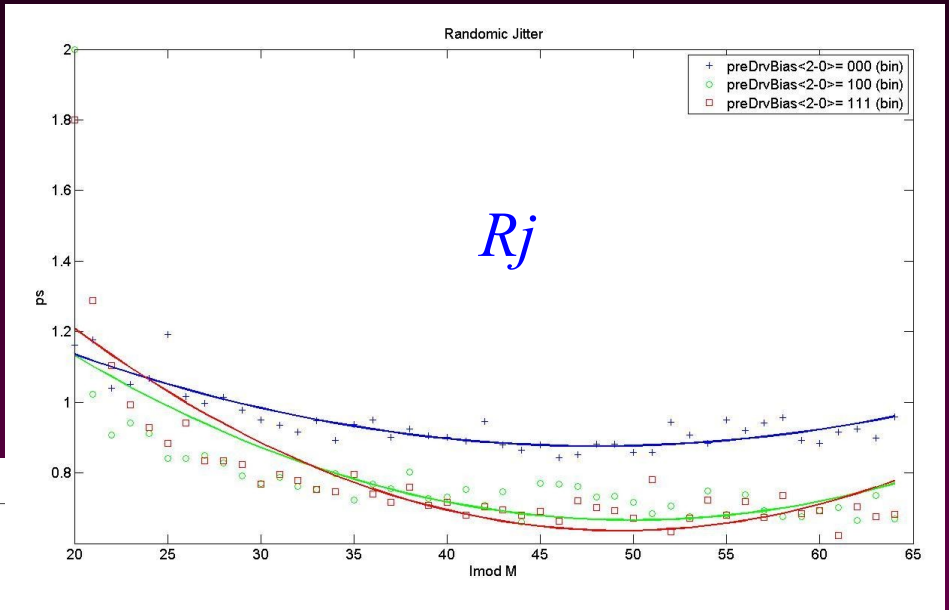
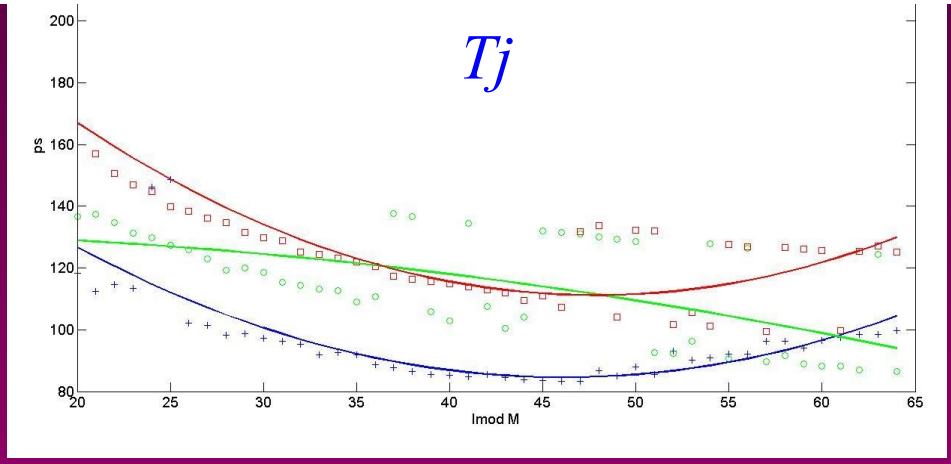




Total Jitter



@ 5 Gb/s

Input range

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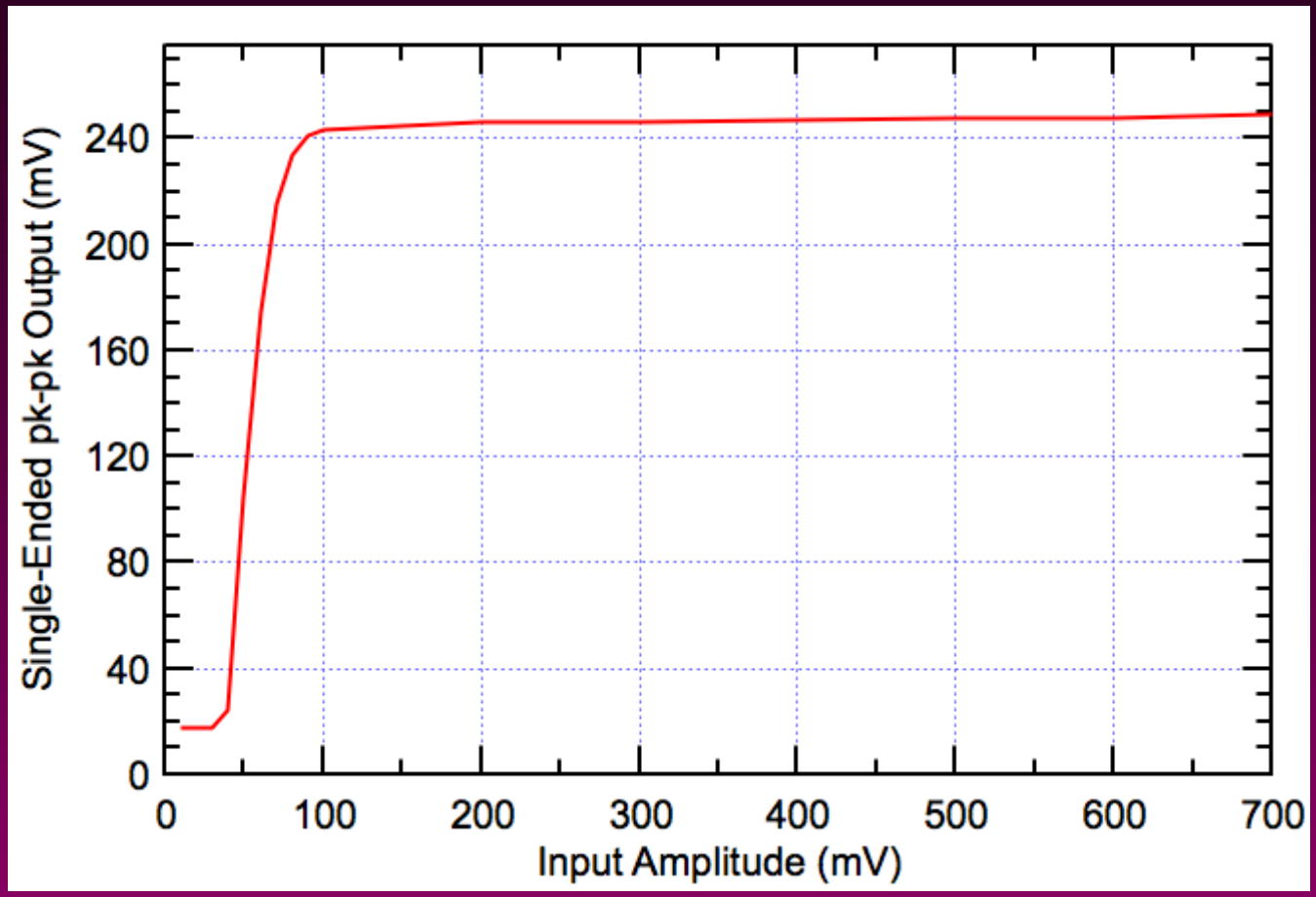

DACs linearity

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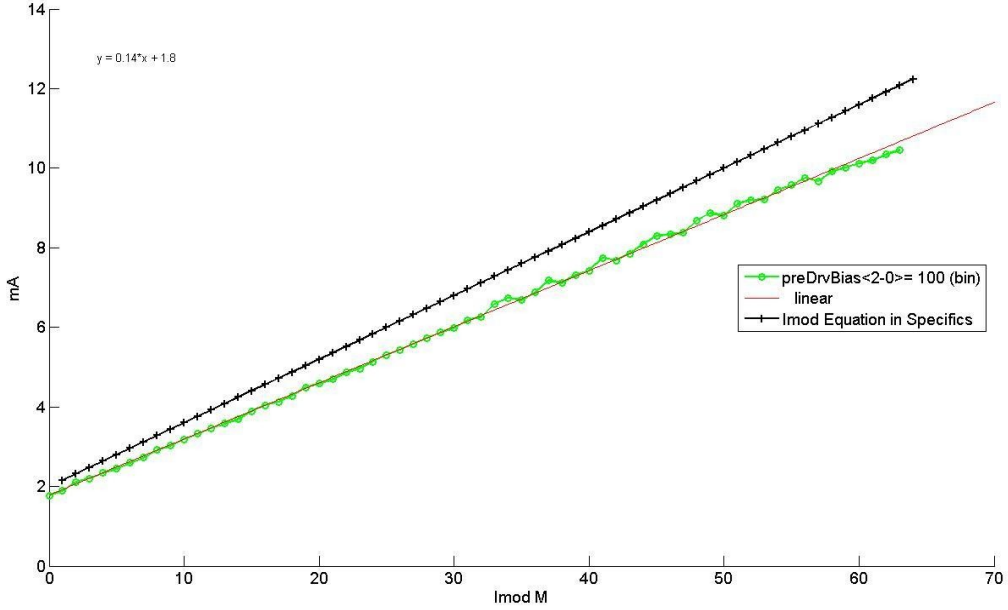
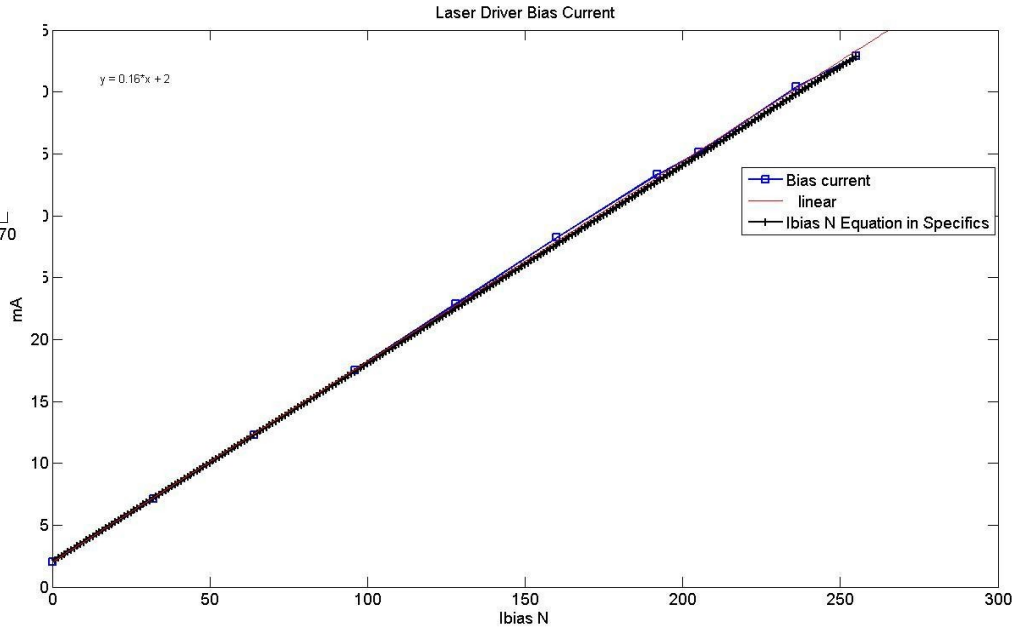


$$I_{MOD} = 0.142 \times M + 1.9 \ [mA]$$

$$I_{BIAS} = 0.158 \times M + 1.8 \ [mA]$$



Tests with pre-emphasis

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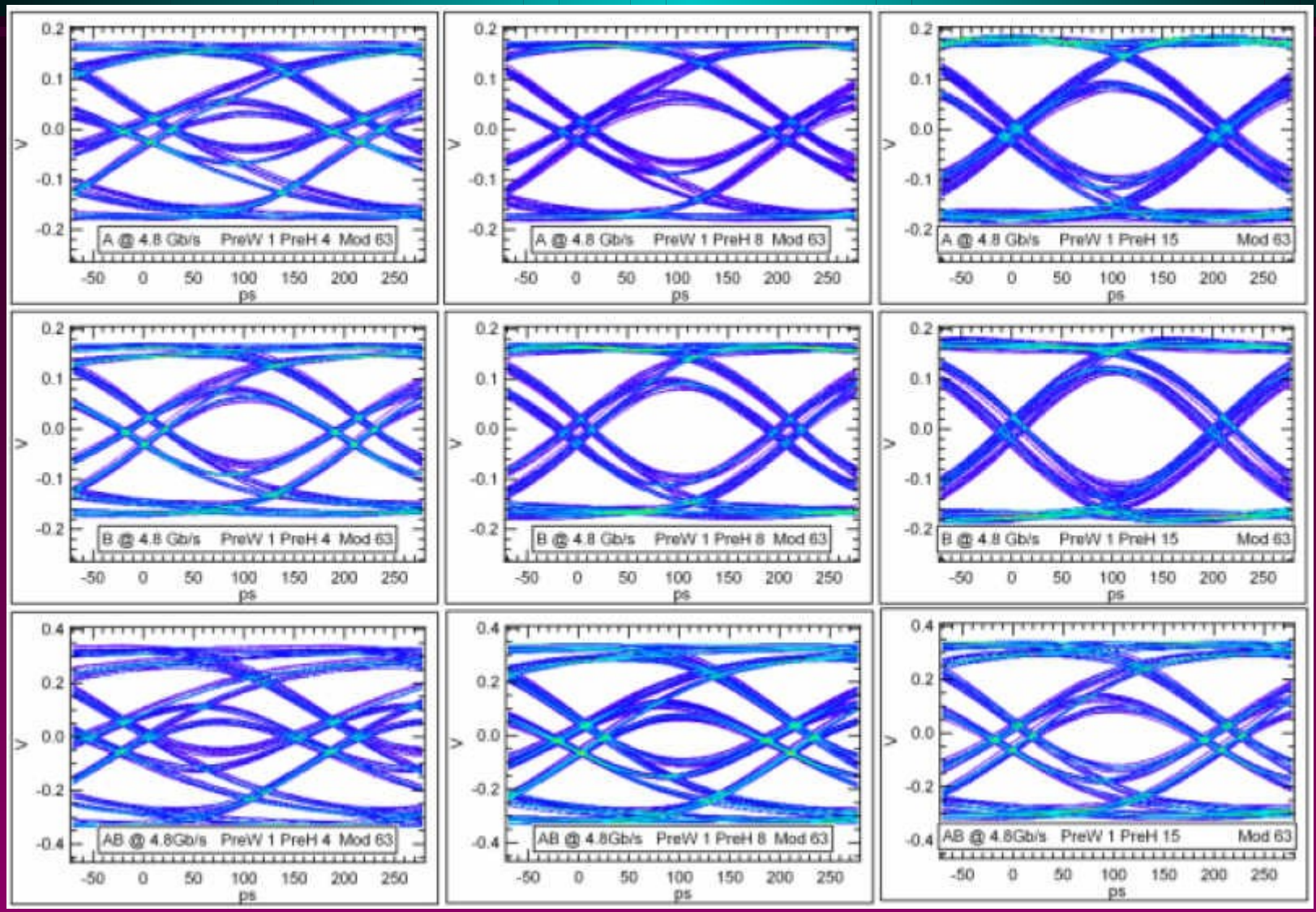
A *4.8 Gb/s*

B *4.8 Gb/s*

A+B *4.8 Gb/s*



Test with VCSEL

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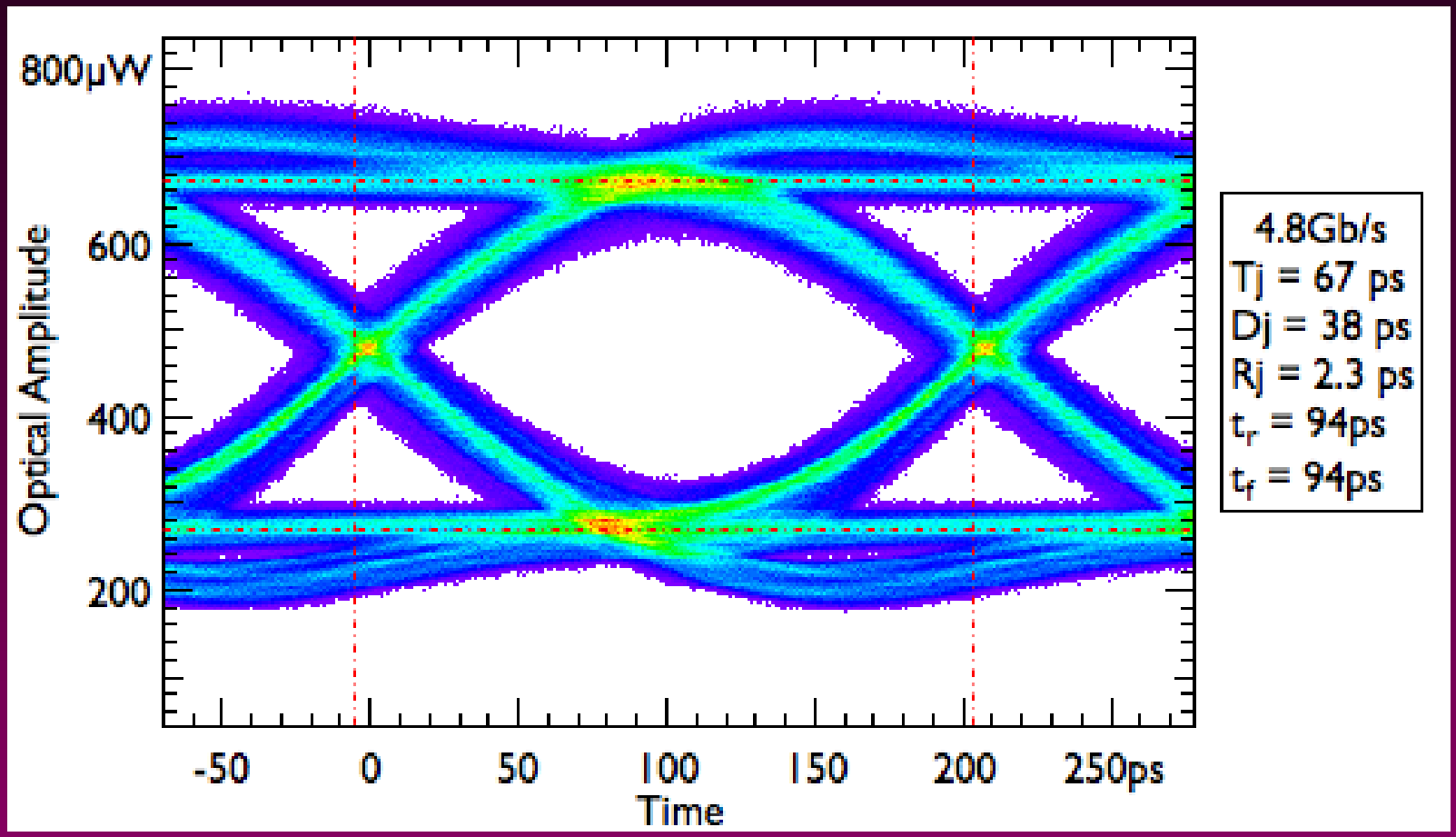

Conclusions

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- A 5 Gb/s laser driver in CMOS 0.13 μm technology has been designed and tested.
- The prototype is functional but does not have enough bandwidth - 5 Gb/s operation possible only with max pre-emphasis
- Performances not yet acceptable...

  ...but not so far from specs.
- Problems in parasitic capacitance evaluation and layout symmetry have been recognized.
- A new version submission is planned for November 2009