ECAL Online Software

- Status
  - New JINF-E software loaded and under test on FS Crate
  - No modification to EDR software and to Configuration files foreseen
- Test
  - Mixed mode A&B DAQ
  - Stand-alone Trigger performance studies
  - Final check of DSP code and configuration files loaded on FLASH memories

ECAL ESS – A&B DAQ Tests

- Detector's electrical configurations fully tested (since ESTEC):
  - ERPD Side A powering 2 Full Crates + FEEs
  - ERPD Side B powering 2 Full Crates + FEEs
- Mixed DAQ (two different sub-sets of the DAQ nodes powered on the opposite Sides) not yet tested
  - Require both +28V inputs of the ERPD to be feeded
  - Allow a full test of the DAQ chain/programs

- Test proposal:
  - JINF-E-x A-side and EDR/ETRG B-sides
  - JINF-E-x B-side and EDR/ETRG A-sides

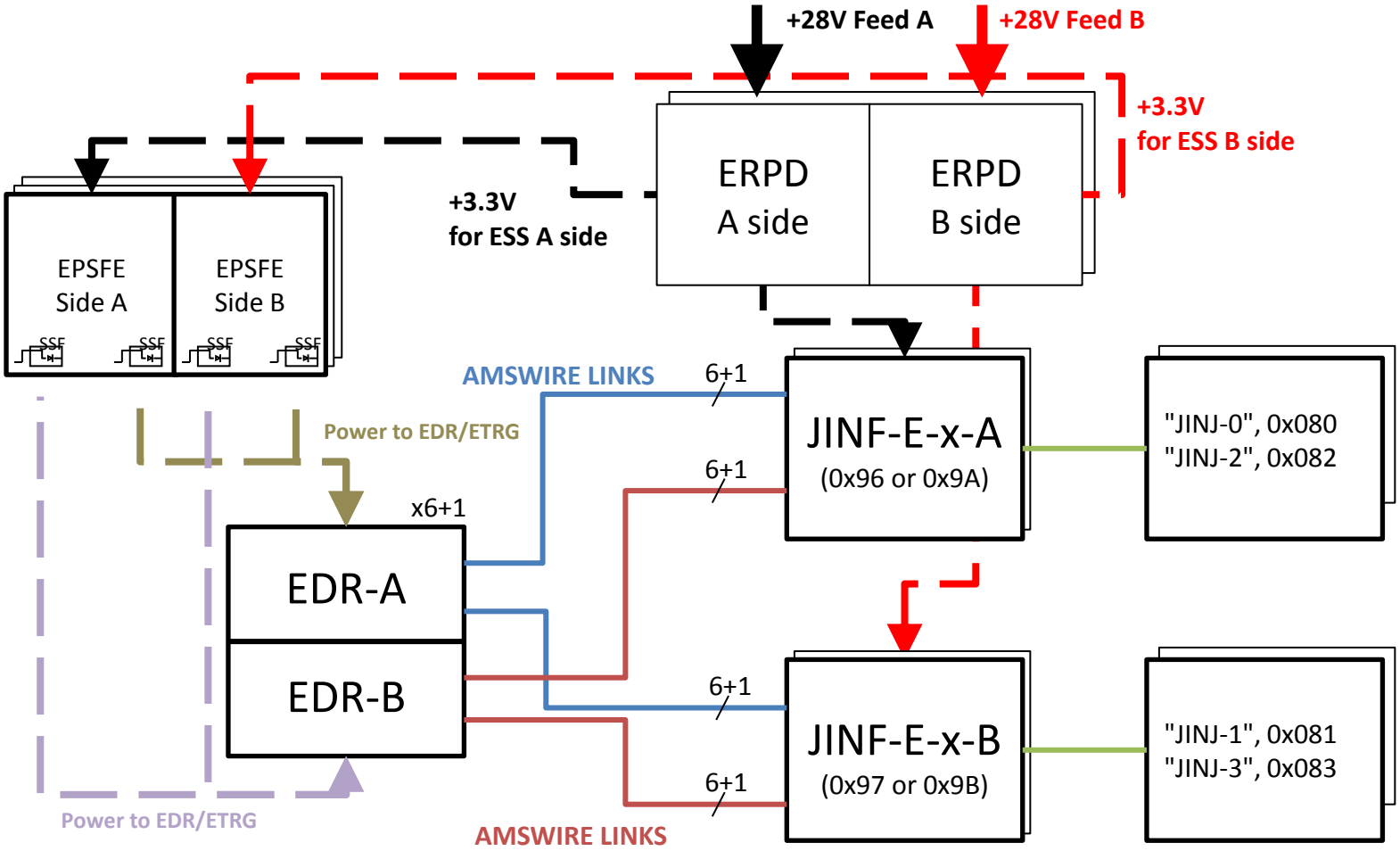
- Requirements:
  - Commands to PDS to have all the ERPD's outlets activated
  - Set of CONFIGURATION commands to change electrical configuration (no changes to config. files in the nodes' flash memories) - scripts ready and tested on FS
  - Change the DAQ config. from whishlist program
  - TESTs don't affects other detectors

ECAL ESS – Standalone Trigger Studies

- Noise induced by RICH
  - When RICH is included in DAQ, ECAL fast trigger rate seems to increase
  - Possible Noise induction from RICH Reset Signal
  - Requires: RICH to deactivate RESET Signal
- RESET delay in ETRG boards
  - Currently default value is 2µsec
  - Change the parameter value (0x0103) to complete trigger efficency studies
  - TESTs don’t affects other detectors

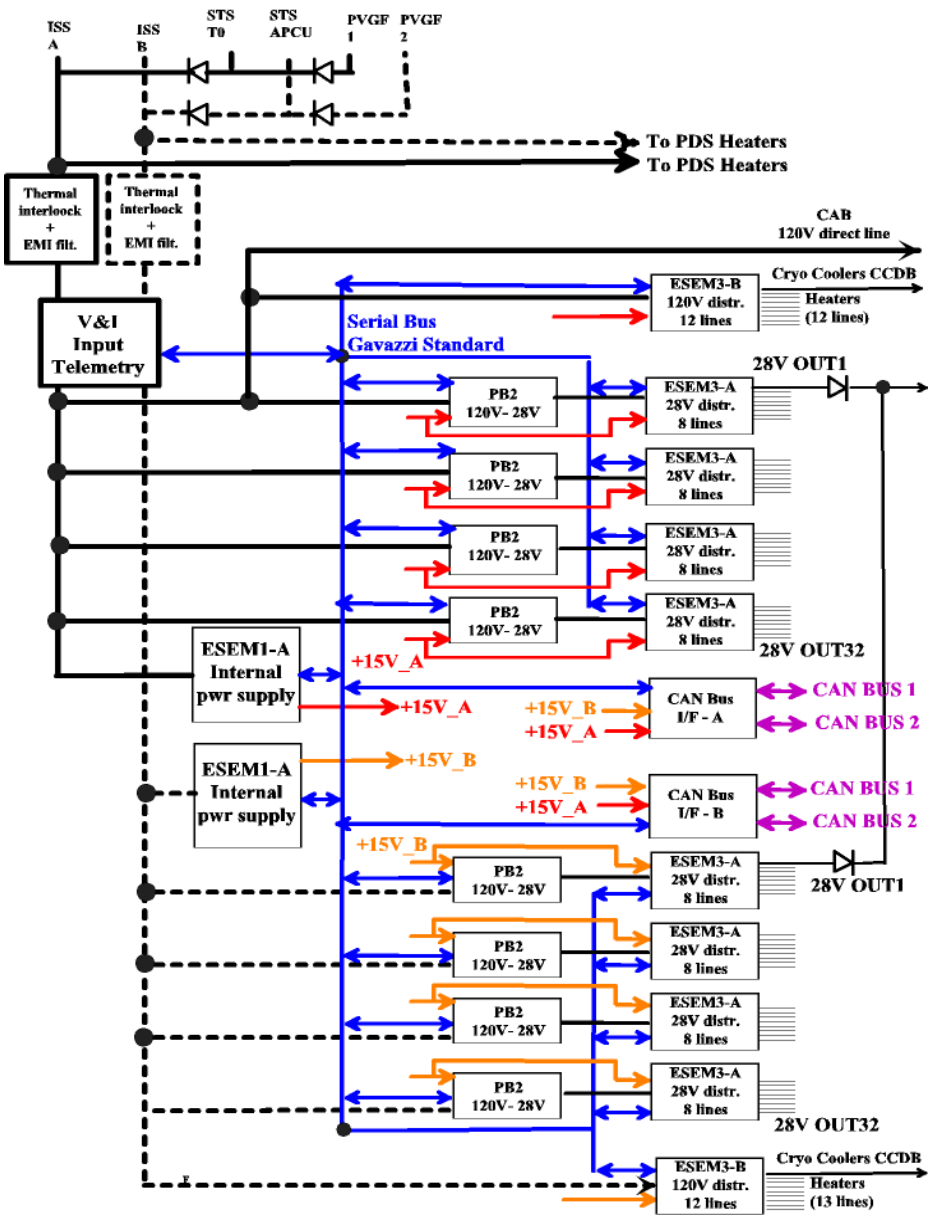
Spares

ECAL DAQ System Redundancy
Block diagram



<u>No DAQ from B side if no power from +28V-B line</u>

PDS Electrical Architecture



- 32 +28V outlets using 4 ESEM3-A board
- each outlet can be powered from both A and B PDS sides
- +28V ERPD feeds:

LINE	Board	Outlet
ER0_N	6	3
ER0_R	8	4
ER1_N	4	1
ER1_R	8	2

- **1 PDS side feeds both ERPD sides**