Contribution ID: **437** Type: **oral presentation**

Simulations and Prototyping of the LHCb L1 and HLT Triggers

Wednesday 29 September 2004 15:40 (20 minutes)

The Level 1 and High Level triggers for the LHCb experiment are software triggers which will be implemented on a farm of about 1800 CPUs, connected to the detector read-out system by a large Gigabit Ethernet LAN with a capacity of 8 Gigabyte/s and some 500 Gigabit Ethernet links. The architecture of the readout network must be designed to maximise data throughput, control data flow, allow load balancing between the nodes and be proven to perform at scale. Issues of stability, robustness and fault tolerance are vital to the effective operation of the trigger. We report on the development and results of two independent software simulations which allow us to evaluate the performance of various network configurations and to specificy the switch parameters. In order to validate the results of the simulation and to experimentally test the performance of the readout network in conditions similar to those expected at the LHC, we have constructed a hardware prototype of the LHCb Level 1 and High Level triggers. This prototype allows a scaled evaluation of our design, soak-testing, and an evaluation of the overall system response to the deliberate introduction of faults. The performance of this test-bed is described and the results compared to simulation.

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Session Classification: Online Computing

Track Classification: Track 1 - Online Computing