



Contribution ID: 422

Type: oral presentation

The Architecture of the ZEUS Second Level Global Tracking Trigger

Monday 27 September 2004 14:20 (20 minutes)

The architecture and performance of the ZEUS Global Track Trigger (GTT) are described. Data from the ZEUS silicon Micro Vertex detector's HELIX readout chips, corresponding to 200k channels, are digitized by 3 crates of ADCs and PowerPC VME board computers push cluster data for second level trigger processing and strip data for event building via Fast and GigaEthernet network connections. Additional tracking information from the central tracking chamber and forward straw tube tracker are interfaced into the 12 dual CPU PC farm of the global track trigger where track and vertex finding is performed by separately threaded algorithms. The system is data driven at the ZEUS first level trigger rates <math><500\text{Hz}</math>, generating trigger results after a mean time of 10ms. The GTT integration into the ZEUS second level trigger and recent performance are reviewed.

Primary authors: SUTTON, M. (UNIVERSITY COLLEGE LONDON); ZEUS GTT GROUP

Presenter: SUTTON, M. (UNIVERSITY COLLEGE LONDON)

Session Classification: Online Computing

Track Classification: Track 1 - Online Computing