First Level Trigger using Associative Memories for CMS at Super-LHC

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Acknowledgments to A. Annovi, M. Dell'Orso, P. Giannetti, G. Parrini, M. Vos, F. Vasey

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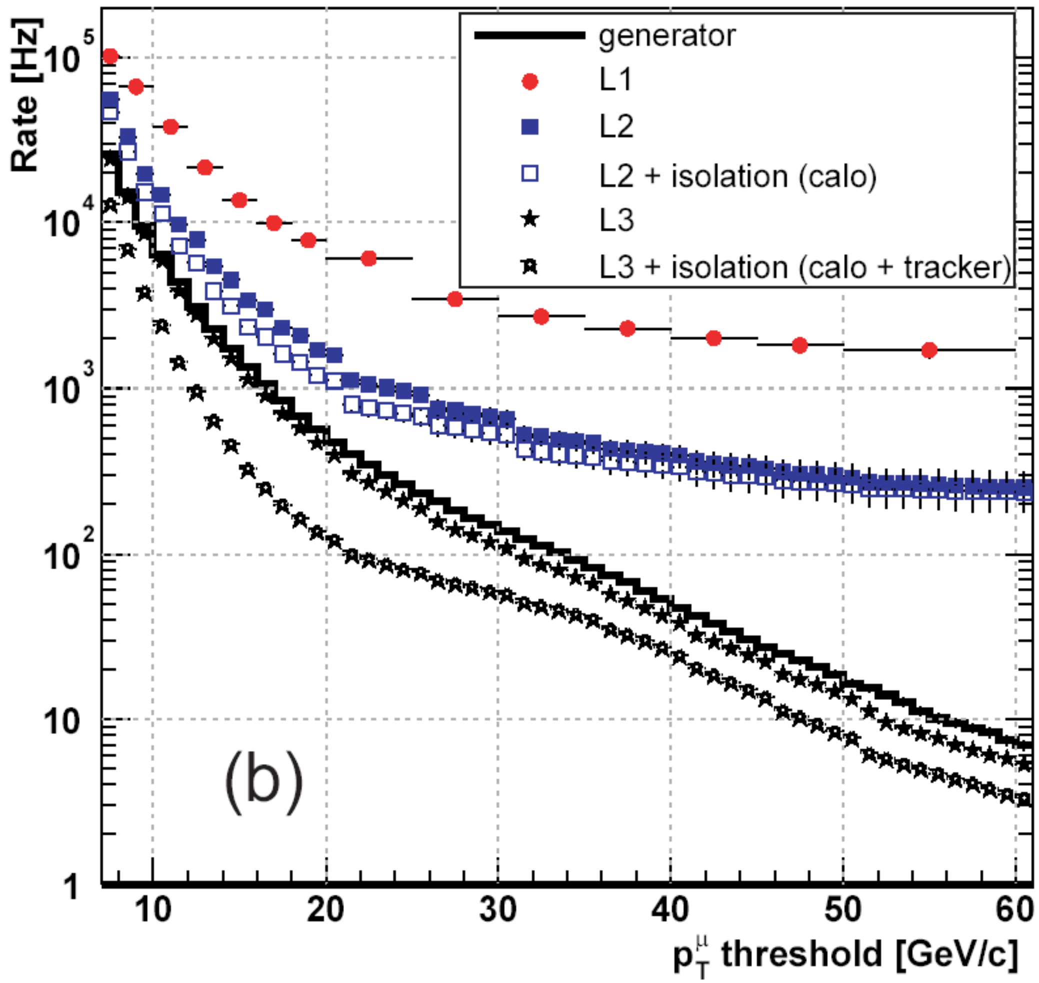
Some issues for SLHC Triggers @ 10^{35}

- ~400 Minimum Bias events/bx (50 ns) [16xLHC]
- Occupancy
  - Degraded performance of algorithms
    - Electrons: reduced rejection at fixed efficiency from isolation
    - Muons: increased background rates from accidental coincidences
  - Larger event size to be read out
    - New Tracker: higher channel count & occupancy $\rightarrow$ large factor, but can be accommodated if digital readout chosen
    - Reduces the max level-1 rate for fixed bandwidth readout.
- Implies raising E_T thresholds on electrons, photons, muons, jets and use of less inclusive triggers
  - Need to compensate for larger interaction rate & degradation in algorithm performance due to occupancy

CMS Muon Rate at $L = 10^{34}$ cm^{-2} s^{-1}

From CMS-DAQ TDR



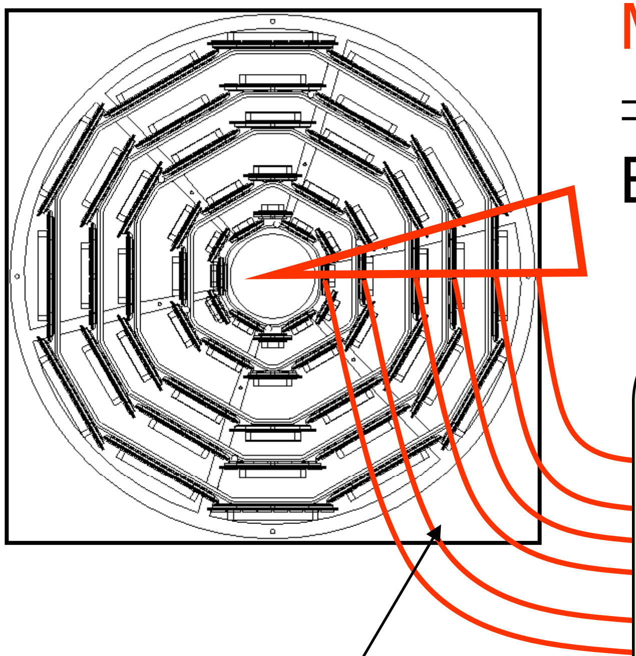
- **Move some HLT algorithms into L-1 or design new algorithms reflecting tracking trigger capabilities**

Note limited rejection power (slope) without tracker information

Tracking Trigger driving ideas

- **Design considerations:**
  - Main usage for p_T reconstruction
    - We need low occupancy and large lever-arm, rather than brilliant space-point resolution
    - If the Tracker material budget will not decrease by a sizeable amount, multiple scattering will drive the momentum resolution below ~10 GeV
  - Use binary readout (0/1) for each channel
  - Avoid duplication of signals to avoid fibers increase
    - Use readout signals for Trigger $\Rightarrow$ move the whole data from the detector out in the barracks
  - Use established detector and electronics technologies to get a robust project, however
    - Push current pixel systems (see R. Horisberger, T. Rohe et al in SLHC CMS workshops)
    - Expand existing (and working) Tracking Triggers (CDF SVT)
    - Profit of miniaturization in electronics (A. Marchioro, transition to 90 nm)
    - More radiation hard optical fibers technologies (F. Vasey…)

Mitigate from CDF SVX approach



Main problem: input Bandwidth (see later)
⇒divide the detector in thin ϕ sectors.
Each AM searches in a small $\Delta\phi$

OFF DETECTOR

1 AM for each enough-small $\Delta\phi$
Patterns
Hits: position+time stamp
All patterns inside a single chip
N chips for N overlapping events identified by the time stamp

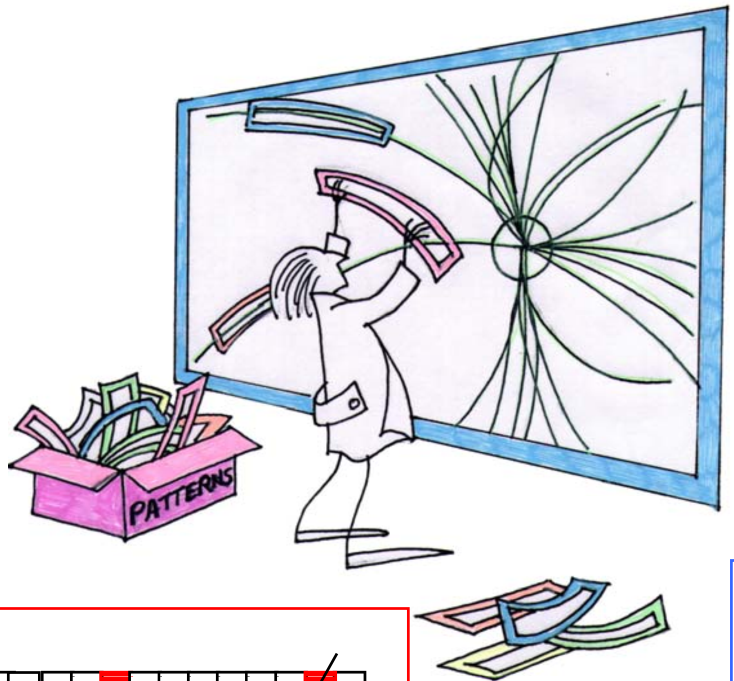
Data links

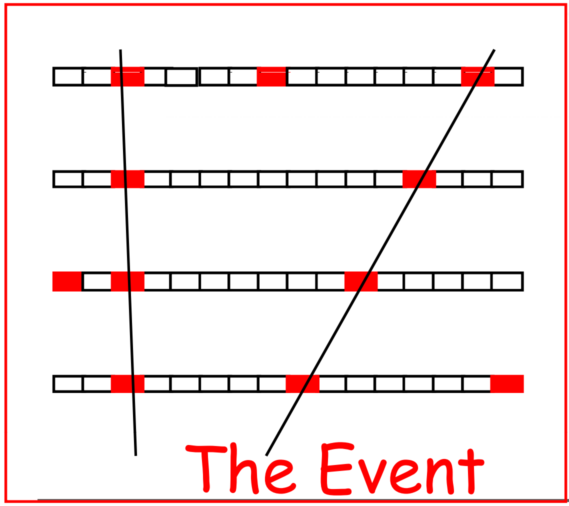
Event1 AMchip1	Event2 AMchip2	Event3 AMchip3	• • • • •	EventN AMchipN

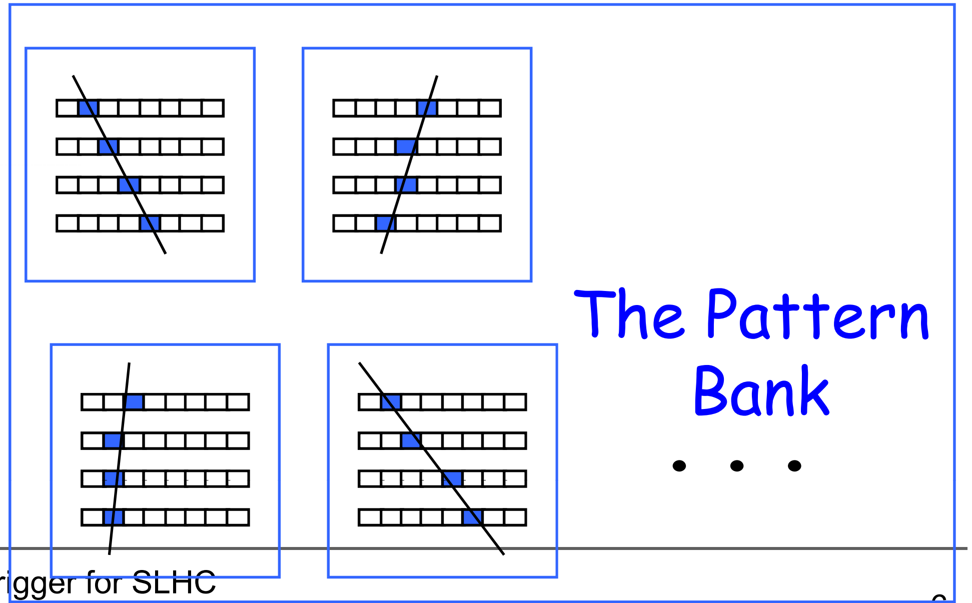
Pattern matching in CDF (M. Dell'Orso, L.Ristori 1985

The pattern bank is flexible set of pre-calculated patterns:

- can account for misalignment
- changing detector conditions
- beam movement
- …







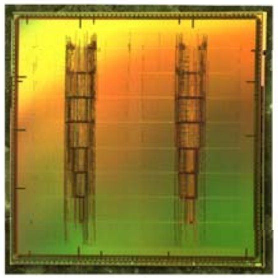
AM chips from 1992 to 2005

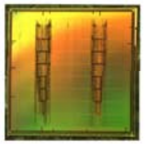
- (90's) **Full custom** **VLSI chip -** 0.7μm (INFN-Pisa)
- **128 patterns, 6x12bit words each**
- **32k roads / wedge**

F. Morsani et al., "The AMchip: a Full-custom MOS VLSI Associative memory for Pattern Recognition", IEEE Trans. on Nucl. Sci., vol. 39, pp. 795-797, **(1992).**

On the opposite side: **FPGA** for the same AMchip

P. Giannetti et al. "A Programmable Associative Memory for Track Finding", Nucl. Intsr. and Meth., vol. A413/2-3, pp.367-373, **(1998).**





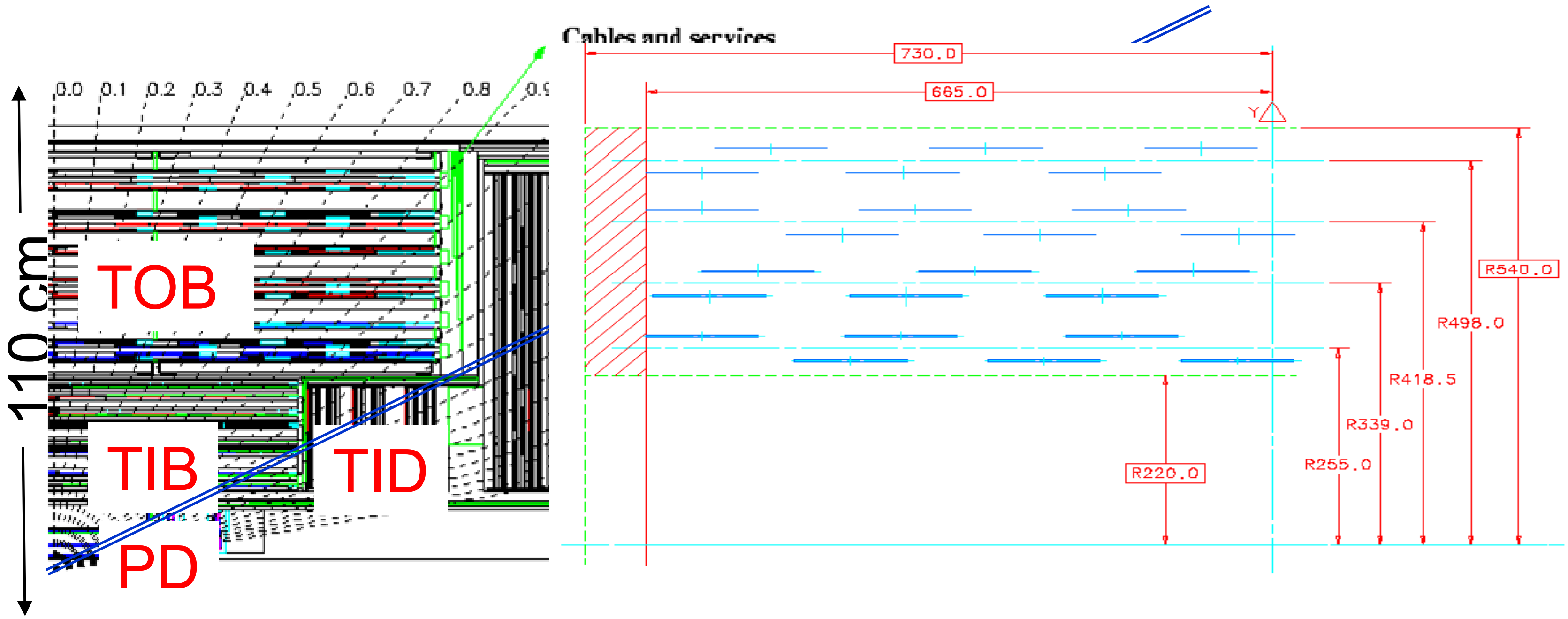
NEXT: NEW VERSION For both L1 & L2

In the middle: **Standard Cell 0.18** μm (INFN-Pisa)→ 5000 pattern/chip AMchip

L. Sartori, A. Annovi et al., "A VLSI Processor for Fast Track Finding Based on Content Addressable Memories", **IEEE Transactions on Nuclear Science**, Volume 53, Issue 4, Part 2, Aug. **2006** Page(s):2428 - 2433

CMS Tracker Trigger Layout a feasibility study

- **As a study, limited to the same barrel region as for the current inner Silicon Strip Tracker barrel (TIB)**
    - **TOB should also be included, for much reduced number of hits, however not in this study**
  - **4 layers with radii at 26, 34, 42, 50 cm from the beam line.**
  - **Barrel coverage up to $|\eta|<1.5$**

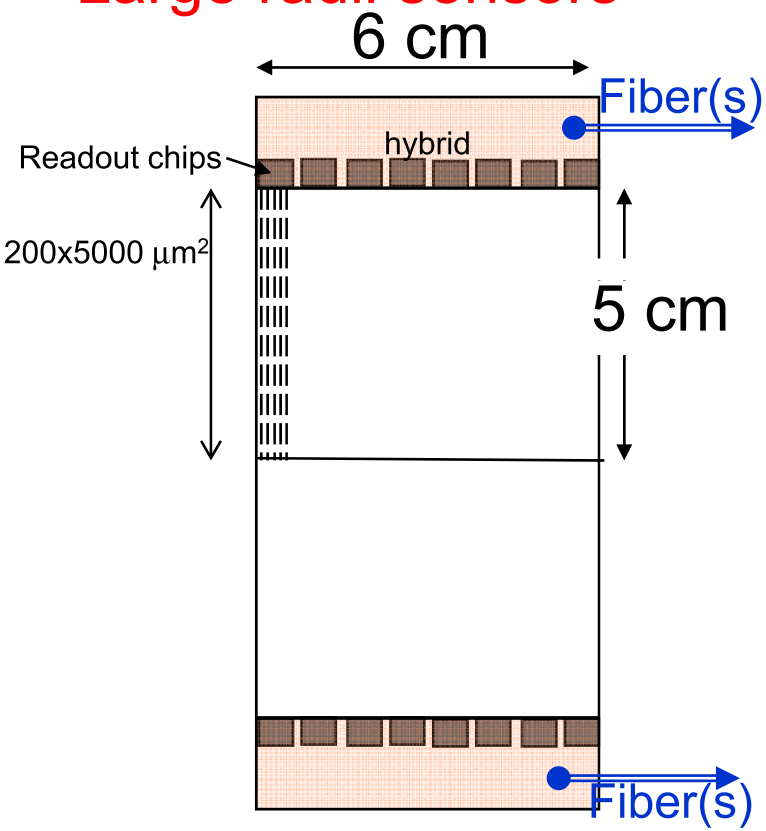


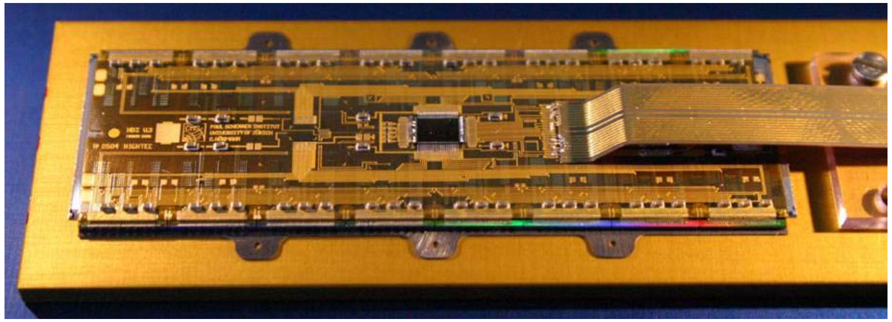
A possible Inner Tracker Layout

- Granularity and costs driven approach
  - Long fibers (~100 m) and high speed (>2.5 Gbps) to extract signal off detector
- Pixel System for radius at 26 cm
  - Single sided pixel detectors, n^+ on p – Silicon (Czochralski) Pixel area ~ 160 μm x 650 μm
  - Sensor area 2 (r-ϕ) x 8 (z) cm^2
  - 1 - 2 fibers/module for 5 Gbps
- Pixel System for radii at 34, 42, 50 cm
  - Silicon strips (actual) have sensor element area of 10 to 15 mm^2
  - 10 fold increase in the luminosity would need a 10 fold decrease of it
    - Large elongated pixels of 200 μm x 5 mm
    - Sensor area 6 (r-ϕ) x 12 (z) cm^2
    - 3 - 4 fibers/module for 5 Gbps

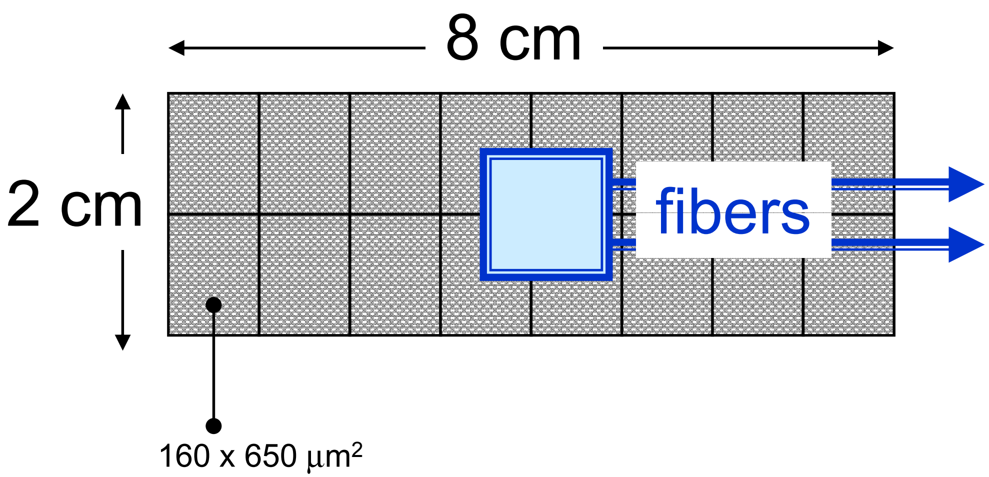
Sensors and signal routing

Large radii sensors





Current CMS pixel sensors



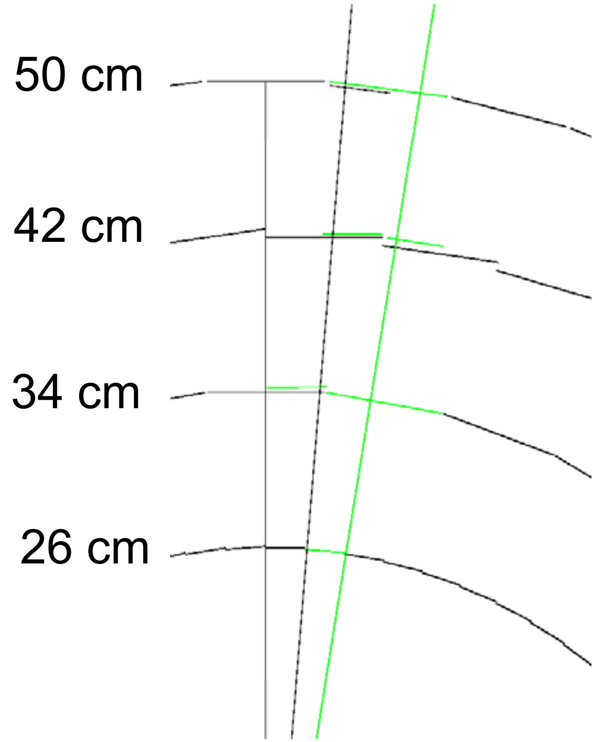
32 bits sufficient to locate pixel position in the sector and bx time stamp

Small radius sensors

From an idea of R. Horisberger http://agenda.cern.ch/fullAgenda.php?ida=a036368

Sector segmentation

- Subdivide the detector in many ϕ sectors
  - Keep data volume limited in each sector
- Combine information from at least 3 layers out of 4 in each sector
  - Momentum resolution of ~ few (<10)% at 10 GeV/c
  - Granularity driven by the minimum measurable p_T for triggering purposes, without loosing efficiency
    - ~80 ϕ sectors at the innermost radius
      - $\Delta\phi$~ 4.5° matches to a module of 2 cm width
      - Well covering the bending of a track of 5 GeV p_T and above
    - Larger ϕ sectors with increasing radii
      - Match the sensors widths



Occupancy studies

- **GEANT4 simulation of pixelized tracking layers**
  - **Simulated 3500 minimum bias using latest Pythia settings events and group into chunks of 100 events per bunch crossing and 250 t-tbar events**
  - **Use current CMS layout (and material budget) but different sensors granularity**

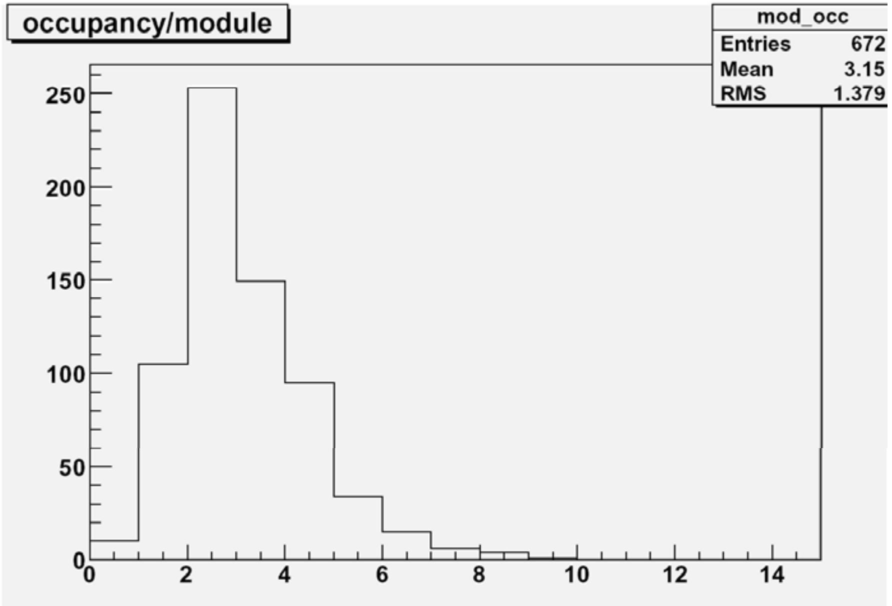
Layer No.	Radius (cm)	Hit/module /bx[a]	No. detectors in ϕ	Data rate*/module (Gbps)	Data rate*/sector (Gbps)	No. data links[†]/layer
1	26	3.1	82	7.9	110	2296
2	34	8.5	36	22	200	1620
3	42	5.3	44	14	124	1188
4	50	3.7	52	10	88	936

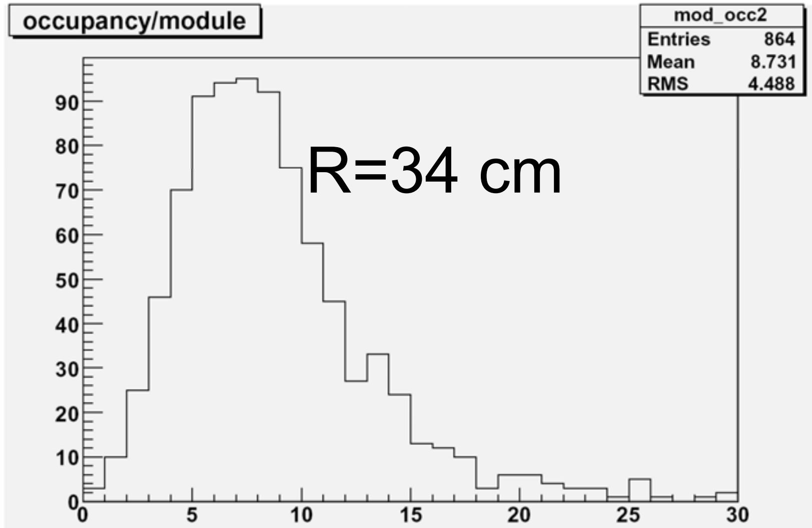
Current links in CMS TIB Silicon Strip: 2000 @ 26 cm - 2600 @ 34 cm

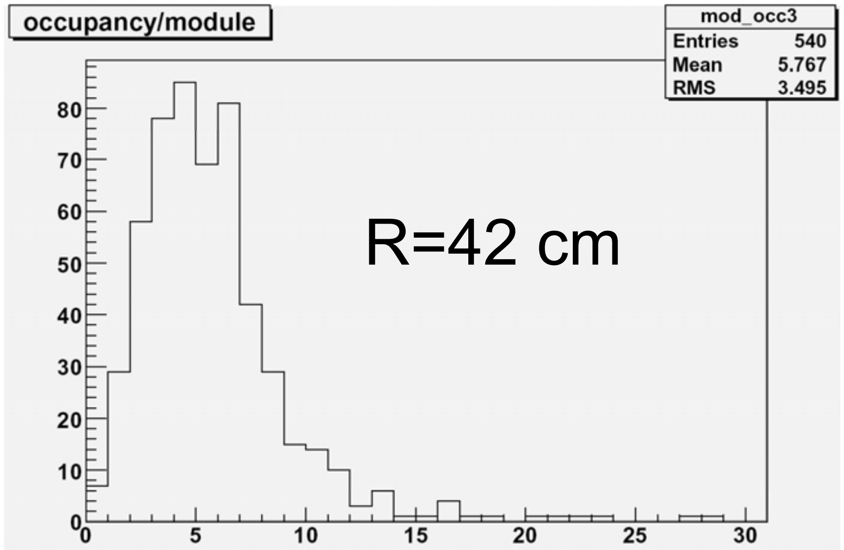
[a] average number on minimum bias events, t-t will contribute on average<<1 hit/det – 12.5 ns bx
It will only double for 25 ns
**32 bits/hit*
[†] for a data link speed of 5 Gbps – does not change with bunch spacing

Number of hits/module/bx

R=26 cm

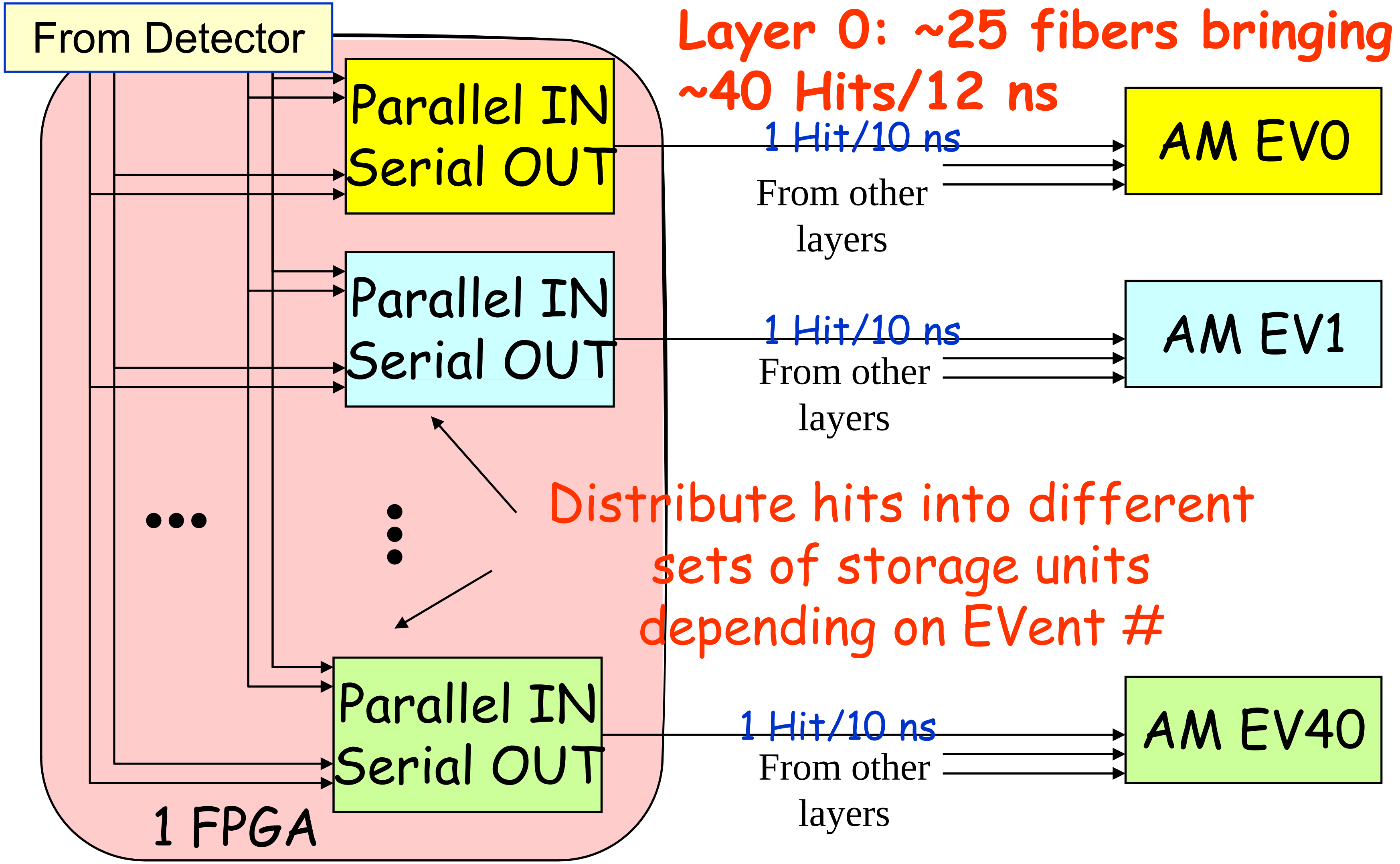






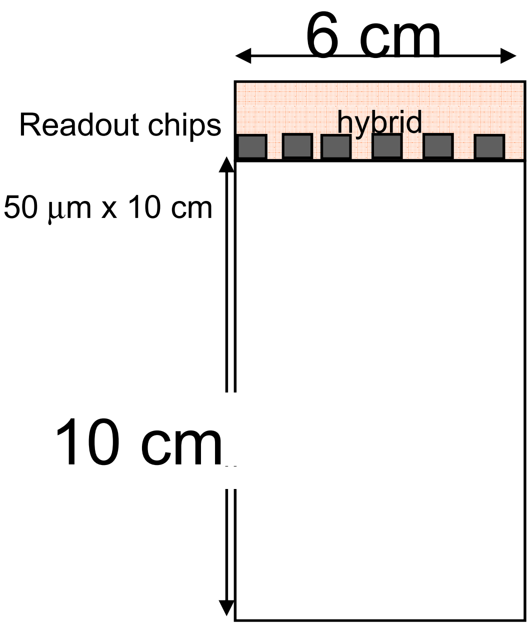
Could accommodate fluctuations using buffers on the detector, or increasing the number of fibers

Conceptual design



Pushing to outer radii

- **Extrapolating the previous layout to outer radii could improve the momentum resolution increasing the lever arm.**
  - **Z coverage up to ±130 cm (for TIB-like configuration up to ±55 cm)**
  - **In order to cover the bending of muons of at least 10 GeV p_T need to consider trigger sectors in phi made by two sensors.**
  - **Proposed cell dimension ~6-8 times smaller wrt the current (CMS) one**
    - **See also next slide for the pitch choice**



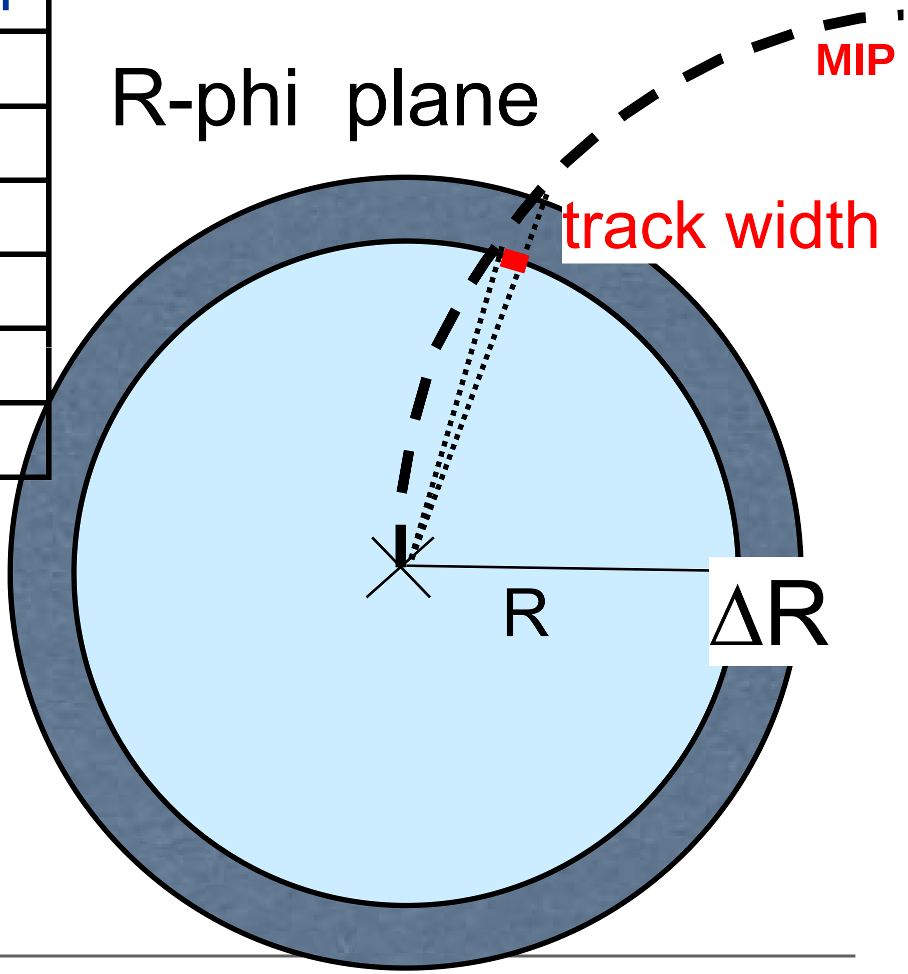
Radius (cm)	No. detectors in ϕ	Data rate* trigger/module (Gbps)	Data rate*/sector (Gbps)	No. data links†/layer
60	63	3	117	1300
70	73	2	86	1500
80	84	2	66	1700
90	94	1	52	1980

Current links in CMS TOB Silicon Strip: 1300 @ 60 cm – 6000 overall

Using the cluster width to reduce trigger data rate

G. Parrini
INFN - Florence

p_T (GeV/c)	Cluster width (μm) for a sensor thickness of 300 μm			
	R= 0.6m	R= 0.7m	R=0.8m	R=0.9m
1	116	139	164	192
2	55	64	74	84
3	36	42	49	55
4	27	32	36	41
5	22	25	29	33
6	18	21	24	27



- In this region, using 50μm pitch, about 3% of the total particles leave cluster sizes with ≤2 strips: ~ 3 GeV pT

- **It could be used for reducing the information for triggering purposes of more than one order of magnitude, leaving the rest (AM) untouched.**

- It would need dedicated ASIC on silicon module.
- Once reduced to ~100 KHz, it would only need few fast readout links to readout the entire Tracker

Efficiency, latency and power

- To increase efficiency in ϕ coverage could send the same fiber to more than one sector
  - Could accommodate more external layers if needed, to reduce ghosts and increase momentum resolution

- Latencies
  - ~100 m fiber 300 ns [24 bx]
  - Switch + AM ~1μs [80 bx]
  - Sensor read-out latency budget should be less than ~80 bx
  - TOTAL ~ <200 bx [1.75 μs]

- Power consumption (R=26 cm, largest density) from laser drivers
  - Largest consumption innermost modules
    - ~1W/module $\Rightarrow$ ~100 mW/cm^2.
  - Current systems (CMS) from pixel ROCs ~ 200 mW/cm^2.

Board dimensions and costs (P. Giannetti et al)

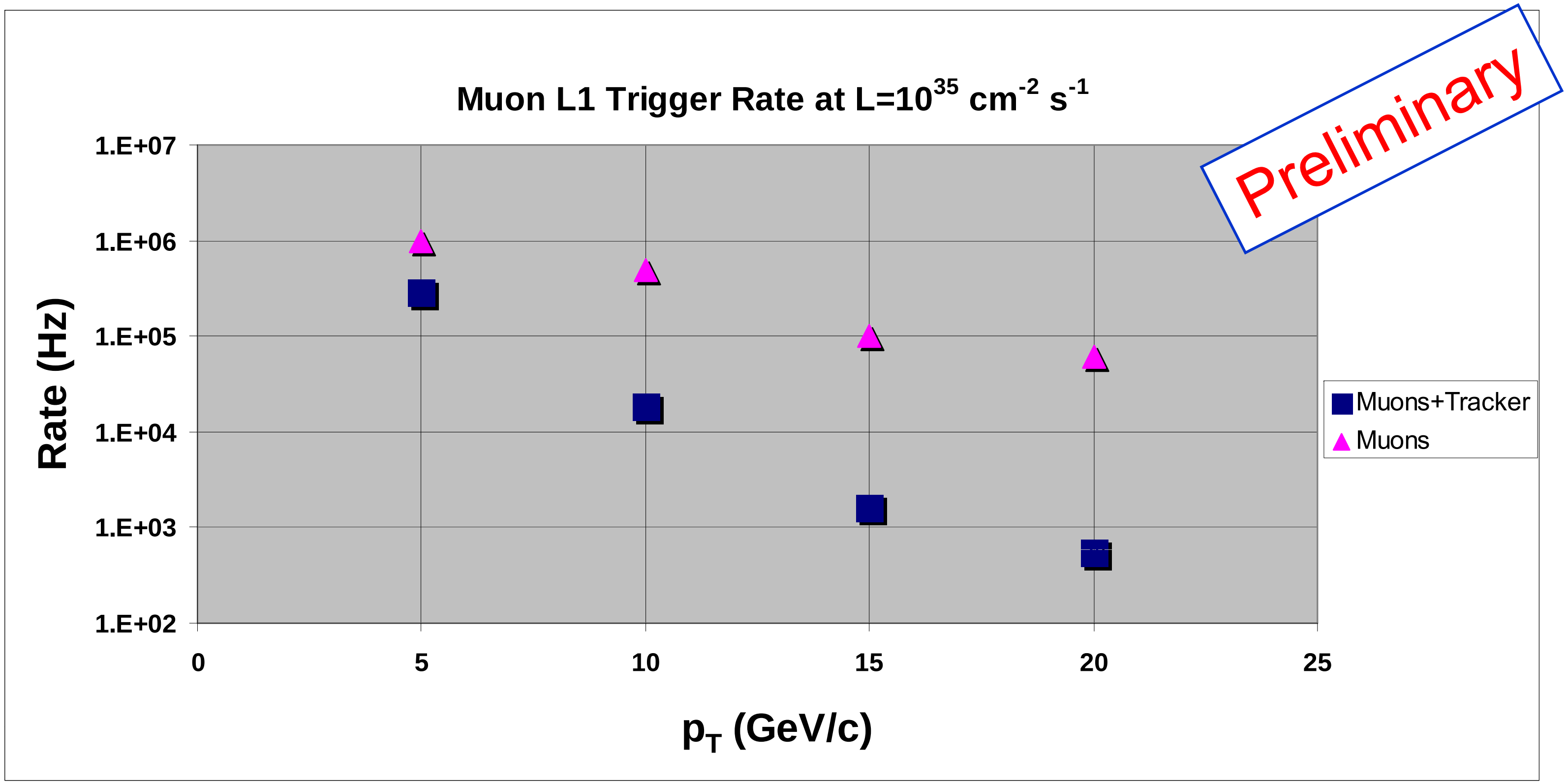
Board dimensions

- About 30,000 patterns per AM chip required
  - Needed ~ 80 boards with ~40 AM chips each
    - 3200 AM chips
- The current AM for CDF holds ~5000 patterns/6 planes in 0.18μm technology
- If developed in the 90 nm technology one could accommodate ~4 times more patterns/AM chip hence 30,000 for 4 planes

- **A batch with 3000 AM chips (yield of 75%) costs 30k$**

Muon Trigger Rate

- Estimate of the L1 Trigger rate for different p_T
  - Assume very simple Tracker Trigger finding algorithm
    - No isolation required
  - Correlate with estimated L1-Muon alone



Conclusions – I

- A conservative approach to a Tracker based Trigger for SLHC based on the existing technologies has been presented
  - Very precise “pixel” layers at intermediate radii (25 to 50 cm)
    - Relies upon “standard” detector technologies
    - Limits the data volume to be transferred
      - Readout buffers could be useful to accommodate fluctuations in the number of hits/event
    - Small power density compared to innermost layer based approaches
    - Very simple digital readout
  - Simulation suggest usage of the outermost layers (TOB) could be used
    - Higher lever arm
    - Lower data rate especially when cutting low pt tracks using cluster width information
  - High speed radiation-hard links very likely available for SLHC
    - Allow off-detector track reconstruction
    - Use same fibers for Trigger as well as for read-out
      - Data link reduction
      - Challenging, need further R&D

Conclusions – II

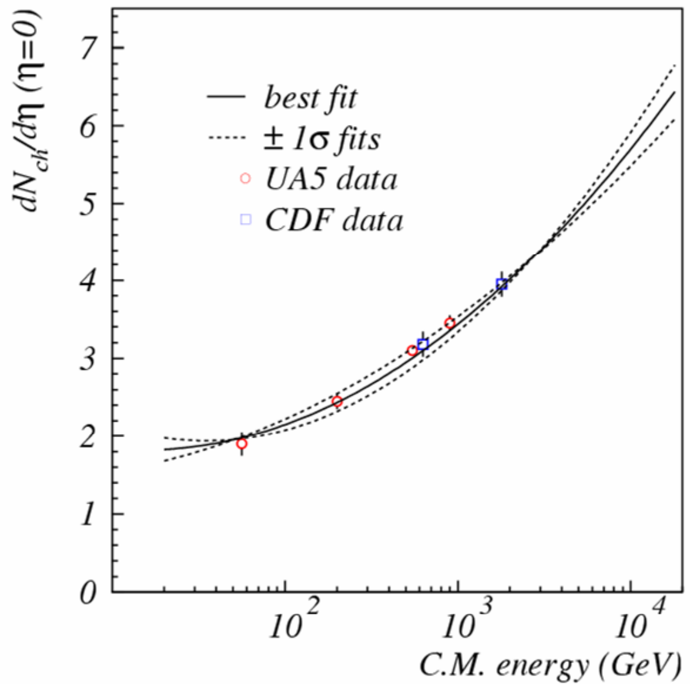
- Full track reconstruction using parallel processing
  - Use
    - current efforts to extend positive CDF (SVT) experience
    - Foreseen electronic miniaturization
    - Heavily based on fast switches. Need R&D
- Used in conjunction with other "traditional" (e,μ, calo) L1 primitives allows to reduce L1 rate to less than 100 KHz
  - Could put additional processing to look for di-lepton resonances at L1 and more exotica
- Production costs not driven by the Trigger boards

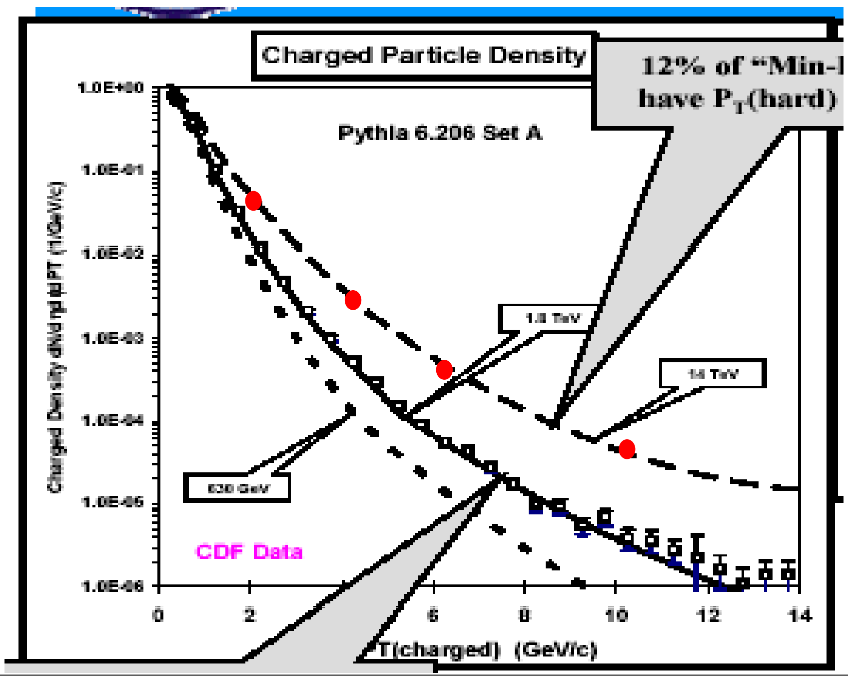
- First starting point, but …
  - Need further R&D
  - Need to be integrated with detector and with mechanics
  - Could we reduce the number of links?
  - Complements inner layers Trigger approach

spare slides

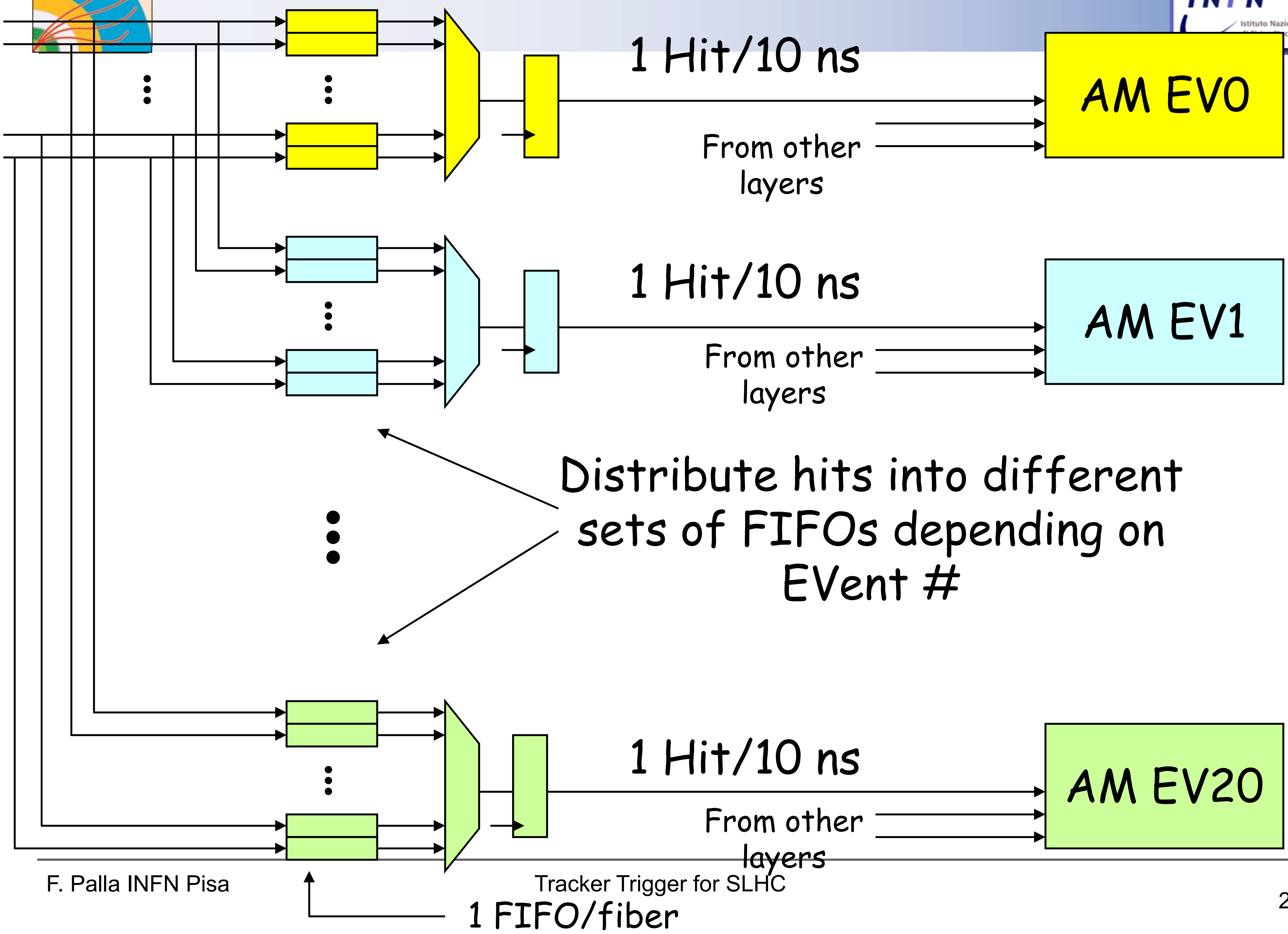
Trigger design (start from Physics!)

- **Main problem is the large number of tracks/bx**
  - **$dN/dy_{|y=0} \sim 6$**
    - **@S-LHC ~2000 tracks/bx in $|\eta|<1.5$**
  - **But only a few ‰ have p_T>5 GeV/c and less if p_T>10 GeV/c**
    - **In principle, triggering on these tracks would give a reduction from 80 MHz to 80 KHz or less, if the fake rate is under control**





Layer 0: ~25 fibers bringing ~20 Hits/12 ns



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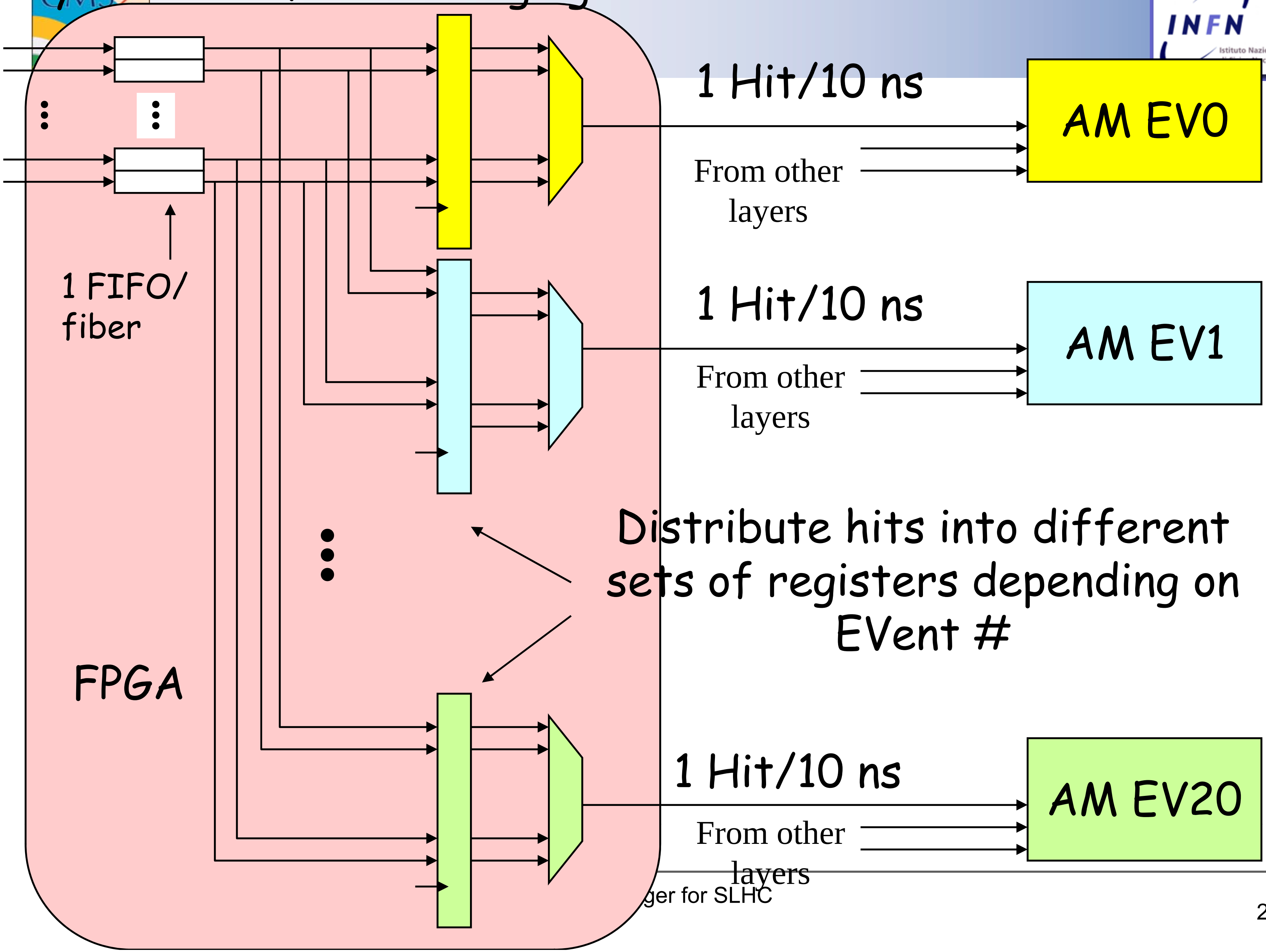

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