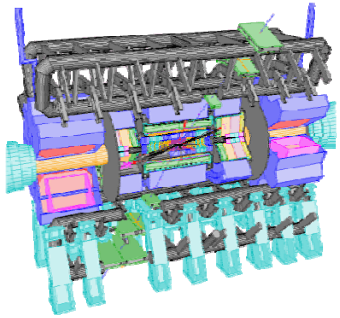


ATLAS LAr Calorimeters

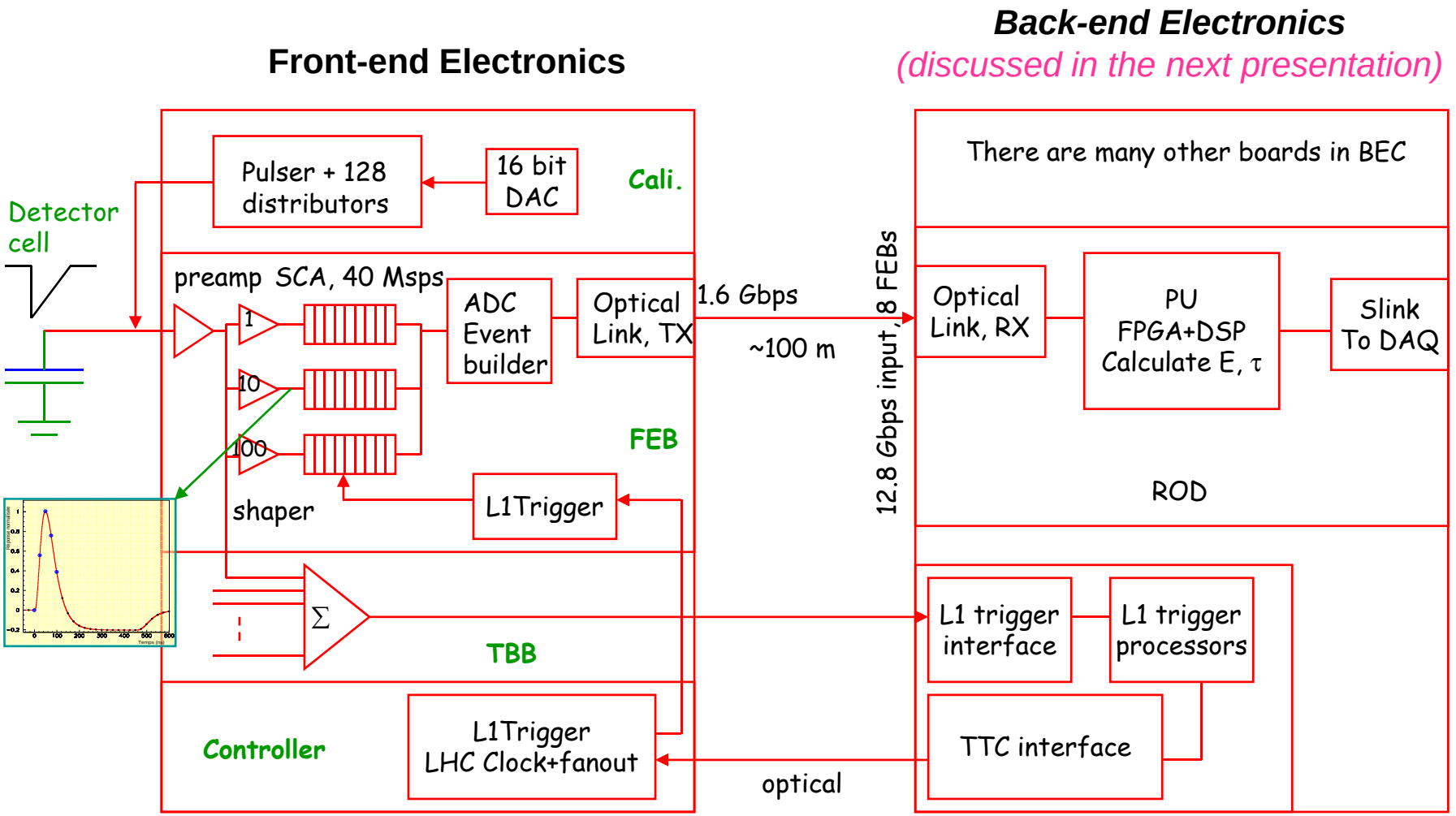
Front End Electronics

Mauro Citterio
INFN, Milan
on behalf of the LAr Community

ACES Workshop, Mar. 19-21/2007

ISTITUTO NAZIONALE DI FISICA NUCLEARE

Overview of ATLAS LAr Calorimeter Readout

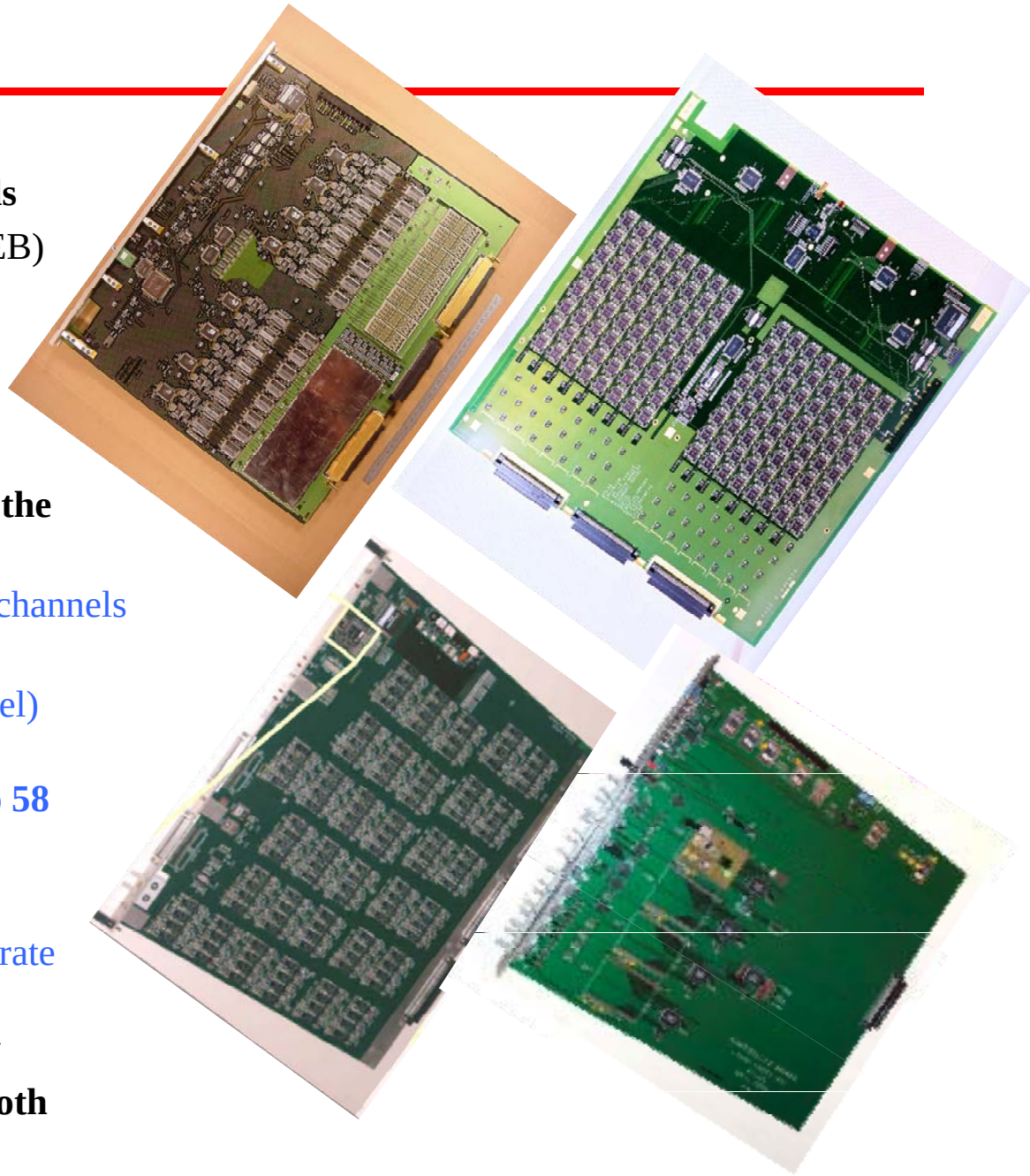


On detector (at warm)

Off detector

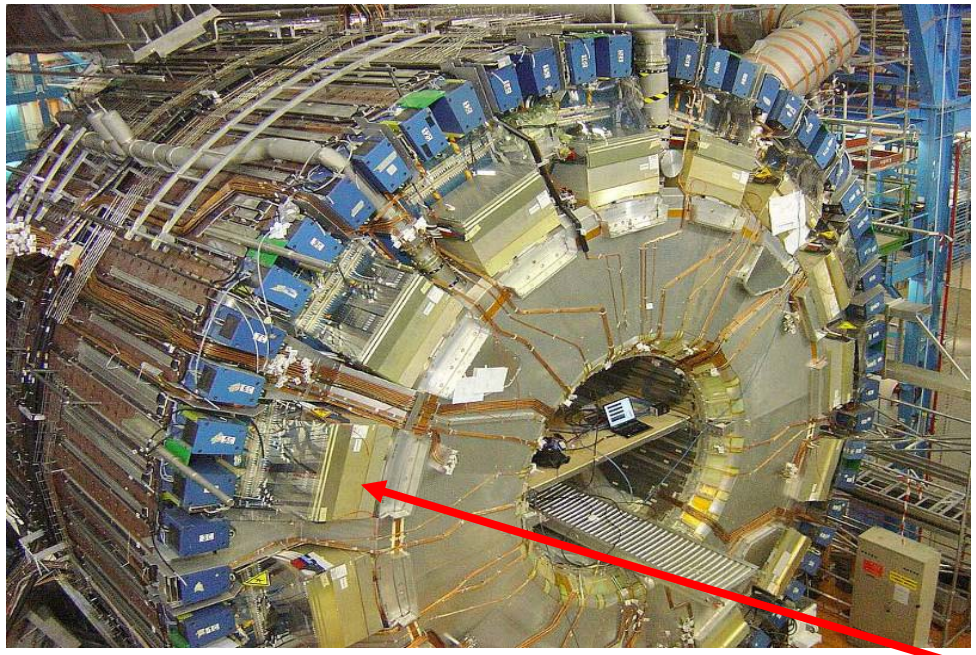
Front End Electronics

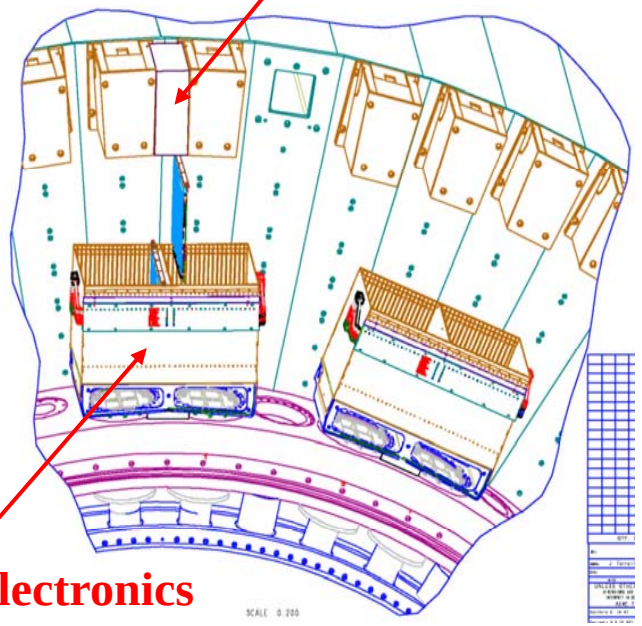
- **Read out ≈ 190k channels**
- **More than 2000 custom boards**
  - 1524 Front End boards (FEB)
  - 124 Tower Builder boards
  - 116 Calibration boards
  - 120 Controller boards
- **The "signals path" is through the FEB:**
  - high channel density (128 channels per board)
  - low power (≈ 0.8 W/channel)
- **The boards are organized into 58 Front End Crates**
  - ~ 36 boards per crate
  - ~ 2.6 kW total power per crate
- **Each board is water cooled by means of plates mounted on both side of the boards.**



Front-End Electronics Location

- **Example: Barrel Calorimeter**



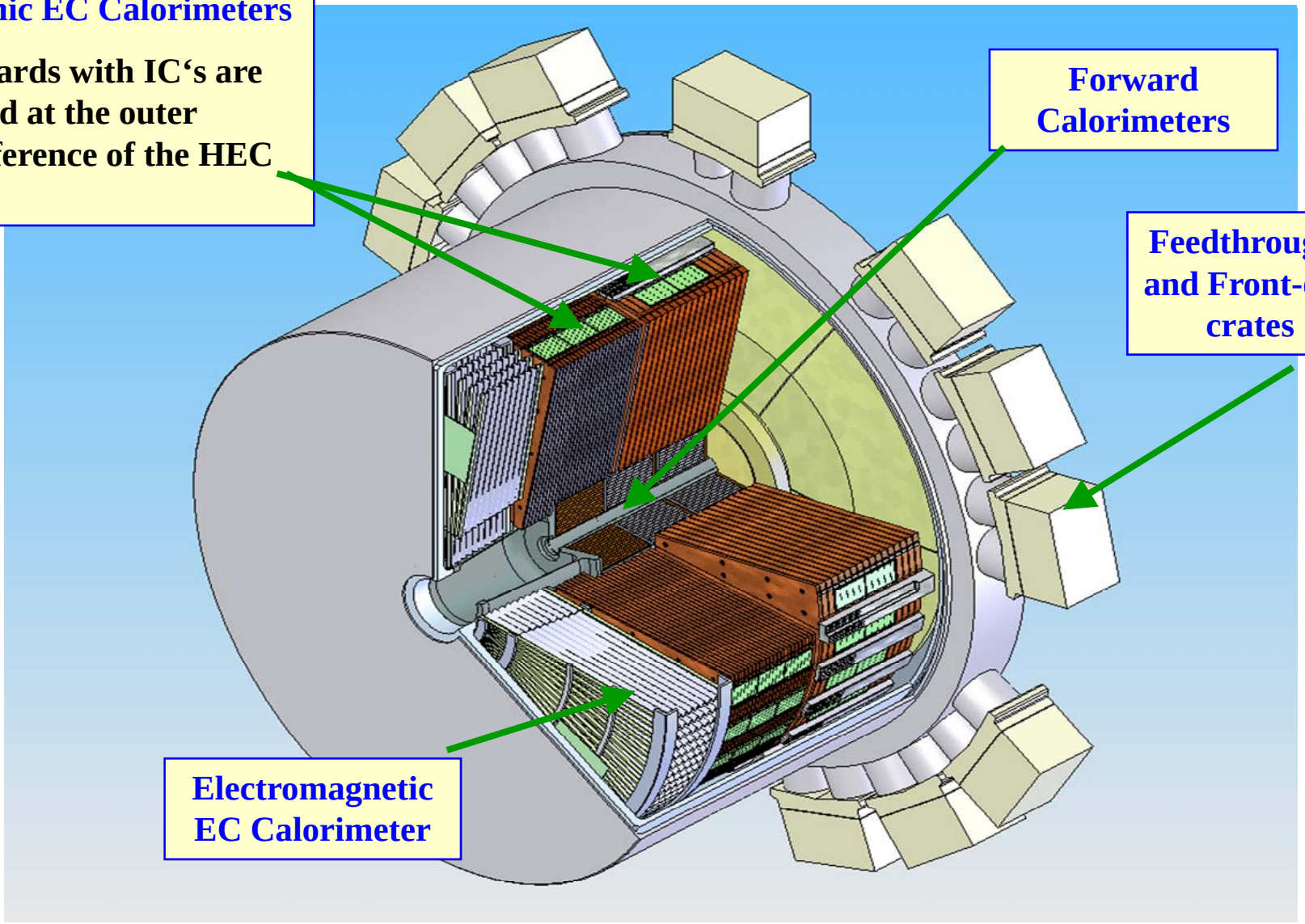


- **Similar location and structure for the End Cap Calorimeters.**
  Note: cold electronics is used for the HEC.

ATLAS LAr End-Cap Calorimeters

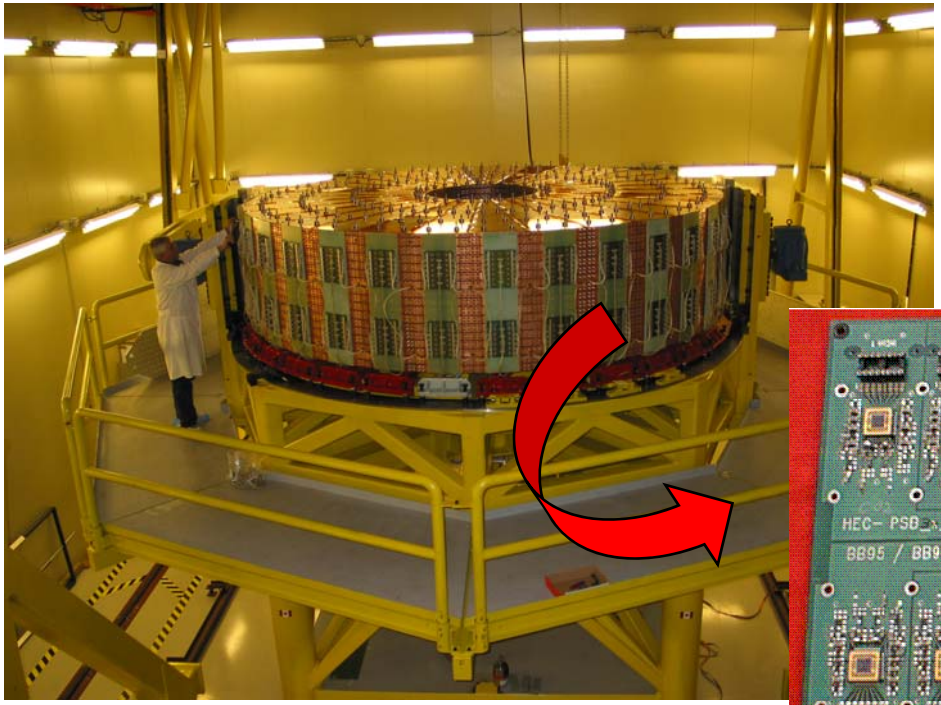
Hadronic EC Calorimeters

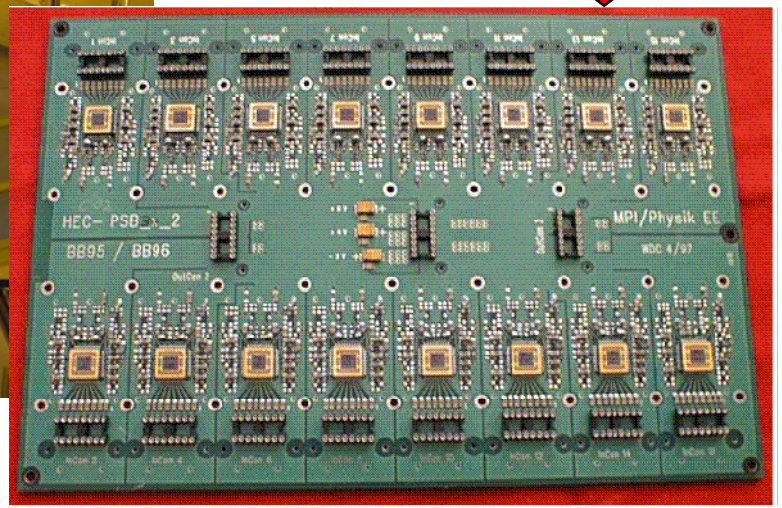
PSB boards with IC's are mounted at the outer circumference of the HEC wheels



HEC Cold Electronics

GaAs IC:
8 preamplifier channels
2 summing amplifiers



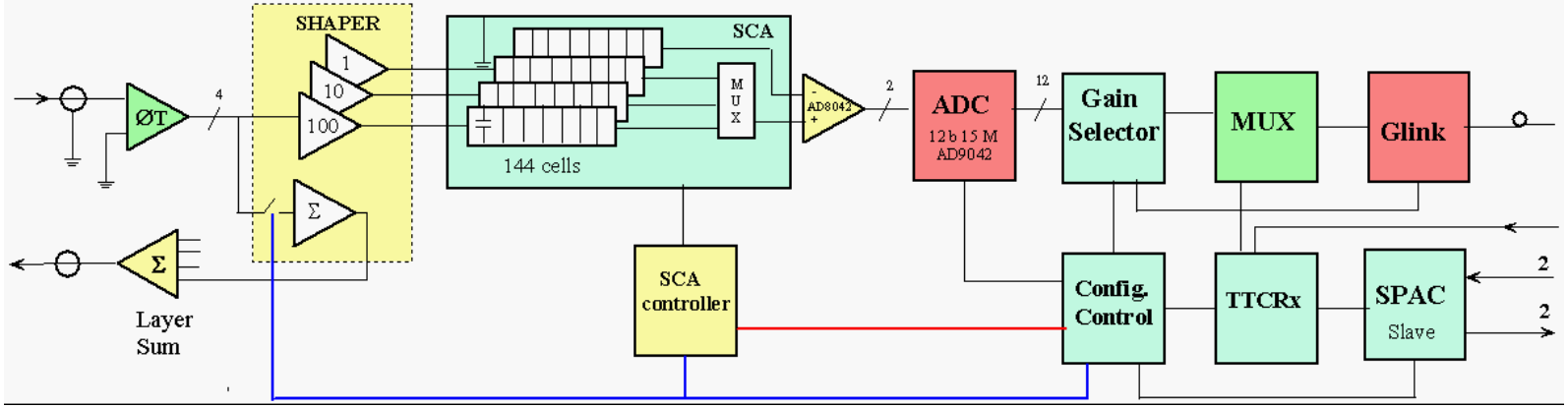


- Concept of ‘active pads‘, i.e. signals from (2/4/8/16) pads are amplified and summed (ASIC) to the required output signals in cold;
- Optimal signal to noise ratio;
- Technology chosen: GaAs TriQuint QED-A 1µm
  Excellent high frequency performance,
  Stable operation at cryogenic temperatures,
  Radiation hard → for LHC operation, at least.

Front End Electronics components …. a "jungle"

- **The present FE electronics has required the development and qualification of 16 custom rad-tol ASICS in various technologies:**
  - **10 in DMILL** (SCA, BiMUX, Opamp, SPAC, CALogic, CONFIG, SMUX, DAC)
  - **4 in DSM (using rad-tol standard cell library)** (SCAC, GainSel, CLKFO, DCU)
  - **1 in AMS BiCMOS**
  - **1 in GaAs IC**
- **Moreover a limited number of COTs are used (preamps, ADC, op-amps, voltage regulators, GLink, line driver)**
  - **Which has required an extensive radiation qualification procedure**
- **The boards are qualified for LHC radiation levels (with safety factors of ~ 10) but not for the SLHC**
- **Different technologies mean also:**
  - **Many different operating voltages → extensive use of Vregs (both + and -)**
  - **Extremely difficult or impossible replacement of single component in case of failure**
- **Highly Accelerate Life Test (HALT) on FEBs are in progress to "anticipate" critical failure scenario ….**

Front-end Board (Present) Architecture



- Receive input signals from calorimeter, amplify and shape them
- Store signals in analog form while awaiting LVL1 trigger.
  - ***Analog pipeline implies communication to FEB for all LVL1 accepts***
- Digitize signals for triggered events
- Transmit output-data bits serially (over optical link) off detector
  - ***A single transmitter per FEB → single point of failure***
- Single clock (40 MHz, distributed by TTC) for readout and transmission
  - ***In principle it could operate at SLHC if beam scenario is "25 ns"***
- Provide analog sums to L1 trigger sum tree
  - ***Limits granularity for improved trigger capabilities***

Preparing for an "Upgrade":

- **The "substitution" of individual components with new ones, is not possible**
  - Some technologies are or will be obsolete soon
  - Current technologies operate at lower voltages
  - Redesign of ASIC required

What can be done for SLHC?

- Either operate with the existing electronics
  - → If radiation induced deteriorations are not too severe
  - → LHC experience will indicate when unacceptable performance will be reached
- Or (***better solution***) build a new complete front-end … starting with the FEBs
  - → Not a replica of the existing design with increased radiation tolerance
  - → The new design should:
    - be optimized against machine options (shaping time versus pile-up, etc…)
    - provide "enhanced" trigger capabilities
  - → Digital versus analog pipeline should be re-considered
    - pipeline could be ON or OFF detector
    - new high speed link could be necessary

  The redesign of the Front End will imply a substantial redesign of the Back End electronics
- **R&Ds for an upgraded Front-End Electronics must initiate now**

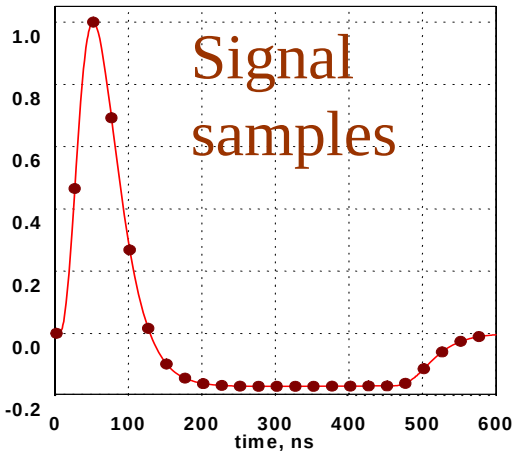
FEB upgrade: Digital versus analog Pipeline

- **Analog pipeline difficult to design given our dynamic range and noise requirements**
  - Operating voltages will be lower than in previous design

- **"Digital" means digitization of all FEB channels at bunch crossing-rate**
  - Power constraint is not to exceed the present ~ 800 mW/channel
  - The digital pipeline could be ON or OFF detector
    - ON → design an IC with adequate redundancy
      → await for LVL1 acknowledge
    - OFF → implement a solution capable of large data transfer
      → high speed links development is part of a "Common Project"
      → it will not require communication from LVL1 trigger down to FEB and could "decouple" trigger upgrade
  - **Digitizing does not mean removing analog trigger sums from FEBs**
    - Analog sums provide also an alternate readout path

Preferable Beam Scenario

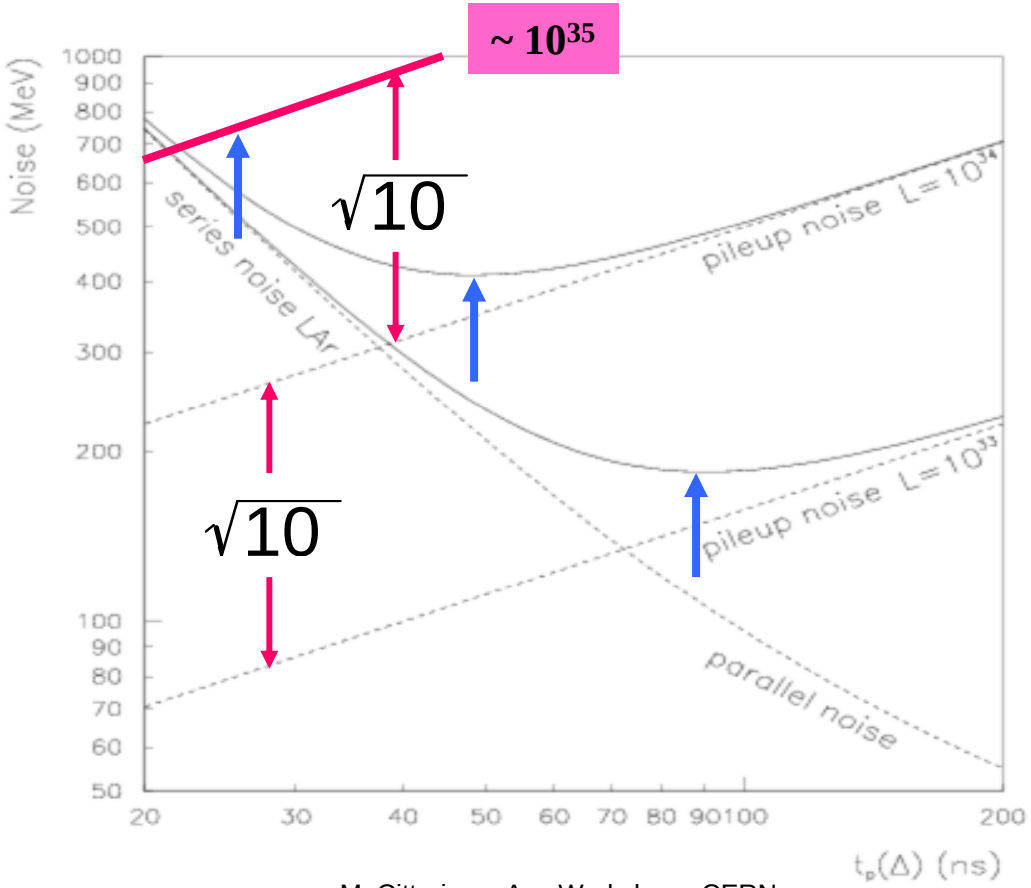
- **Current readout is based on a 40 MHz clock distribution (TTC)**
- **TTC signals distributed at a different frequency will affect the detector performances**
  - The energy reconstruction in a calorimeter cell is made through sampling the shaper output signal at every bunch crossing (25nsec) and calculating a weighted sum of the digitized samples.
  - The optimal filtering coefficients (OFC) used to reconstruct the cell energy optimize the energy resolution and compensate, partially, for a given pileup noise rate.
- **Based on the two proposed beam scenario (25 and 50 nsec option) we will continue to sample at 25 nsec intervals.**
  - To operate the readout at slower sampling rates, optimal number of samples must be studied again
  - At 50 nsec bunch crossing, not enough samples to reconstruct the positive lobe of the signal (aliasing effects)



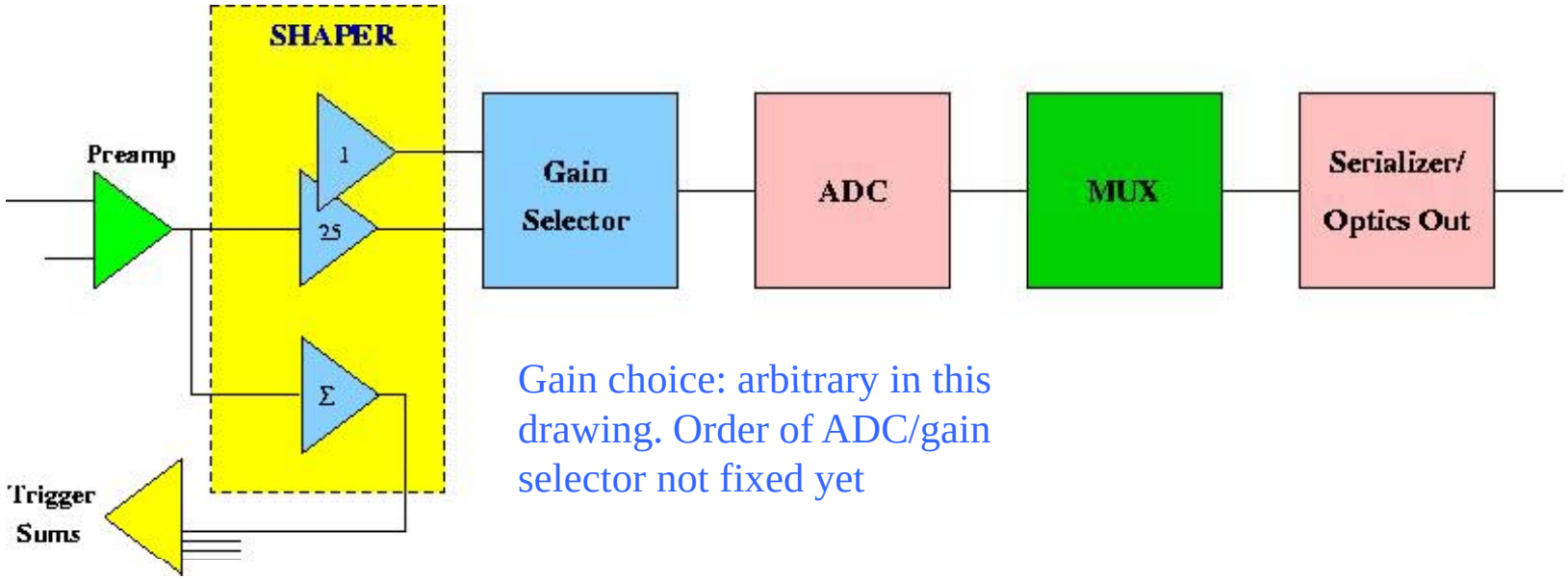
For Optimal Filtering, see: W.E. Cleland and E.G. Stern NIM A338 (1994) 467-497

Preferable Beam Scenario

- **Providing that "beam leveling" is achieved → Pileup is similar in the two beam scenario**
  - Pileup events from minimum bias are treated as an additional source of noise that scales approximately with √L (L being the instantaneous luminosity).
  - It should be investigated to what extent the OFC compensate for a non-optimal shaping (indeed at $10^{35}cm^{-2}s^{-1}$ the optimal peaking time would be ~28 ns instead of 40 ns for the current readout).



A possible new FEB architecture



- **Baseline is to digitize all channels at nominal sampling rate (25 nsec)**
  - Possibility to provide more fine-grained, "higher precision" data for a subsequent upgrade of the trigger system
  - Dynamic range is assumed to be 16 bits, still
  - No more "single" clock approach for both acquisition and data transmission
- **Variations to this preliminary architecture will still be explored**
  - In particular the use of a digital gain selector (that leads to a multiplication of the number of ADC channels)
- **At 25 nsec sampling rate → ~ 100 Gbps/board (128 channels)**
  - Fallback solution is to add a digital pipeline on the board
- **Analog trigger sums are ALWAYS available**

R&Ds needed and of interest

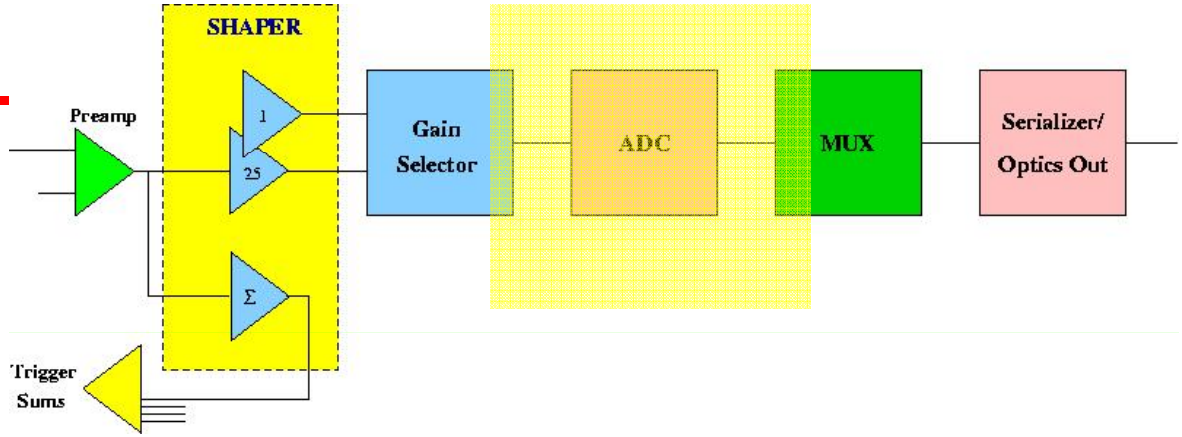
- **Activities are going to be focused on*:***
  - ***Optimization of design parameters***
    - *Shaper response*
    - *Number of gains*
    - *Analog or digital gain selector*
    - *ADC: # of bits*
    - ….
  - ***Technology selection for analog ASIC design***
    - ***Resistance to radiation***
    - ***Level of ASIC integration***
  - ***Selection between commercial and custom-designed ADCs***
  - ***Digital logic and "demonstrator set-up"***
  - ***Design of transmitters***
    - The baseline design calls for shipping data off detector at the nominal sampling rate → requiring 100 Gbps per board in transmission bandwidth.

Technology for Analog ASIC design

- **SiGe BiCMOS technology appears to be a good candidate for the analog ASICs**
  - 0.18 μm has been characterized for radiation hardness by CERN
    - Neutron/ionizing radiation hardness "by construction"
    - Better evaluation of SEE problems is ongoing
  - Geared toward HF/RF applications → analog friendly
  - IN2P3 Microelectronics Poles have grouped resources and expertise (proven building blocks, etc.) (C. de la Taille, LAL)
  - IBM 8WL process now available through MOSIS
  - **However in conflict with CERN "investment" in IBM 0.13 μm process**
- **R&D to evaluate process performance has started**
  - **Proposal submitted to Upgrade Steering Group**
    - Joint collaboration between ID and LAr groups

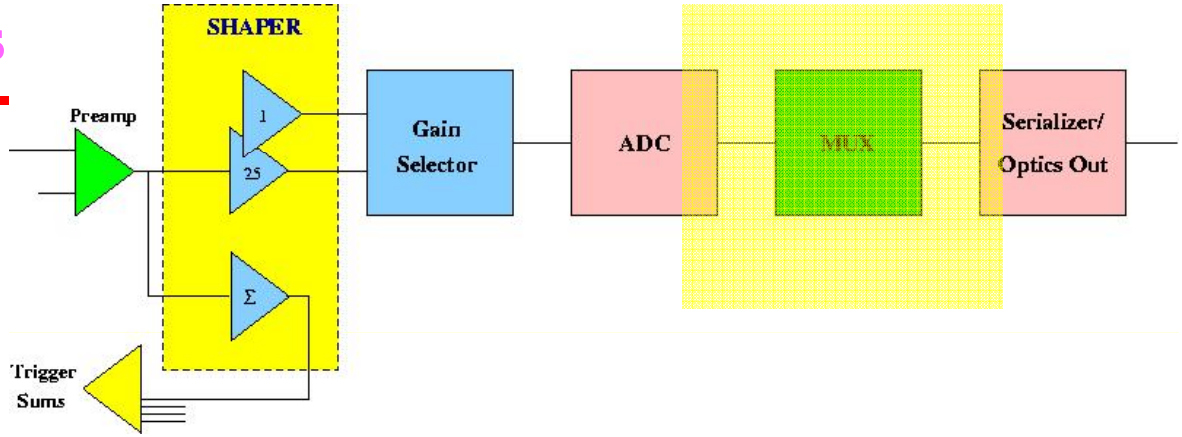
    → **ATL-P-MN-0008: Evaluation of Silicon-Germanium (SiGe) Bipolar Technologies for Use in an Upgraded ATLAS Detector [A.Grillo, S. Rescia]**
  - **Radiation testing started on test structures (UCSC, BNL, Georgia Tech)**
  - **Preamp feasibility study done in 7WL process (S. Rescia BNL)**
    - Translation of the circuit design in 8WL process is in progress
  - **Technology looks a good candidate for other analog components as well**
    - shaper, gain selector, front end of ADC

ADC issues

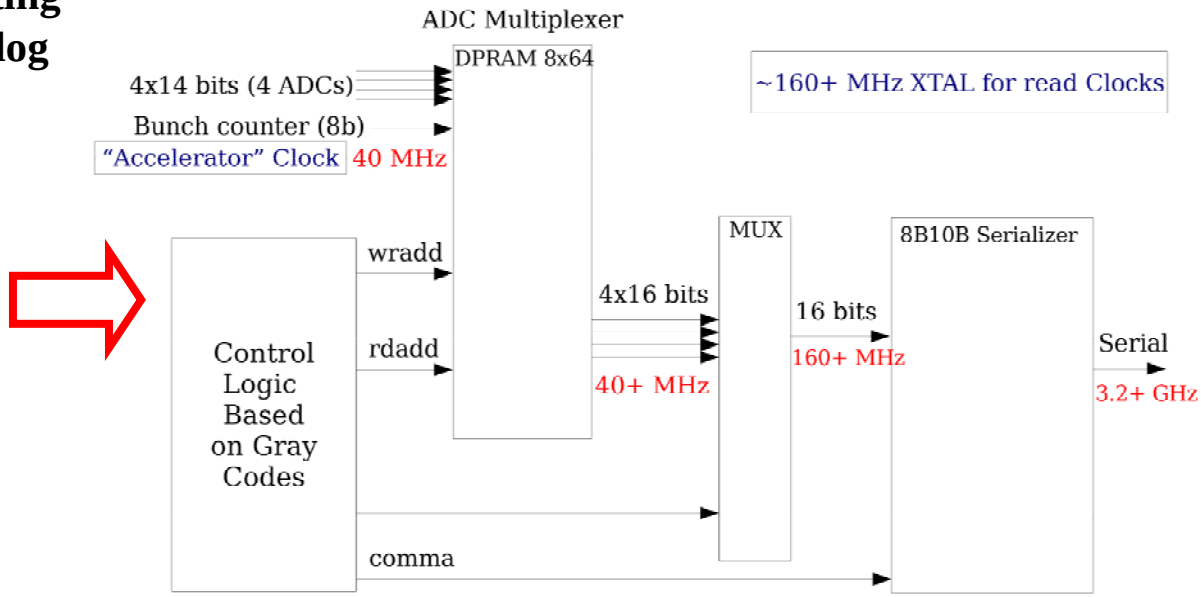


- **Difficult Problem:**
  - Large dynamic range (16 bits)
  - High speed
  - Low power → tentative estimate < 400 mW/ch
- **Some commercial ADCs close to satisfy the requirements**
  - **Must be tested again radiation → success not guaranteed**
  - **Process information are proprietary**
- **IN2P3 R&D program has developed nice low power ADCs**
  - Work on dynamic range still necessary
- **The ADCs could be a custom design if no commercial solution becomes available**
  - Time is needed to develop such a circuit

Digital Logic Studies



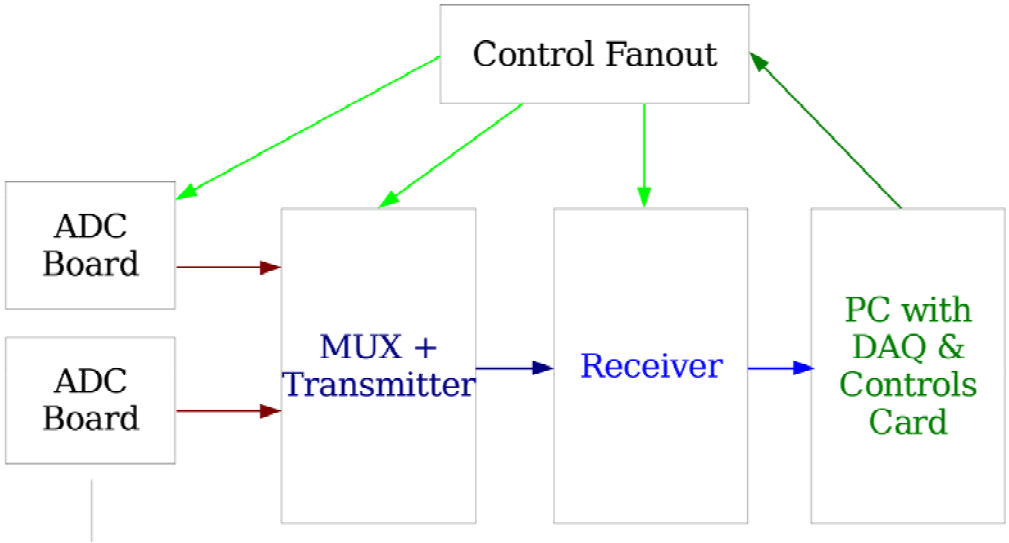
- **Studies started (G. Brooijmans, NEVIS)**
  - **Starting point to "focus" ideas**
  - **Important part of the testing infrastructure to test analog component**
- **A first "test prototype" available:**
  - **Composed by a MUX + transmitter**



MUX + Transmitter "test jig" Design Features

- **Two independent clocks**
  - ADCs clocked to nominal sampling time, fill "ADC multiplexer" at that rate
    - Needs to be brought down to the board
  - MUX, serializer (all high-speed components) use clock derived from a crystal
    - Much better jitter control
    - Choose frequency to be (4+e) times accelerator clock, allowing regular insertion of control words
- **Gray code to manage ADC multiplexer addresses**
  - Minimize effect of errors
- **Data spends very little time in "ADC multiplexer" (few bunch crossings)**
  - Minimize upset possibility there
- **But triple redundant MUX**
- **IBM 8B10B encoding at serializer level**
  - Standard in many high-speed applications (PCI Express, Gb Ethernet, ...) – part of FPGA "libraries"
  - Low complexity (5B6B + 3B4B)
  - Sufficient transition density for clock recovery (never more than 5 consecutive identical bits), DC balanced
  - Error detection and control characters
- **Also considering a "scrambling" model**

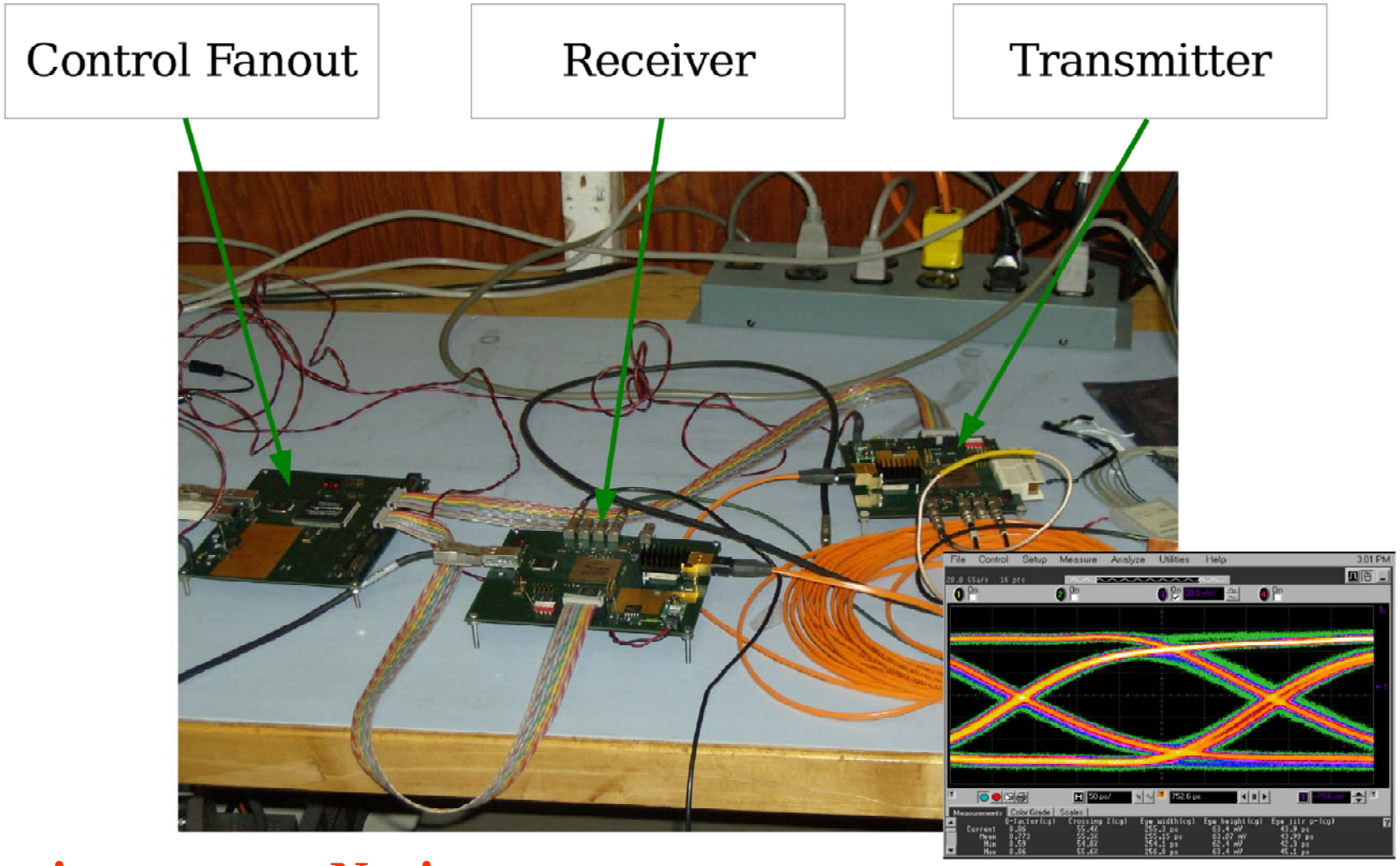
Testing Infrastracture (1 of 2)



Current Status at NEVIS

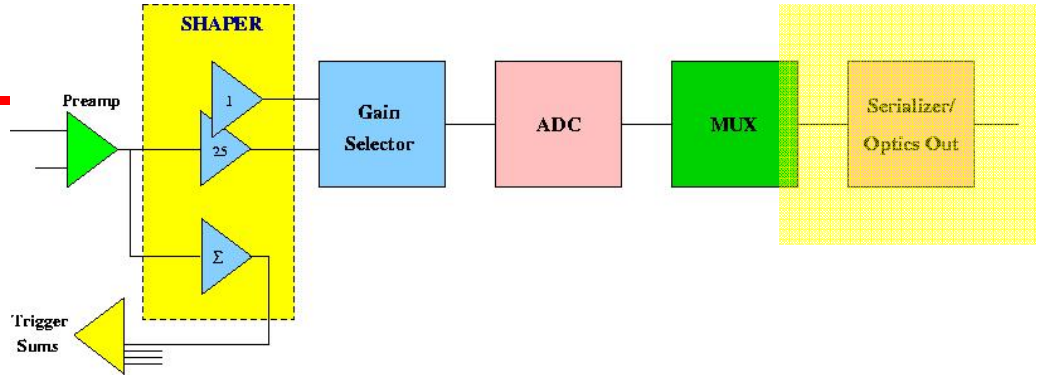
- DC, transmitter, receiver and PCI express (1x) DAQ board all working
  - All use “placeholder” COTS devices
  - TI ADS 5272: 8 channel, 65 MSPS 12-bit ADC with multiplexed LVDS outputs (~100 mW/channel)
  - ALTERA Stratix GX FPGAs drive optical transmitter
  - Agilent (now Avago Technologies) HFBR-772 optical transmitter (and corresponding receiver)
- By the end of the year, test large data transfers at high speed
- Next year plan: Signal injection in ADC
  Radiation testing of ADCs (in parallel with SiGe)

Testing Infrastracture (2 of 2)



Testing setup at Nevis

Transmitter



- **100 Gbps imposes strong constraints**
  - High bandwidth per link → target speed is ~ 10 Gbps
  - Reduced power consumption
- **Link-on-chip (J. Ye and P. Gui, SMU)**
  - **Serializer, PLL, laser driver and laser in one single chip**
    - No off-chip high speed lines
    - Flip-chip bonding reduces capacitance and inductance
  - **Technology chosen: Silicon-on-Sapphire with transparent substrate**
    - Test chip to evaluate radiation hardness of Peregrine 0.25 μm SoS process designed by SMU in 2005 → speed achieved ~ 2.5 Gbps
    - SEE under test, but expected to be much smaller than for bulk CMOS (based on results with 0.5 μm SoS)
  - TID test at BNL in fall 2006 (Co-60 source)
    - Results not fully analyzed yet, but preliminary indications suggest survival up to 4 MRad
- **For more info:**

  http://indico.cern.ch/materialDisplay.py?contribId=24&sessionId=2&materialId=slides&confId=7791

Other boards and infrastructure … that need to be upgraded

- **Upgrade of the other boards which are integral part of the front end electronics:**
  - **The calibration board should be redesigned mostly to cope with increased radiation background**.
    - No substantial architectural changes are expected in the calibration board in respect to the existing boards.
  - **Unless a trigger upgrade is simultaneous, the tower builder board will need to be replaced as well**.
  - **The need for a controller board in the upgrade scenario is still under discussion**.

  → At the moment the focus is mostly on the FEB redesign

- **The LV power supplies will also need to be replaced**
  - This will either require separate R&D or rely on a commercial vendor.
  - This will be addressed after the current power supply issues are resolved.

- **Cooling System:**
  - Knowledge of the power consumption of the future FEBs is not yet known
  - Power budget (~2.6 kW/crate) must not be exceeded
  - Experience with the existing cooling system will determine whether a replacement of that system is necessary as well.

Summary

- Possible, but not likely that LHC Front-end Electronics will be OK for SLHC
- Upgrade means “replace everything”
- R&D program has been started by
  - **joining existing proposal**
  - **submitting Expression of Interest**
- Under discussion are:
  - **ASIC technologies**
  - **Ideas about new architecture**
- Some progress in studying digital architecture have been made through “test set-up”
  - **Get full testing infrastructure as by product**
- More detailed information on machine scenario will help in properly defining the boundary conditions