CMS Strip Architecture

OUTLINE

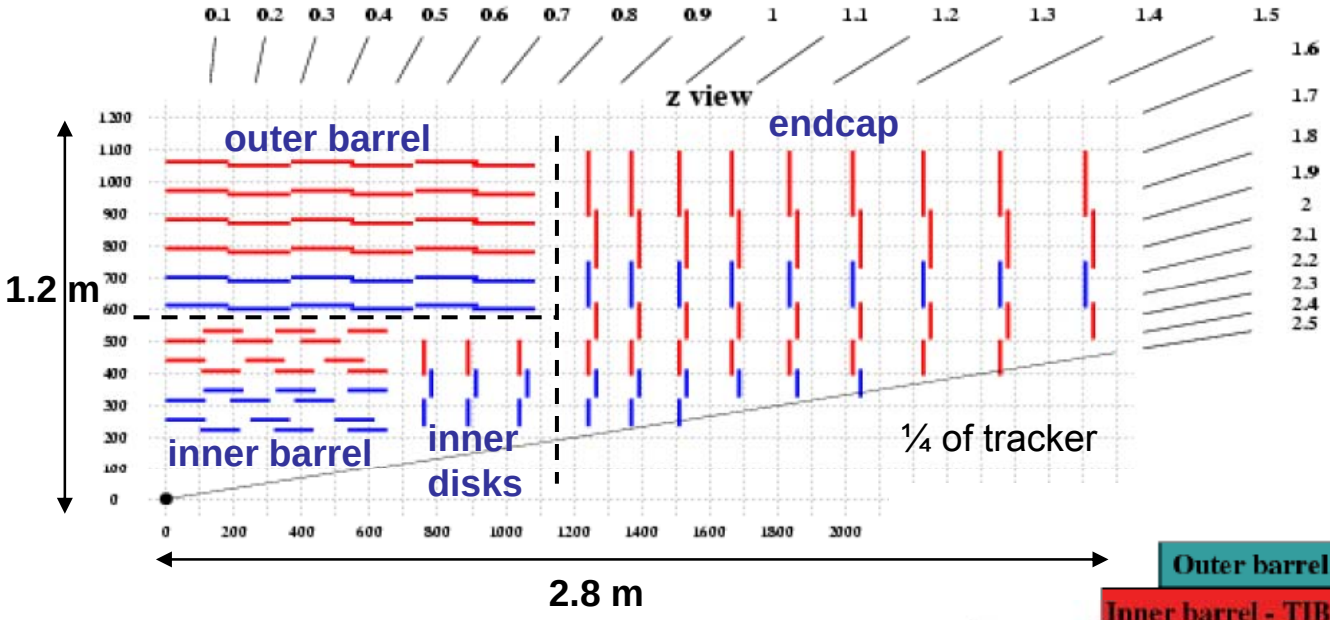
review of current CMS microstrip tracker architecture

some ideas on architectures for SLHC
concentrating mainly on power issues

possible areas for Atlas/CMS collaboration

Mark Raymond – Imperial College London

CMS LHC strip tracker



all single sided sensors

single layer modules

double layer modules (two modules, back-to-back, angle between strips)

some numbers

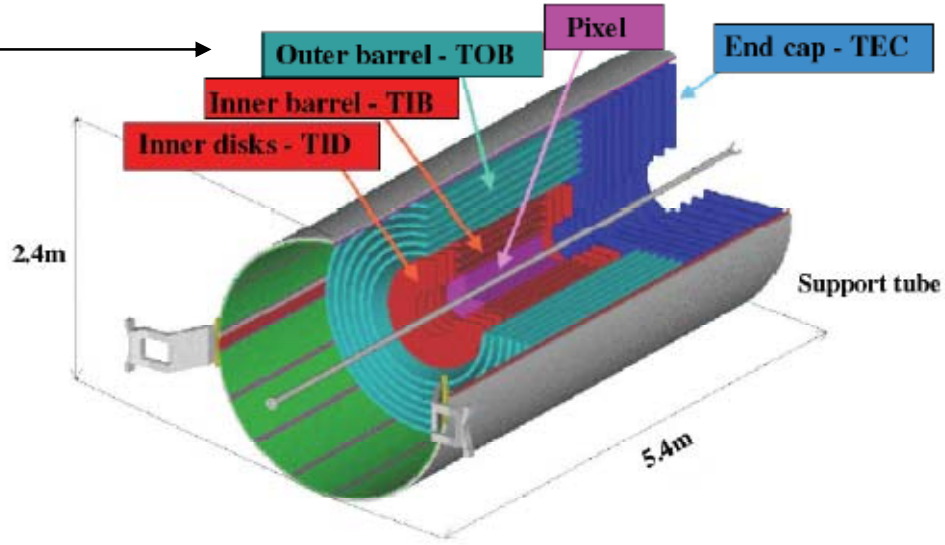
~ 200 m^2 sensor area

~ 15,000 detector modules altogether

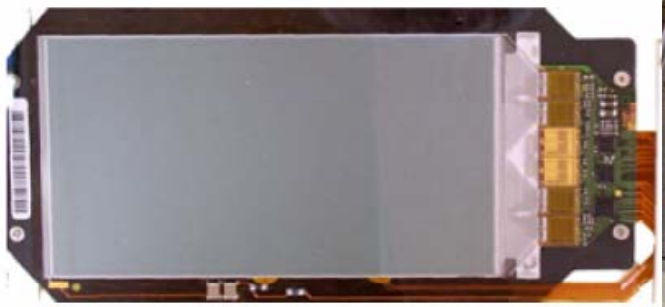
~ 10^7 strips, ~75,000 FE chips (APV25)

strip lengths: ~ 12 – 19 cm

strip pitches: ~ 80 – 180 μm



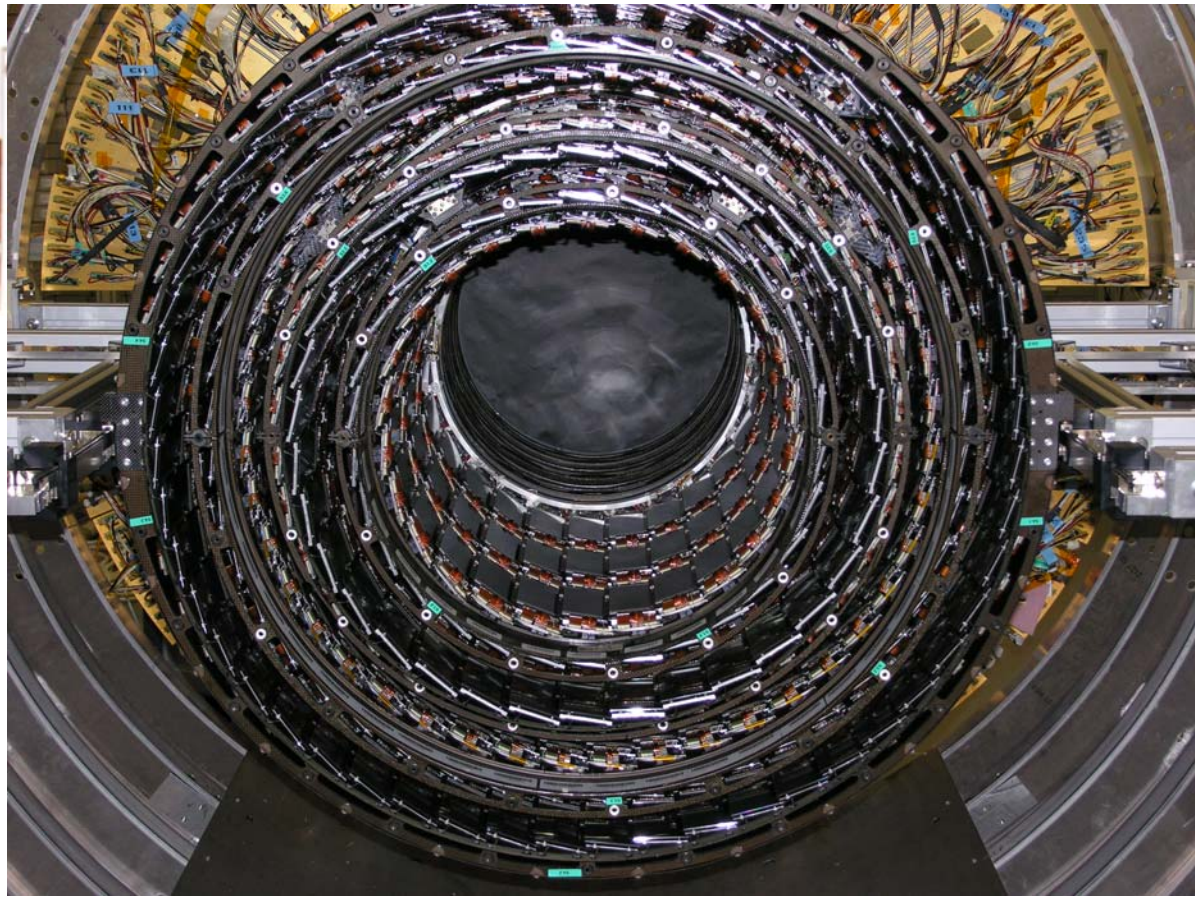
inner barrel



single sensor / module

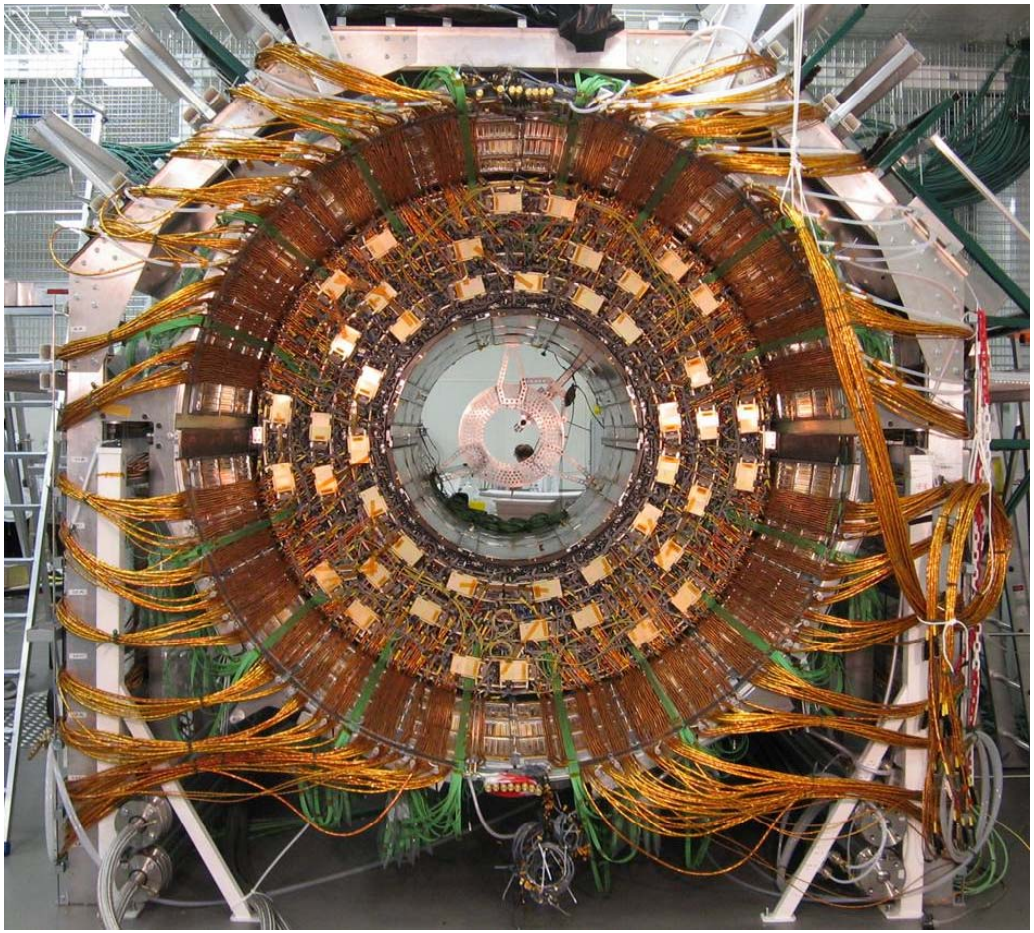
inner barrel

4 layers (2 double-sided)
320 μm thick sensors



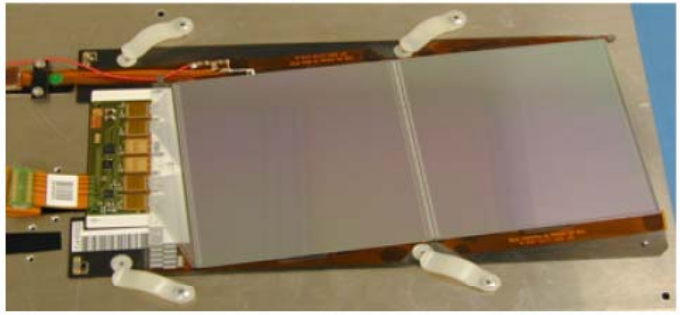
~ 1m

outer barrel



outer barrel – cabled up

2.4 m



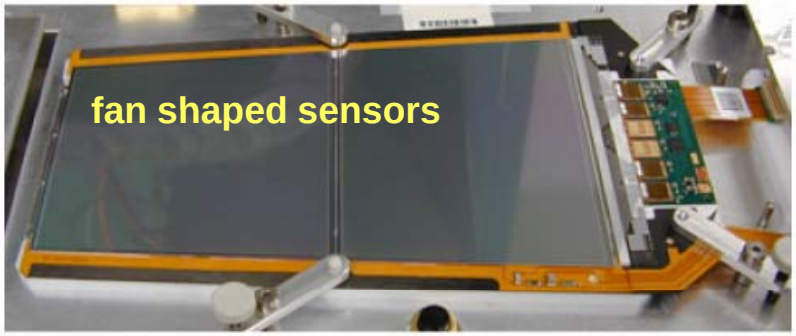
double sensor modules

outer barrel

6 layers (2 double-sided)

500 μm thick to get good
S/N for larger sensor capacitance

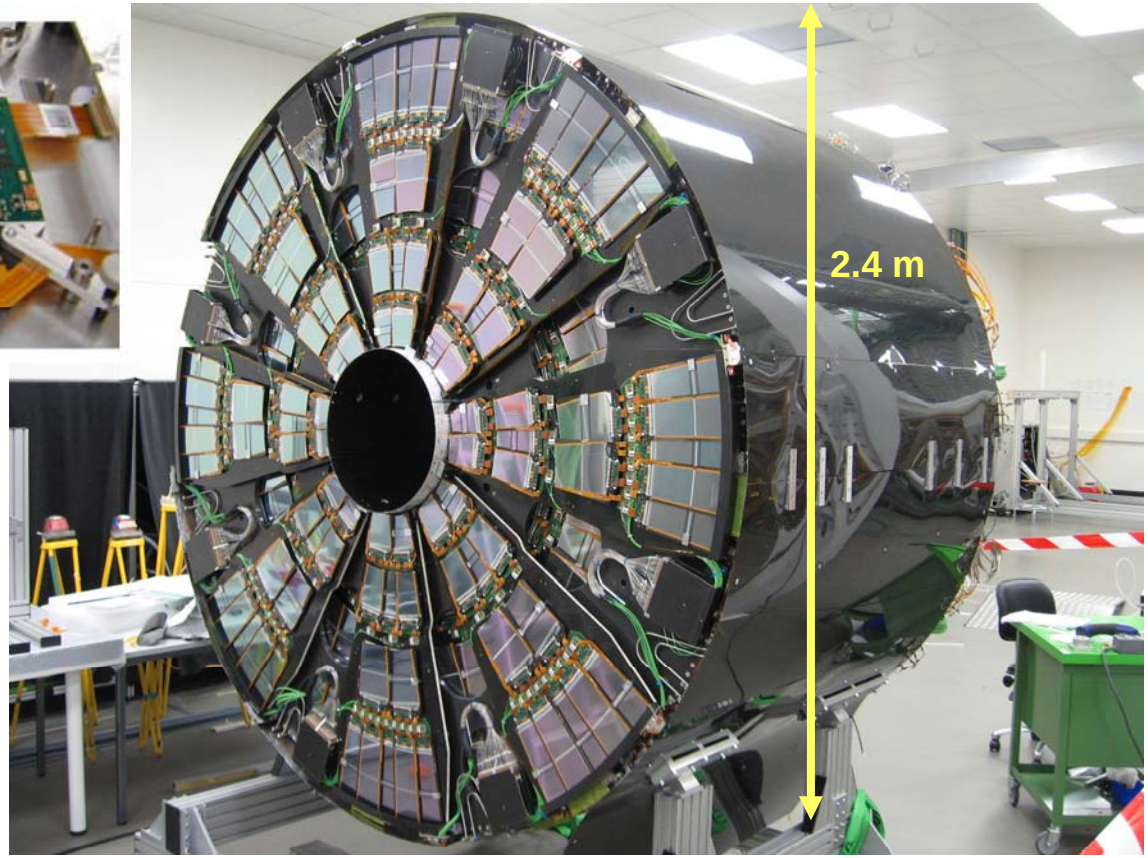
endcaps



double sensor module

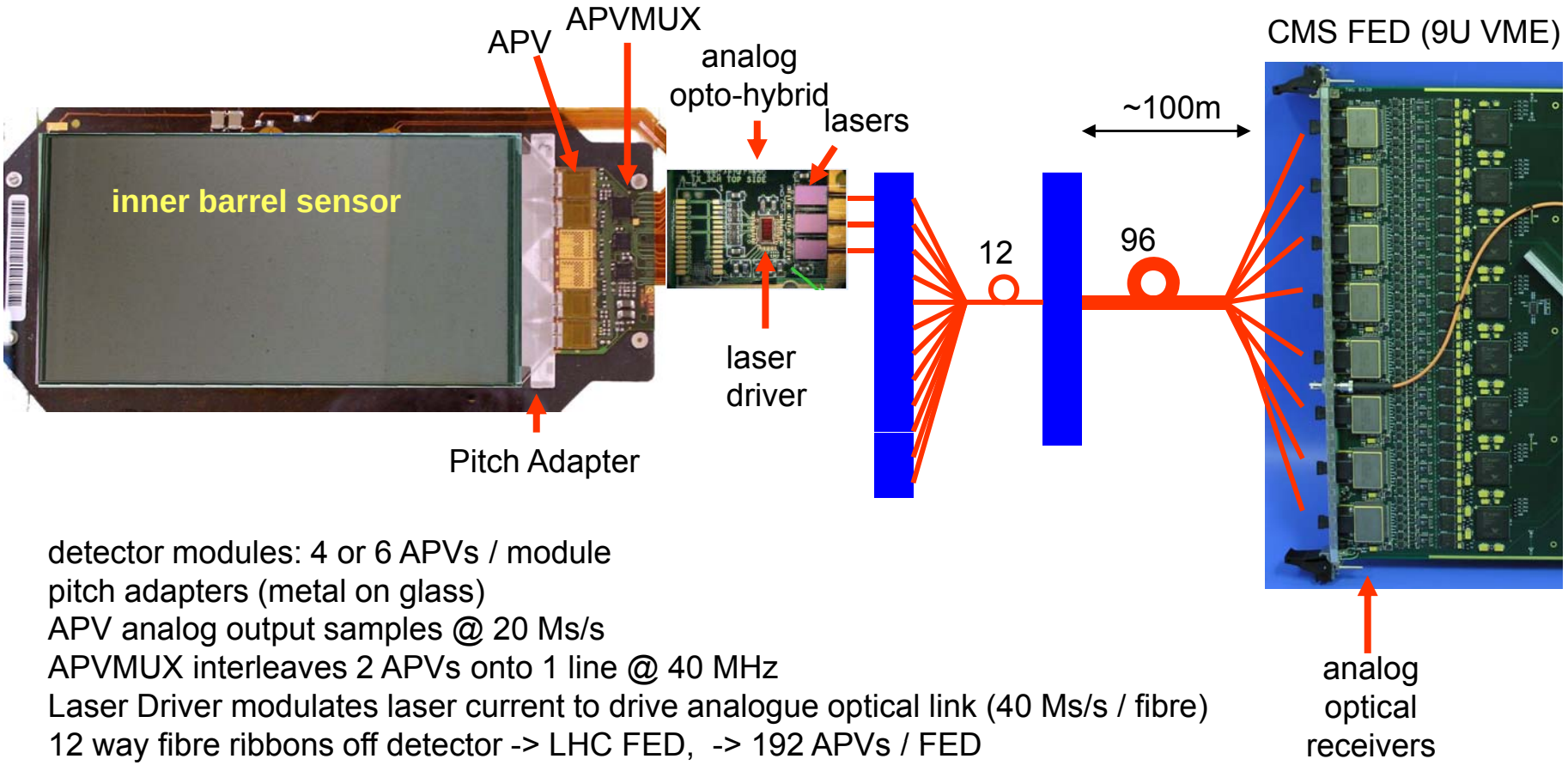
endcaps

9 disks/endcap
mixture of double/single layers
mixture of double/single sensors/module
thin and thick sensors



one tracker endcap in integration facility – disks made up of petals

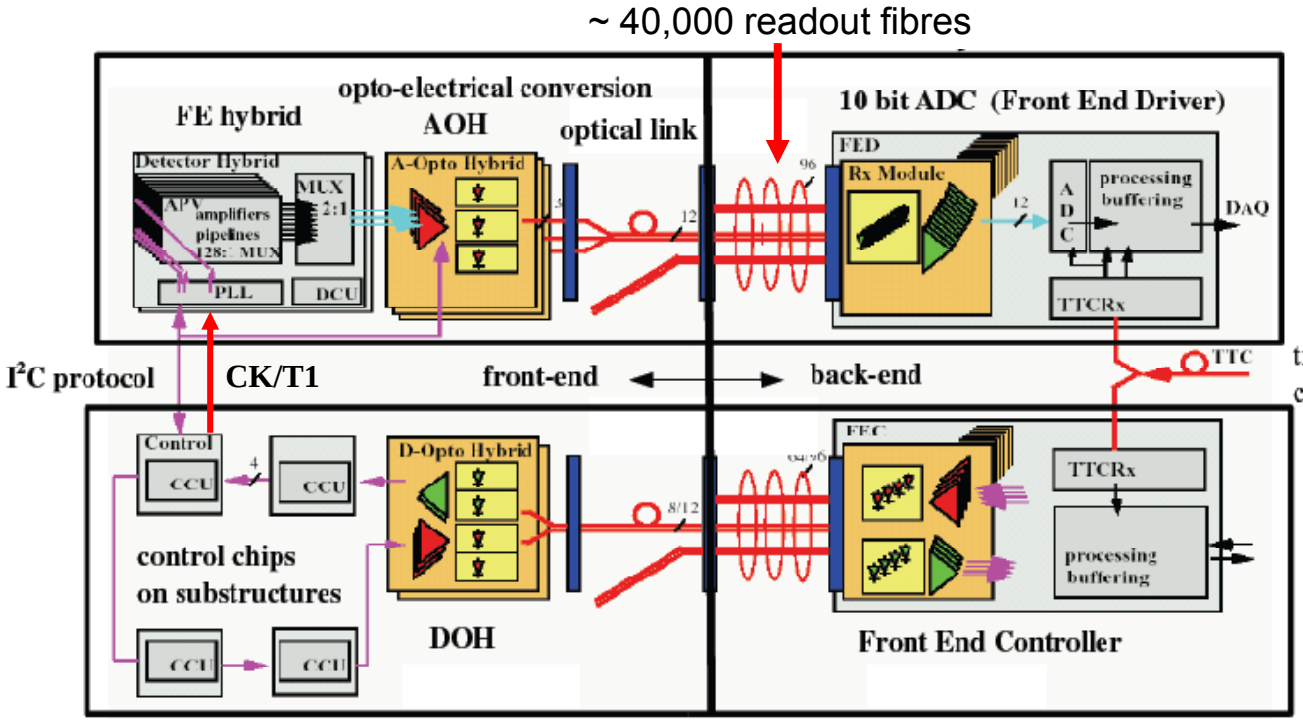
CMS LHC strip readout system



detector modules: 4 or 6 APVs / module
pitch adapters (metal on glass)
APV analog output samples @ 20 Ms/s
APVMUX interleaves 2 APVs onto 1 line @ 40 MHz
Laser Driver modulates laser current to drive analogue optical link (40 Ms/s / fibre)
12 way fibre ribbons off detector -> LHC FED, -> 192 APVs / FED

all on-detector chips in 0.25μm CMOS (including control system)

control system



digital optical control link
from FEC -> front end provides
Ck/T1 and control data

opto-electrical conversion
on front end

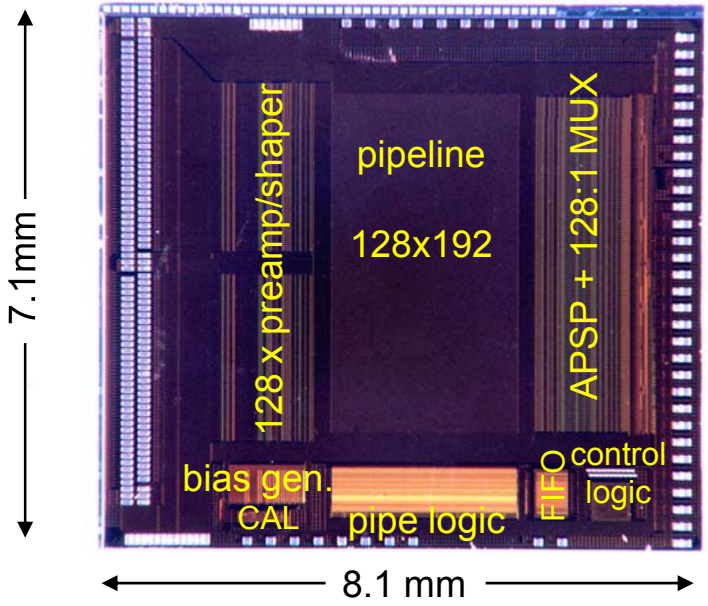
CCU chip electrical control ring
architecture on front end reduces
no.of control fibres required

each CCU provides
Ck/T1 and I²C control buses
to up to 16 FE modules

I²C used for:

- programming APV registers (bias generation and operation mode)
- reading DCU monitoring info (voltages, currents, temperatures)
- setting up optical link system (laser driver gain, bias currents)

APV25

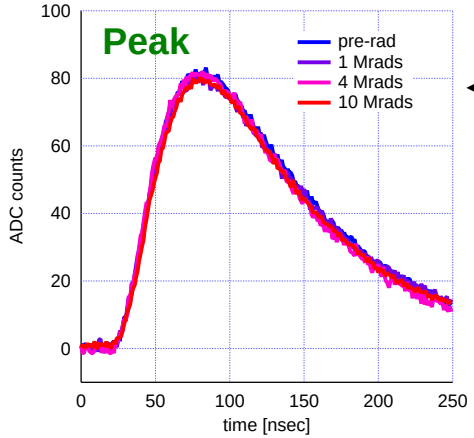


128 channel chip for AC coupled sensors

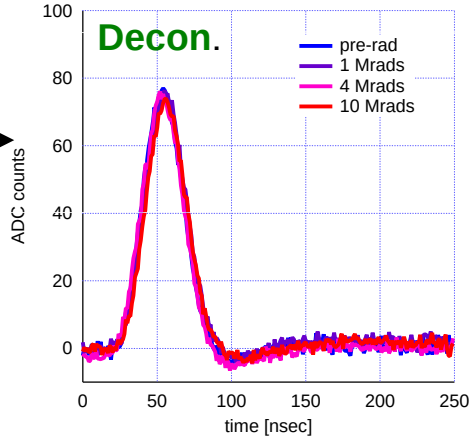
slow 50 nsec. CR-RC front end amplifier

192 cell deep pipeline (allows up to 4 μsec latency
+ locations to buffer data awaiting readout)

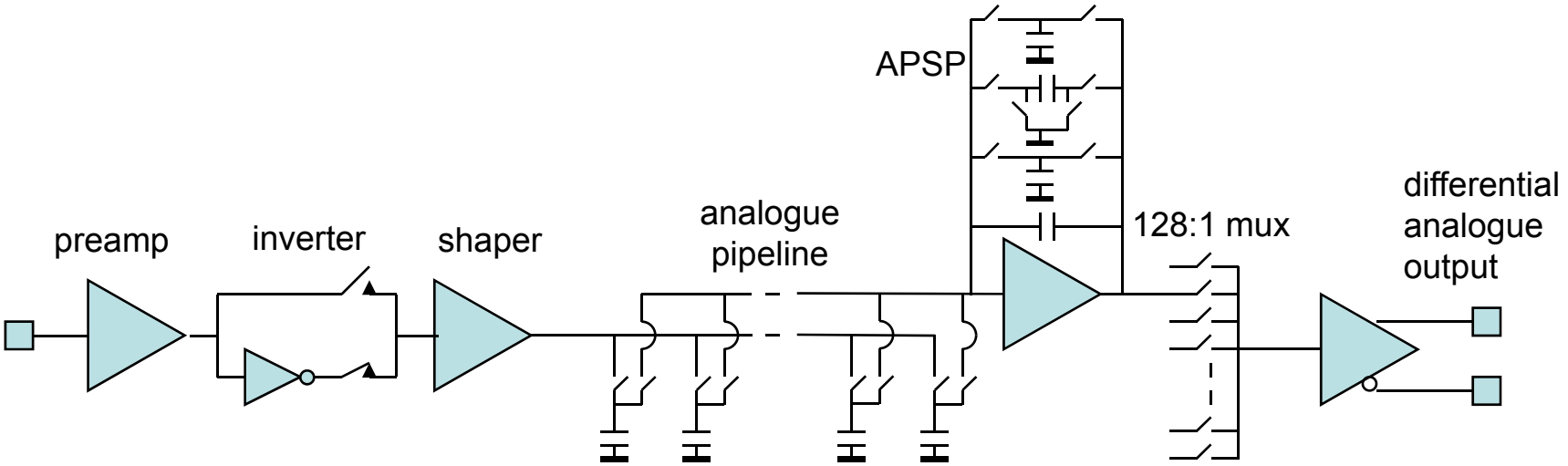
peak/deconvolution pipeline readout modes
peak mode -> 1 sample -> normal CR-RC pulse shape
deconvolution -> 3 consecutive samples combined to give single bunch crossing resolution



noise
270 + 38 e/pF (peak)
430 + 61 e/pF (deconvolution)

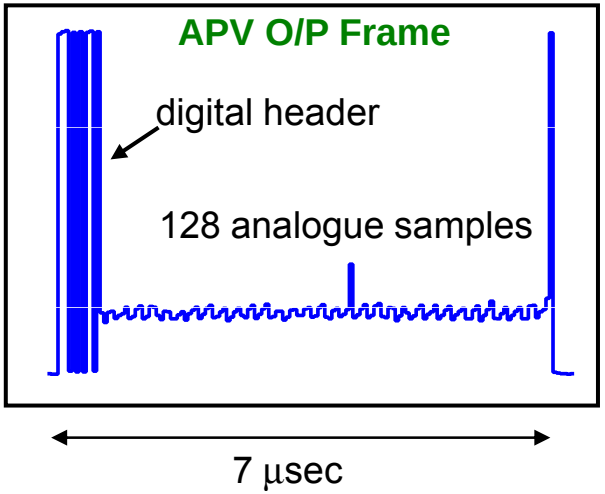


APV25 – analog chain



pipeline readout slow, just has to keep up with L1 latency (< 10μsec)

no sparsification on-detector in CMS
output data frame consists of
128 analog samples
digital header - contains pipeline address from where data originated



off-detector FED functionality

opto-electric conversion

10 bit 40 MHz digitization

pedestal and CM subtraction

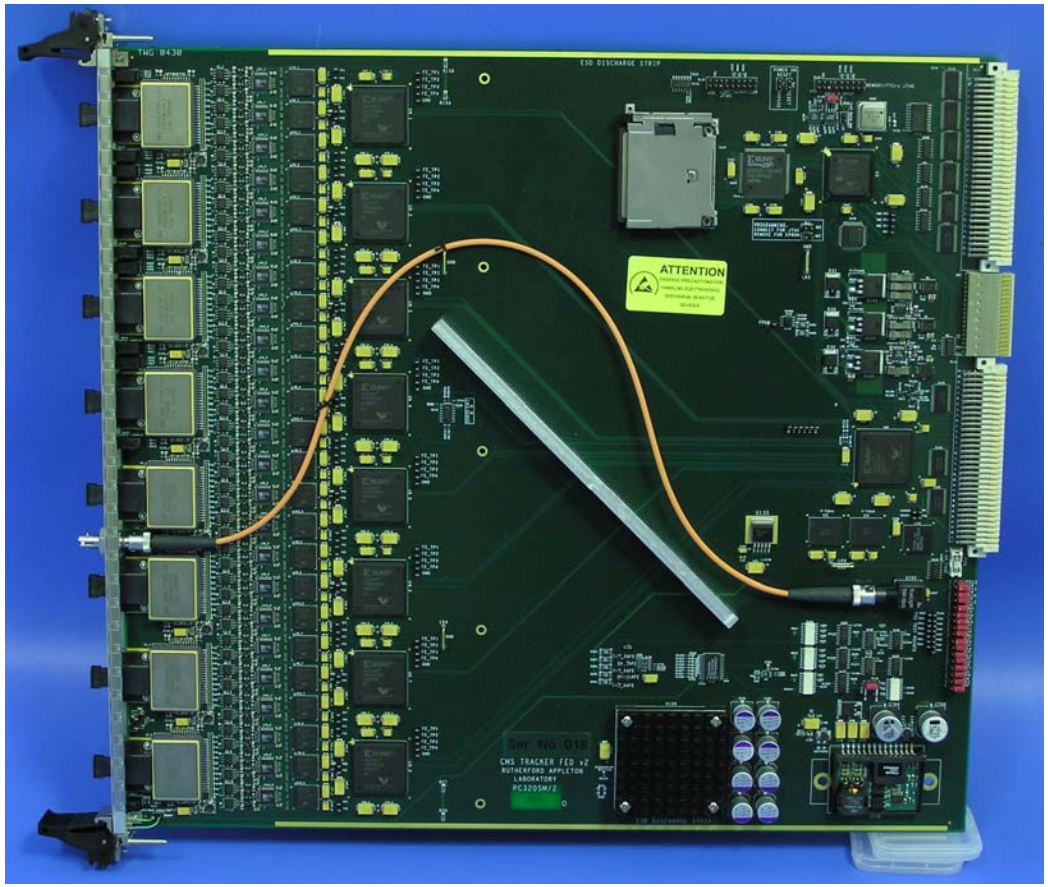
hit finding (sparsification)

formatting and transmission of data
up to higher DAQ level

check of APV synchronization

- all tracker synchronous, so all pipeline addresses of all APVs should be the same

- FED checks received APV pipe address matches with expected value
(APV logic emulated at trigger level)



9U VME

CMS strip tracker for SLHC

CMS SLHC tracker design still evolving, current ideas are:
- expand pixel regions to radii up to 60cm
- short strips outer barrel region (R >60cm)

necessity for tracker info in L1 trigger
- probably use dedicated triggering layers (other talks)

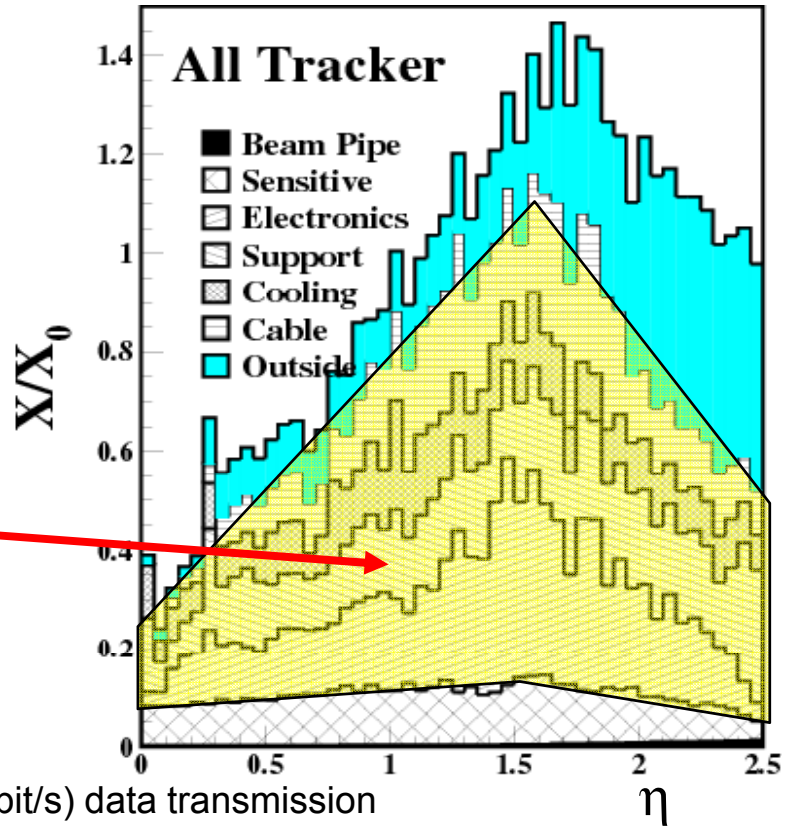
power is the big issue
- higher luminosity, higher granularity => more FE chips
- electronics related material dominates material budget

0.13 μm technology will help but savings depend on
any additional front end functionality required

off-detector optical links will be high speed digital
- follow commercial developments for high speed (multi-Gbit/s) data transmission

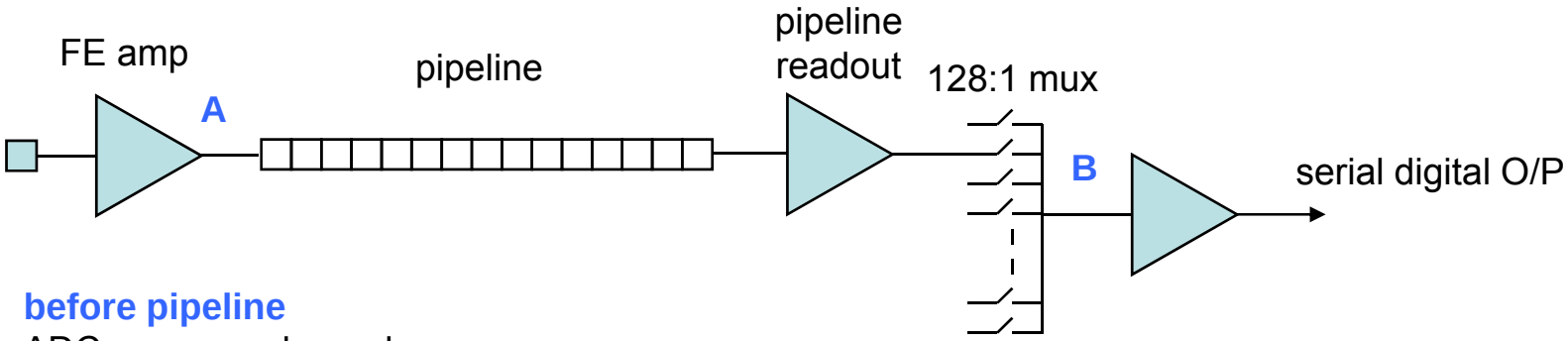
=> one additional functionality on-chip digitization if want to retain analog information

CMS tracker material budget



SLHC FE architecture

generic pipeline chip architecture – where to go digital?



A) before pipeline
ADC on every channel
digital multi-bit/channel pipeline
fast FE to achieve single bunch resolution
(unless digital deconvolution?)

B) after mux
ADC power shared by 128 channels
analog pipeline, analog mux
could keep slow FE + decon pipeline readout

ADC runs at 20 MHz in location A
~ same in location B (still need to digitize 128 chans in < 10 μsec)

ADC power drives choice of A or B

ADC power consumption

ADC Scaling *

- A/D Performance Figure of Merit

$$FoM = 2^{ENOB} * f_{sample}/P$$

Year	2003	2006	2009	2012	2015
Tech [nm]	130	90	65	45	32
FoM [GHz/W]x10³	0.8	1.2	1.6-2.5	2.5-5	4-10

From ITRS roadmap 2003

International Technology Roadmap for Semiconductors (ITRS-2003)
(forecast from the semiconductor industry with 15 year perspective)

based on general considerations (individual architecture dependent)

ADC power given by process, Effective No. Of Bits, conversion frequency and FoM

ADC on every channel hard to do

6 bits @ 20 MHz -> 1.6 mW (0.13μm)

ADC on every chip quite possible

8 bits @ 20 MHz -> 6.4/128 -> 50 μW/chan

APV25 power
2.7 mW / chan.

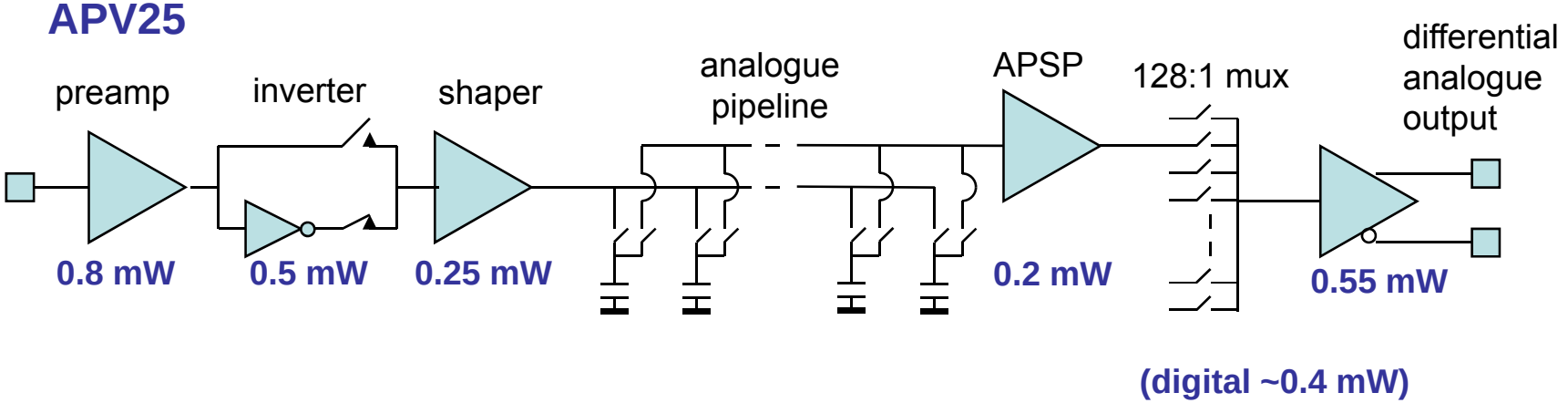
ADC power @ 20 MHz [mW]

	130nm	65nm
8bits	6.4	2.5
6bits	1.6	0.6

* from A. Marchioro talk at 2nd CMS SLHC workshop

front end power

APV25



APV25 power breakdown [mW/channel]

preamp/shaper	1.05
inverter	0.5
APSP	0.2
mux & output stages	0.55
digital	0.4
	2.7

front end power dominates

preamp dominates FE power (I/P device current)

what FE power can we expect for 0.13 μm design for short strips?

can get some idea by translating existing design to 0.13

0.13 μm preamp

go for straightforward architecture translation

but one difference for preamp

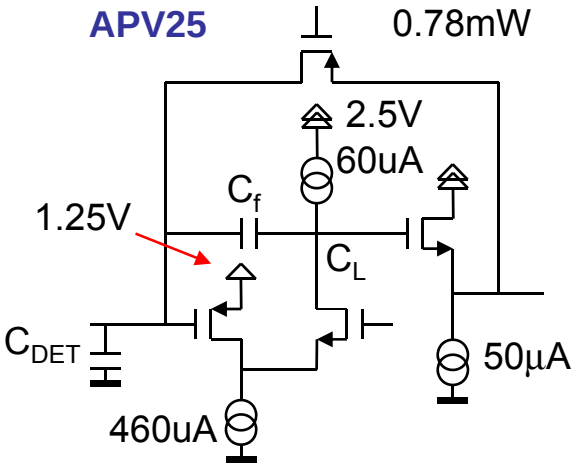
APV25 preamp: 3 supply rails (0, 1.25V, 2.5V)

1.25 V saves power

propose not to do this again for SLHC

use 2 rails only, 0 and 1.2V, accept power penalty

but gain simplification in power supply system

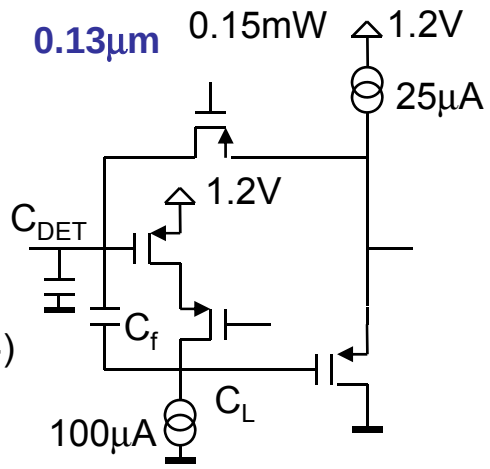


preamp noise & speed depend on input device transconductance (gain) g_m

noise ∝ $C_{DET}/\sqrt{g_m}$

risetime ∝ $C_{DET}C_L/C_f g_m$

$g_m \propto \sqrt{C_{OX}(W/L)I_{DS}}$	S.I.
$\propto I_{DS}$	W.I.



shorter strips -> smaller C_{DET} so lower g_m tolerable

if choose to accept ~ factor 2 increase in noise slope (over APV25)

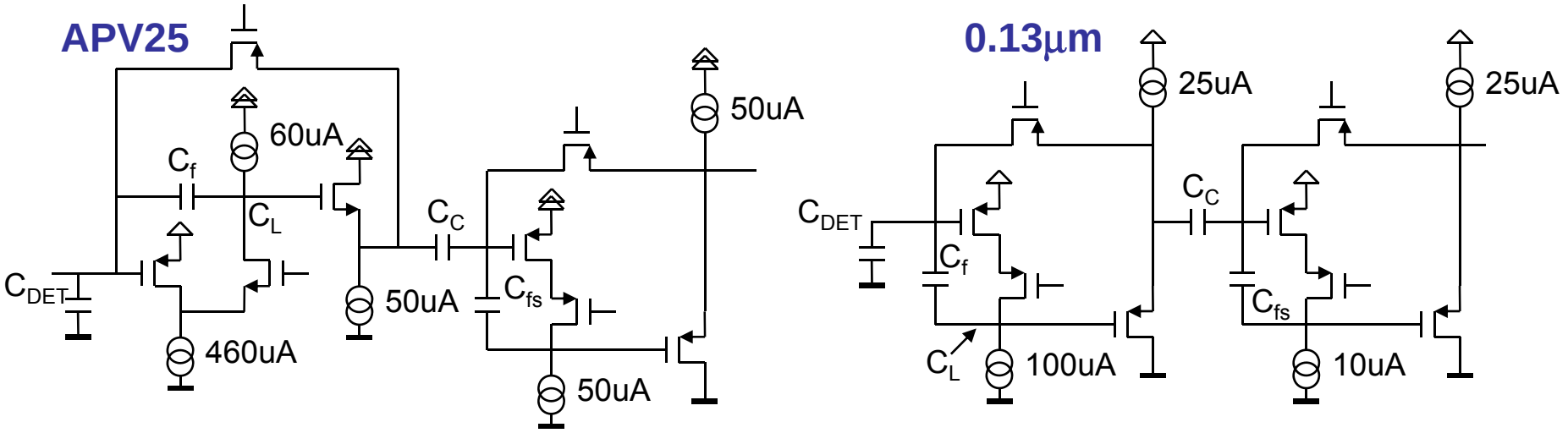
then factor 4 decrease in g_m

simulation shows this achieved for ~ 100 μA in 0.13 I/P device (W/L = 1000/0.24)

total preamp power (including source follower) = 125 μA x 1.2 V = 0.15 mW

factor ~ 5 reduction from 0.78 mW (APV25 preamp only)

preamp/shaper design



shaper

0.13 µm architecture identical to APV25, 50 ns time const.

keep gain as high as possible

80 mV/mip c.f. 100 mV/mip for APV25 (1 mip = 4 fC here)

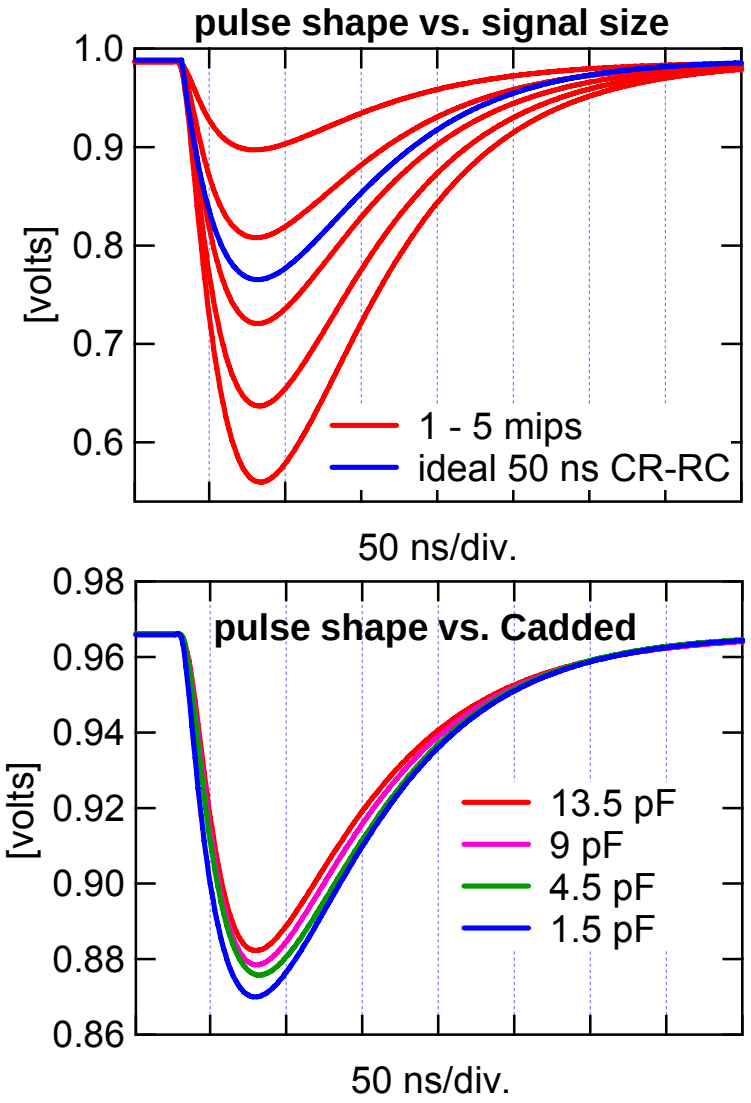
maximises use of available dynamic range, but only works for one polarity (-ve input signal)

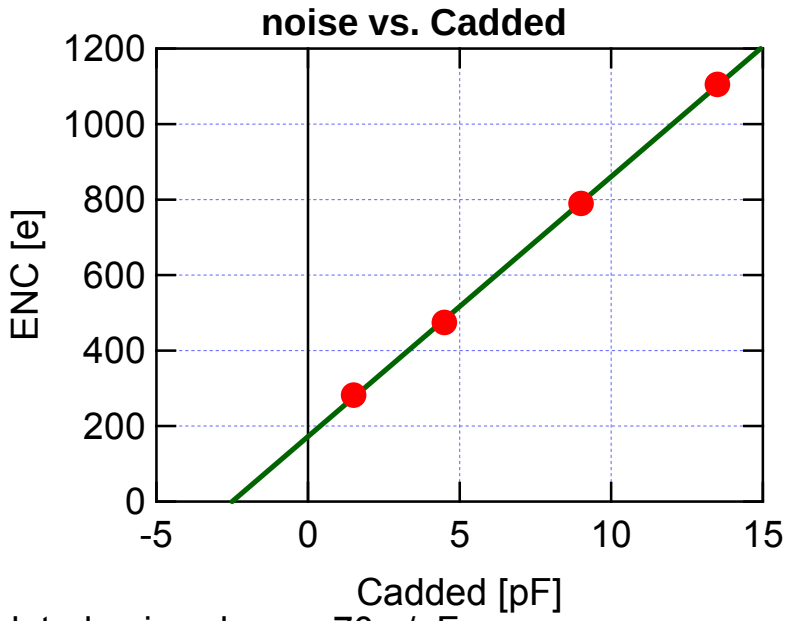
=> need alternative architecture for p-strip signals

total 0.13 shaper power 42 µW

factor ~ 6 reduction from 250 µW (APV25)

0.13 preamp/shaper simulated performance





simulated noise slope ~ 70 e/pF

=> input noise spectral density ~ 2.6 nV/√Hz, compares quite well with real transistor measurement ~ 2 nV/√Hz

can cope with strips up to ~ 10 cm

overall preamp/shaper power consumption reduction
1.025 mW (APV25) -> 0.192 mW (0.13 μm)

factor ~ 5

0.13 preamp/shaper comments

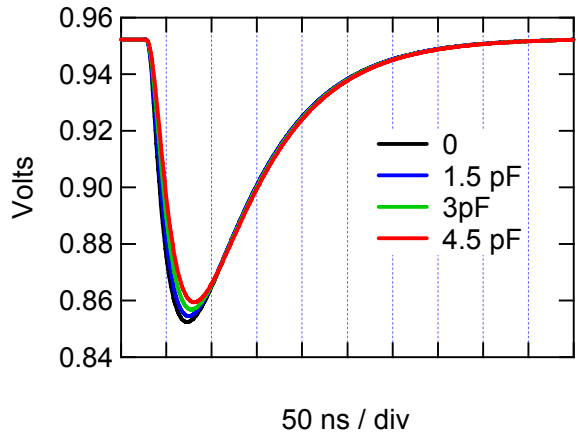
significant FE power savings possible
short strips (lower C_{DET}) helps a lot

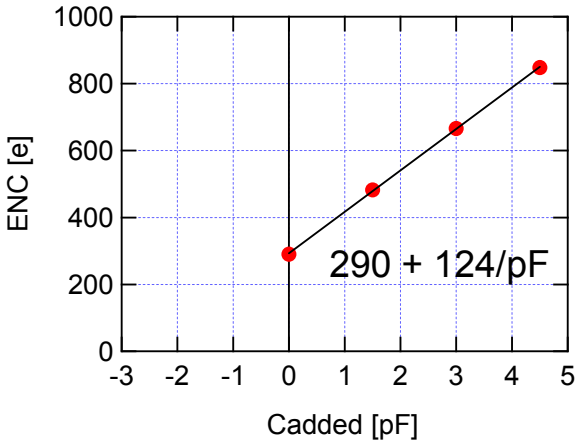
can do better if accept worse noise slope
(e.g. for very short strips)

results for only 40 μA in input device →

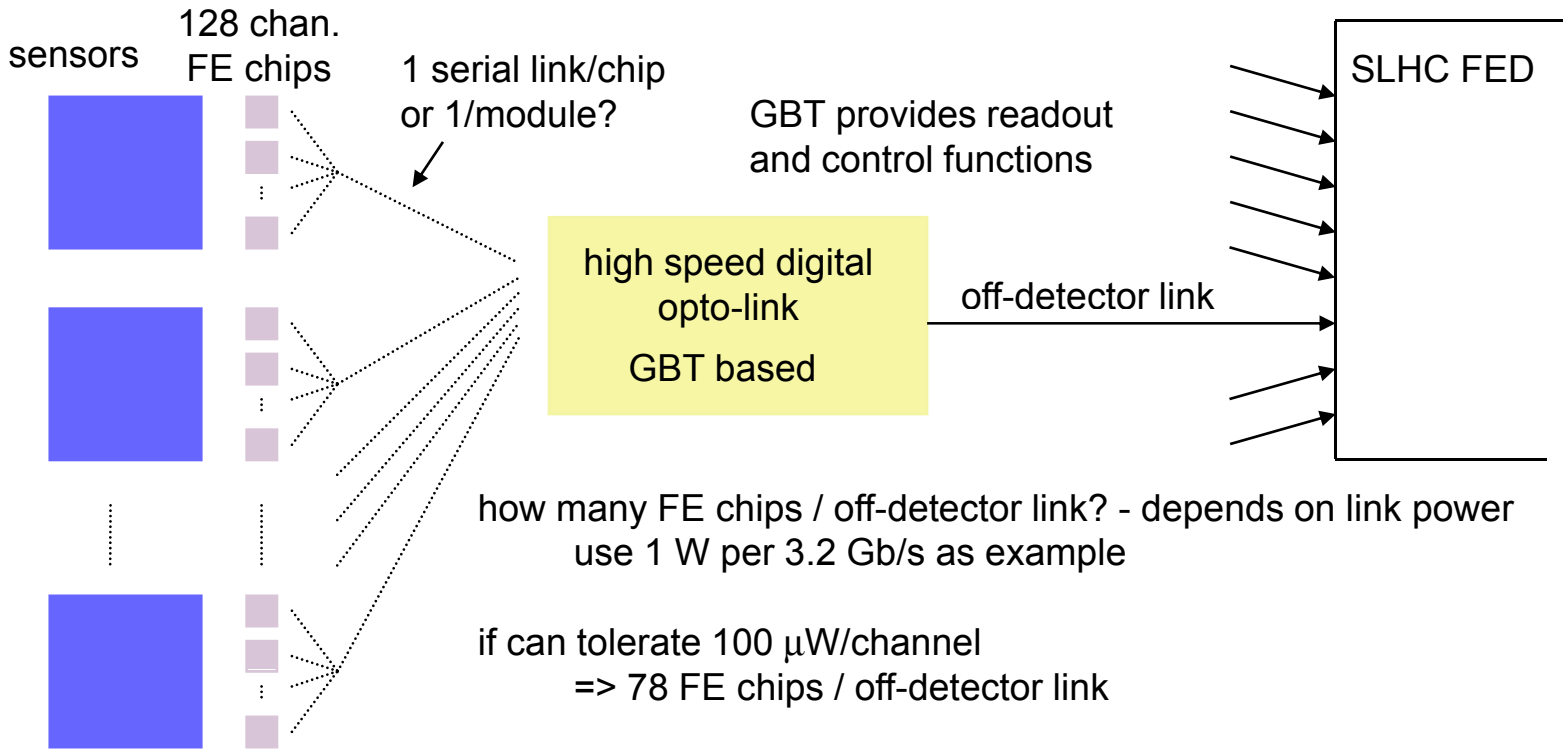
OK for strips < few cm
preamp power 78μW
overall preamp/shaper power
0.12 mW
factor ~8 reduction from APV25

not a rigorous design study here – but encouraging
may end up with output stages dominating overall
channel power for this type of architecture





further up readout chain?



how many FE chips / off-detector link? - depends on link power
use 1 W per 3.2 Gb/s as example

if can tolerate 100 μW/channel
=> 78 FE chips / off-detector link

need to ship data/trigger off-detector in less than 10 μsec (ave. L1 spacing)
=> < 32,000 bits available for 78 chips
< 410 bits / FE chip

implies sparsification on FE chip required
e.g. 6 bit ADC/chan x 128 chans. = 768

CMS/Atlas collaboration

some common SLHC projects already in place

opto-links

Atlas/CMS working group on optical links

control and readout system

GBT (Gigabit Bidirectional Trigger and Data Link)

– timing, trigger, slow control and data transmission

talks at this workshop

0.13 μm technology access

lots of help available through CERN – MPW runs now possible

common IP blocks (suggestions from A. Marchioro)

analog

- voltage reference
- internal linear regulator
- temperature sensor
- simple 8 bit DAC – bias generation

digital

- LVDS I/O pads
- PLL/DLL
- Error correction blocks
- Ethernet ports
- I^2C master/slave

maybe CMS/ATLAS can share useful, characterized circuits, and add to common blocks

perhaps other common circuit examples will emerge as chip designs begin

CMS/Atlas collaboration

interconnect

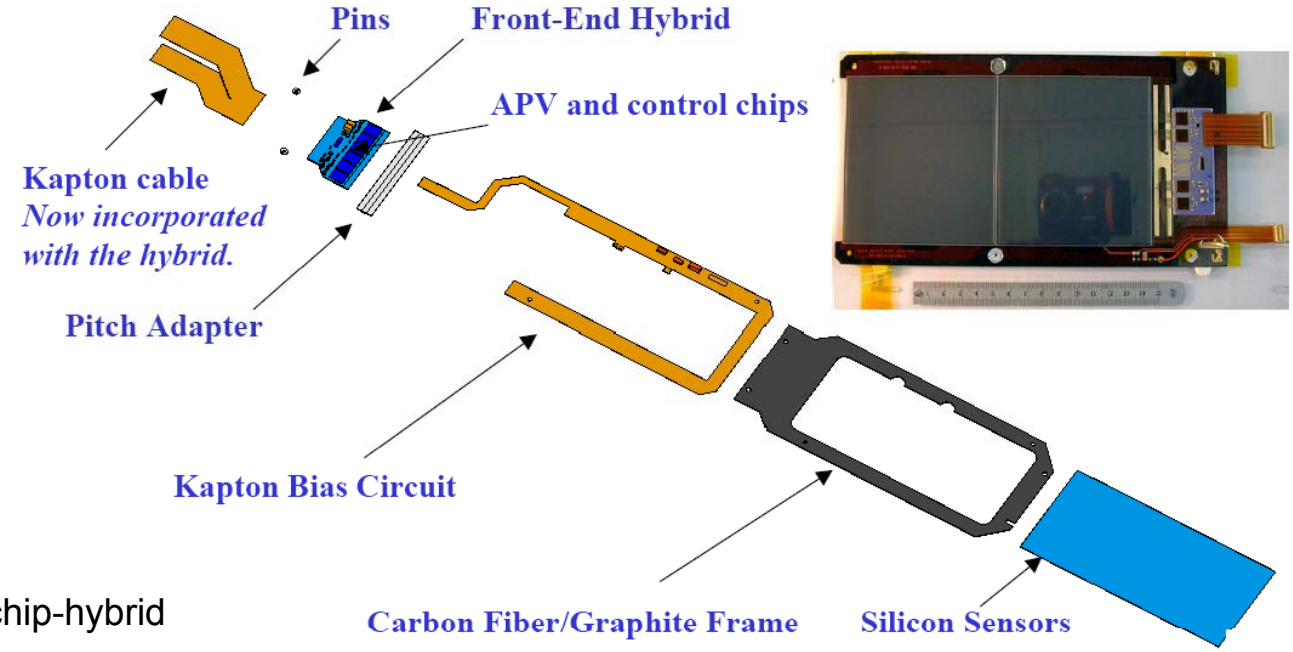
no clear CMS concept yet for physical design of modules
e.g. sensor/FE chip/hybrid interconnection

existing CMS tracker:

26 different module types
14 types of sensor
24 types of pitch adapter
3 types of hybrid
19 types of frames
~25M wire bonds

can we simplify for SLHC?

less sensor variants?
PA on sensor?
bump-bonding? – sensor-FEchip-hybrid



are there any common SLHC solutions here?

CMS/Atlas collaboration

several talks at this workshop

powering schemes have implications for FE chips

serial powering: modules at different DC levels
=> AC coupling - DC balanced serial interfaces

parallel powering: local DC-DC conversion – more conventional module powering
supply noise rejection issues
- lowest power FE chip architectures less likely to have good supply rejection

CMS FE chip designers need to get more involved here
follow and participate in developments and evaluate different schemes

conclusions

timescale short – CMS tracker SLHC electronics R&D activity needs to ramp up

front end chip architectures need more study
- final architecture not clear - need results of more detailed design studies
- emphasis on power – may find that chip back ends start to dominate

some ATLAS/CMS collaboration already exists in key areas
- – maybe more possible, particularly in interconnect and powering

extra

plans

proposed SLHC upgrade date 2015 (~ 8 years away)

large scale manufacture of components has to start **much** sooner
=> need tested solutions ~ 2010/11, ~ 3 years away

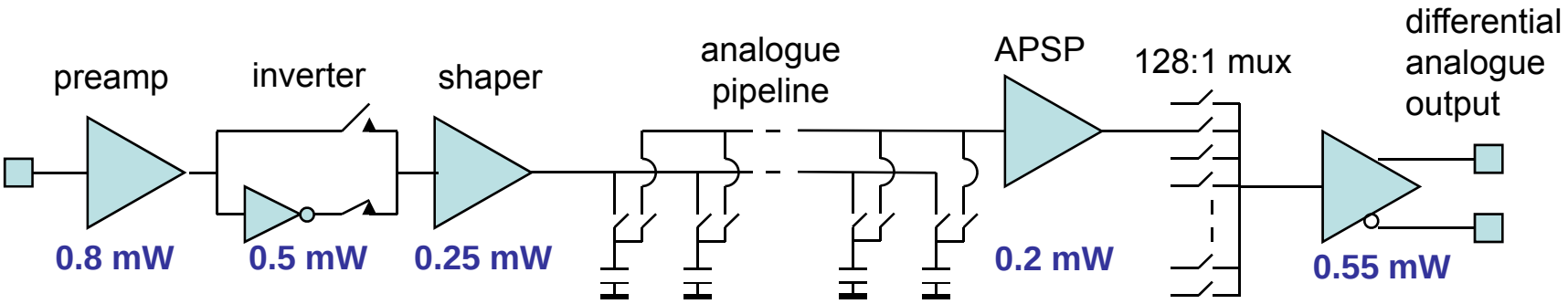
CMS planning 3 year front end chip development program

year 1: test structures
different front end designs for different sensor choices (polarity, strip length, AC/DC coupling)
low power ADC architectures, other test structures, …

year 2: FE chip prototype
develop full readout chip (could still have front end amplifier variants)
use to evaluate different sensor options

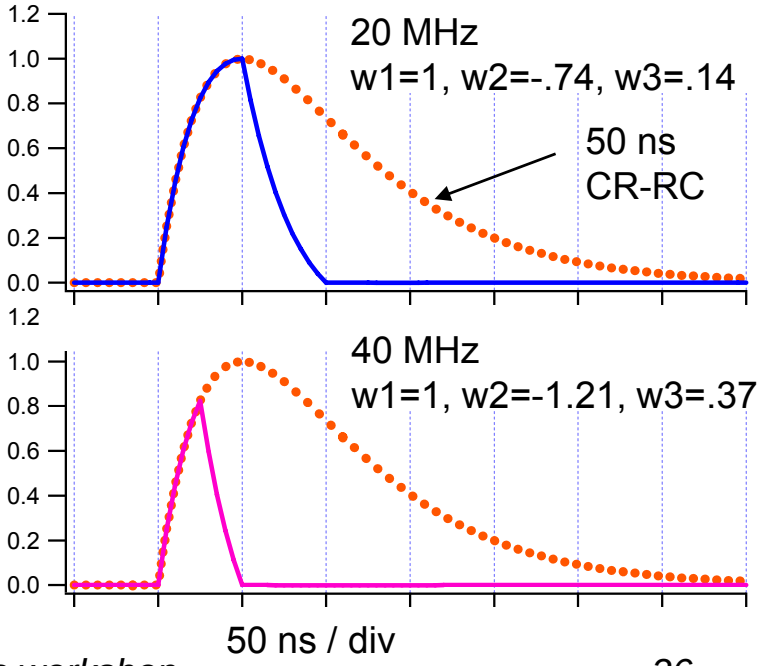
year 3: pre-production prototype
final architecture choice will depend on:
outcome of previous 2 years prototyping
evolving system definition

coping with 25 nsec bunch crossing?



implementing deconvolution in APSP pipeline readout circuit
- gives single bunch resolution with no extra power
  - (you need something to read pipeline out anyway)

relevance to SLHC?
- switchable weights to APSP could allow 20/40 MHz bunch crossing frequency adaptability without much extra complexity

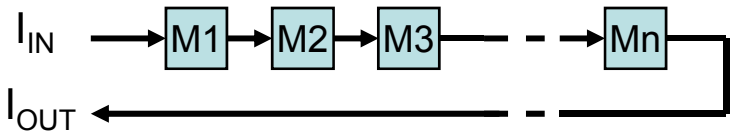


Power provision

0.25 μm -> 0.13 μm

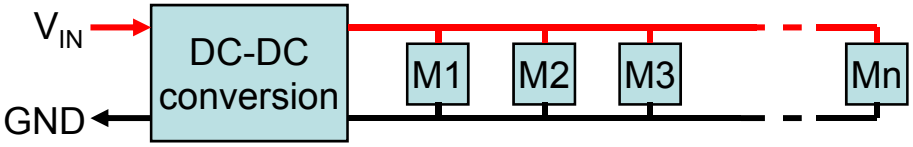
chip supply voltages halve, so currents double for same power consumption
=> 2x power dissipated in cables and 2x voltage drop along cables
solution is to deliver power at higher voltage (lower current)
=> local DC-DC conversion or serial powering -> both have implications for FE chip

serial



chain of modules at different DC voltages
linear regulation on each module
AC or opto-coupling of signals (readout & cntrl)

parallel



module powering more conventional
DC-DC conversion the main issue
FE chip supply rejection issues?

see DC to DC Power Conversion, Ely and Garcia-Sciveres, LECC 2006 (Valencia)

0.13 μm input transistor choice

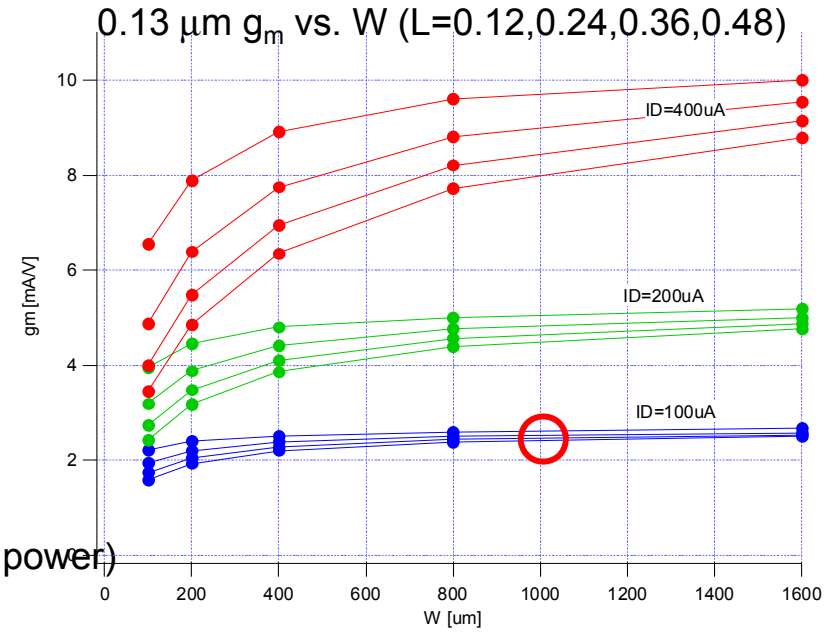
input device choice determined by:

speed: O/P risetime goes as C_{DET}/g_m
thermal noise: goes as $C_{DET}/\sqrt{g_m}$

C_{DET} ∝ strip length so lower g_m possible

allowable bias currents put 0.13 μm devices in W.I.

gm ∝ I_D with very weak W/L dependence



rigorous (complicated) optimisation required (including power)

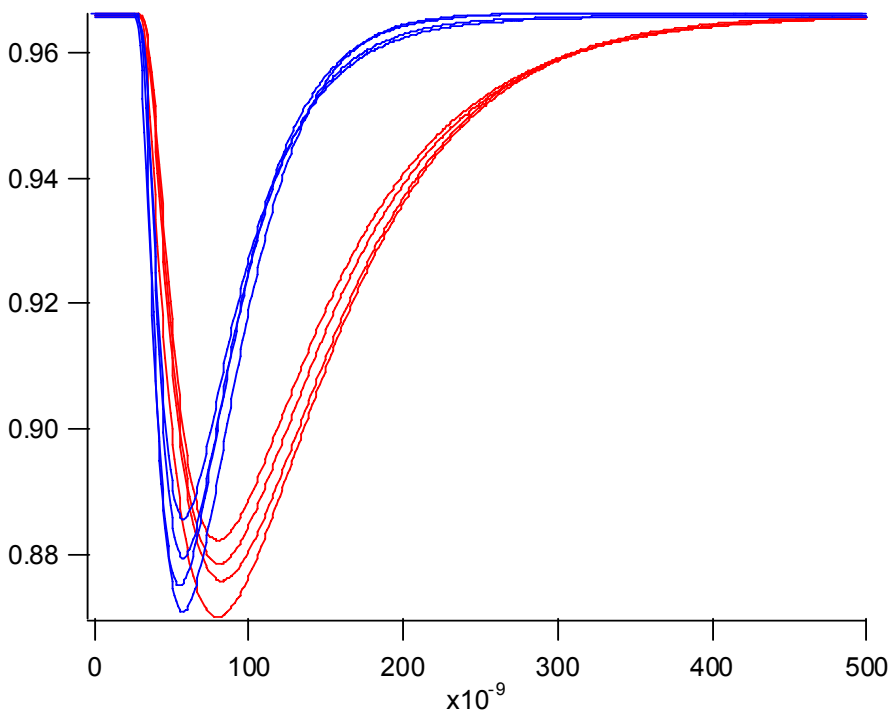
make some simple choices here

lets say C_{DET} reduces factor 4, => g_m can also reduce factor 4 (so noise slope increases factor 2)

choose W/L = 1000/0.24 here and I_D = 100μA, -> g_m > 2 mA/V (APV25 I/P device gm ~ 8 mA/V)

50/25 nsec

50/25 ns pulse shapes for different C_{DET} values



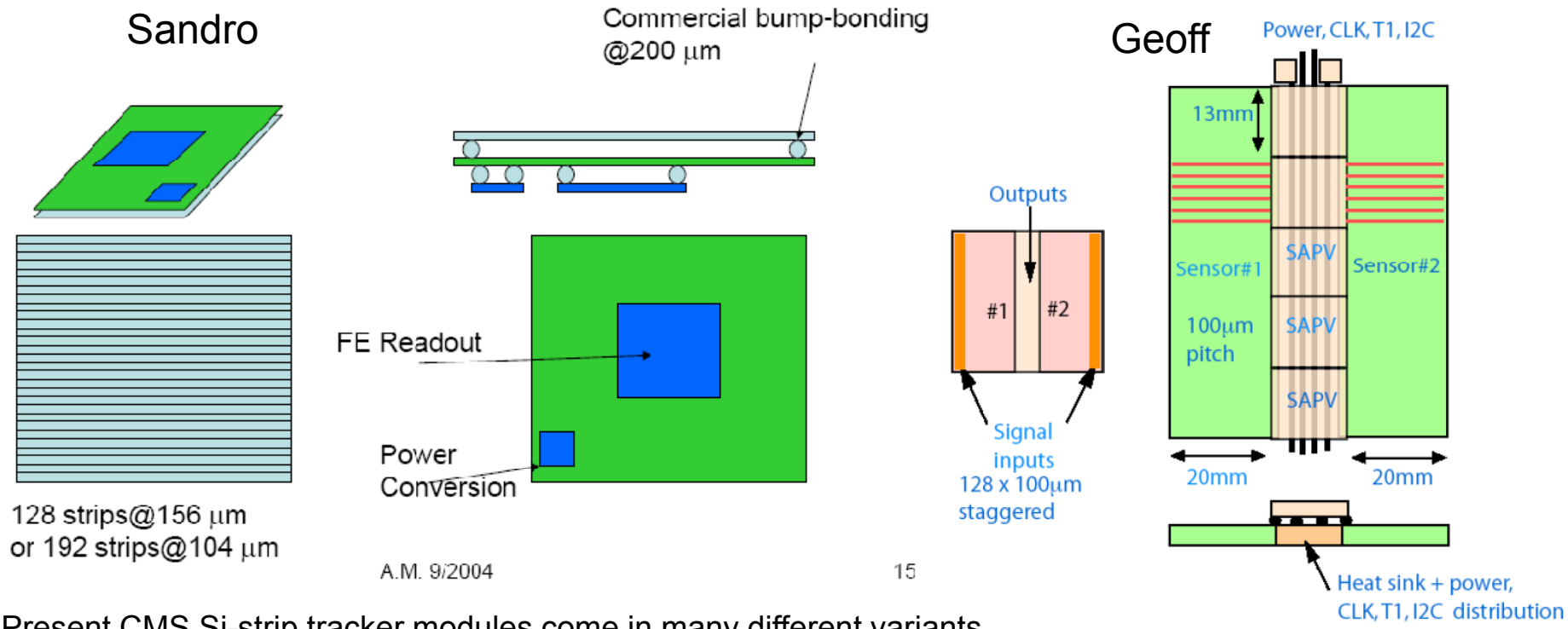
is 25 nsec pulse shape possible without changing shaper transistor dimensions?

yes - can speed up pulse shape using Isha/vfs only

but power penalty

C_{DET}	isha(50ns)	P[μW]	isha(25ns)	P[μW]
0	10	12	20	24
4.5	10	12	25	30
9	12	15	35	42
13.5	14	17	50	60

straw man detector module designs



Present CMS Si-strip tracker modules come in many different variants

different sensor pitches/shapes, different #'s of FE chips/ module, different mechanical designs

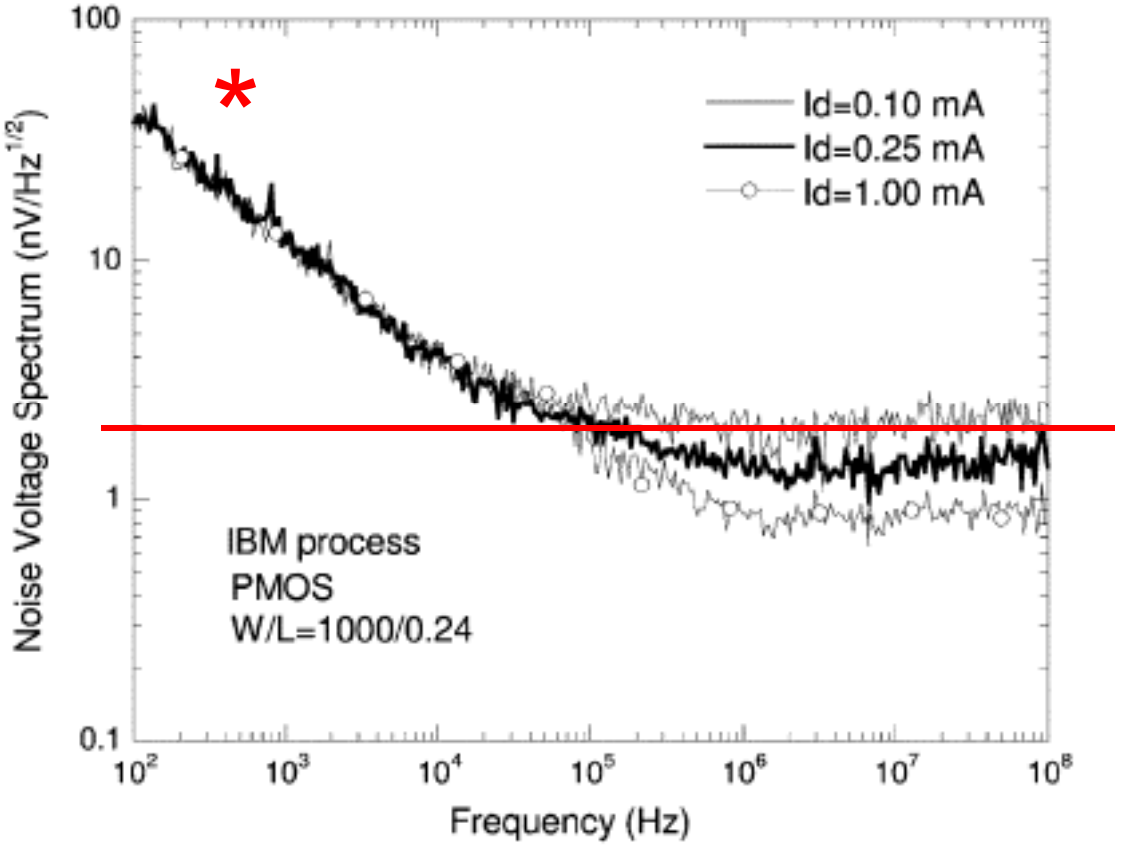
What will SLHC Si-strip modules eventually look like?

don't know, but things to consider are how much can be sacrificed for manufacturability

bump-bonding is one common theme in above examples

Choices here will affect final FE chip design (but maybe not crucial to know the answers now)

W/L = 1000/0.24 noise spectral density measurement



2 nV/√Hz @ 100 μA

** from Manghisoni et al, Noise performance of 0.13μm Technologies for detector front-end applications IEEE Trans.Nucl.Sci. Vol.53, no.4,Aug.2006 (2456-2462)*

pipeline gate capacitor leakage

APV uses gate capacitance for pipeline (~ 300 fF)

~60 pA @ 1V for 200μm²

=> 10 pA for 33 μm² (0.5 pF)

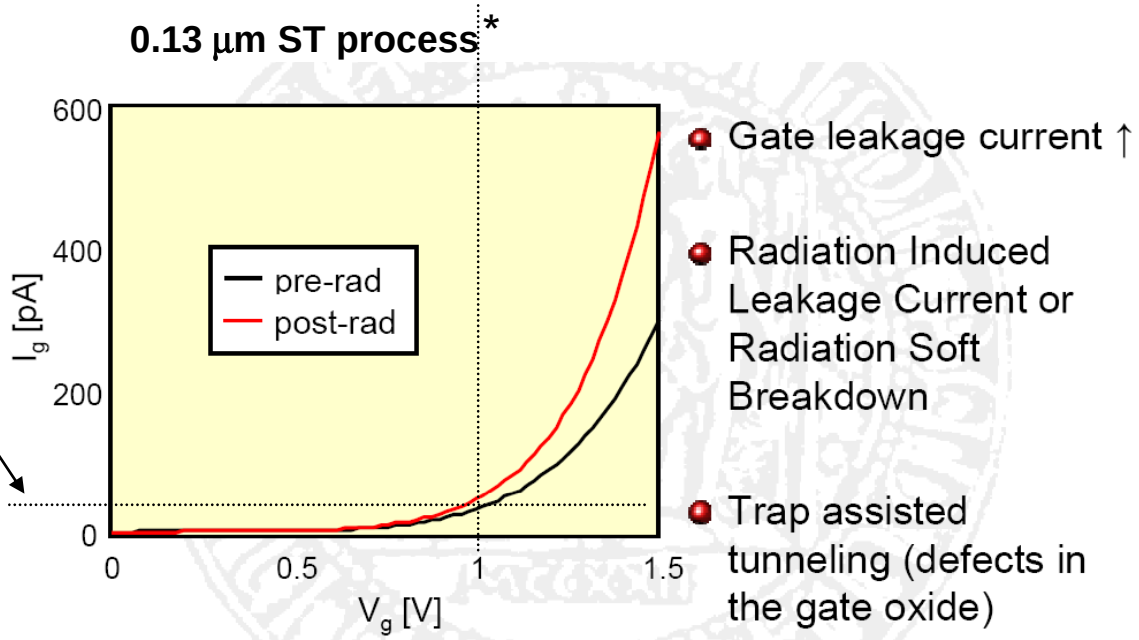
=> 20 μV / μsec (I / C)

=> 2 mV droop over 100 μsec

probably not a problem, but should take care

try and avoid more voltage across gate than necessary

will get worse for deeper sub-micron



Array of NMOSFETs with total gate area = 200 μm², Φ = 10^{16}p/cm²

* From S.Gerardin, Effects of irradiation on 130 nm CMOS, 4th CMS SLHC workshop, Perugia