Atlas ABCNext/SiGe

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Joint effort by:
CERN
Geneva University
Krakow - AGH
Santa Cruz - SCIPP

Supported by majority of
SCT Institutes

Strategy

- **Address in the ASIC design all system aspects from the very beginning.**

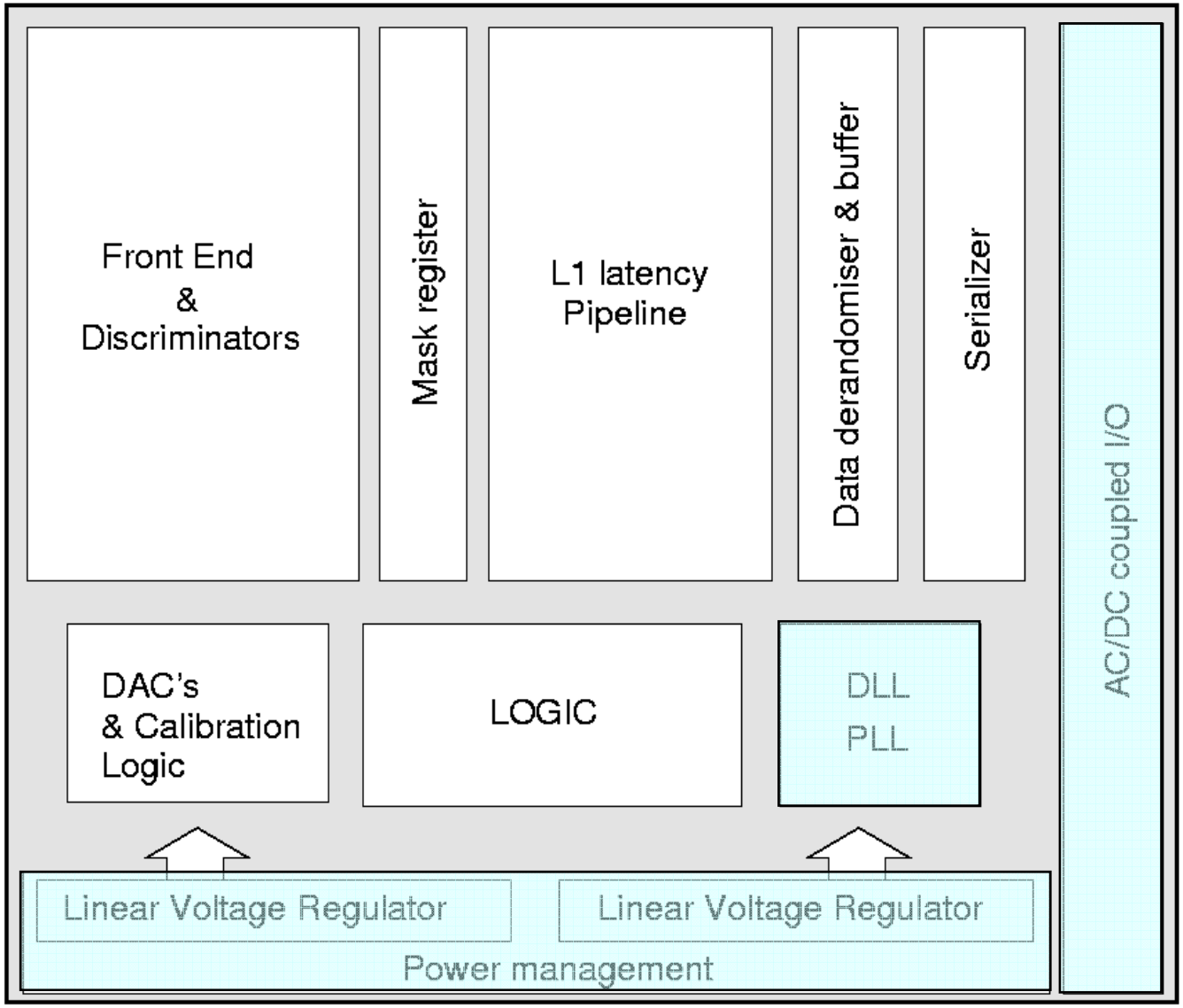
- **It should help to avoid situations „let others to solve the problem”, e.g. cooling and power.**

- **Provide a test vehicle for R&D work on sensors and modules/staves development.**

- **Develop a fully engineered ASIC with full architecture in the 0.25 μm CMOS technology first.**

- **Progress with investigation of new technologies, 130 nm CMOS and SiGe, in parallel.**

ABCNext architecture



Sensor requirements

- **Strips are 2.4 cm and 9.7 cm long, 75.6 μm pitch.**
- **The design should compatible with 25 ns bunch crossing and be able to cope with strip occupancy up to 4%.**
- **The design should be compatible with both signal polarities.**

The ABCNext design will be optimised for short strips as they represent most demanding requirements with respect to critical system aspects, like power budget, power distribution, hybrid and module design.

- **Maximum strip leakage current 1.4 μA**
- **The operating threshold of 0.5 fC after full irradiation, assuming collected charge of 11 000 electrons**
- **ENC of 750 e- after full irradiation including contribution from the detector leakage current**
- **Threshold matching below ~1/4 of ENC**

System requirements

- **Similar "core" functionality as for the present silicon strip tracker: signal amplification, discriminator, binary data storage for L1 latency, readout buffer with compression logic, and data serializer.**
- **Implementation of on-chip power regulation systems to enable the design of detector modules powered through serial powering scheme or using DC-DC converters.**
- **Increased data bandwidth up to 160 Mb/s.**
- **Delay adjustment of control and data signals.**
- **Immunity to SEU.**
- **Minimum power techniques in digital circuits.**
- **Readout of internal registers.**
- **The readout should be compatible with the present readout protocol as well as with a protocol assuming a module control chip.**
- **Compatibility with existing SCT DAQ hardware desired but not mandatory**

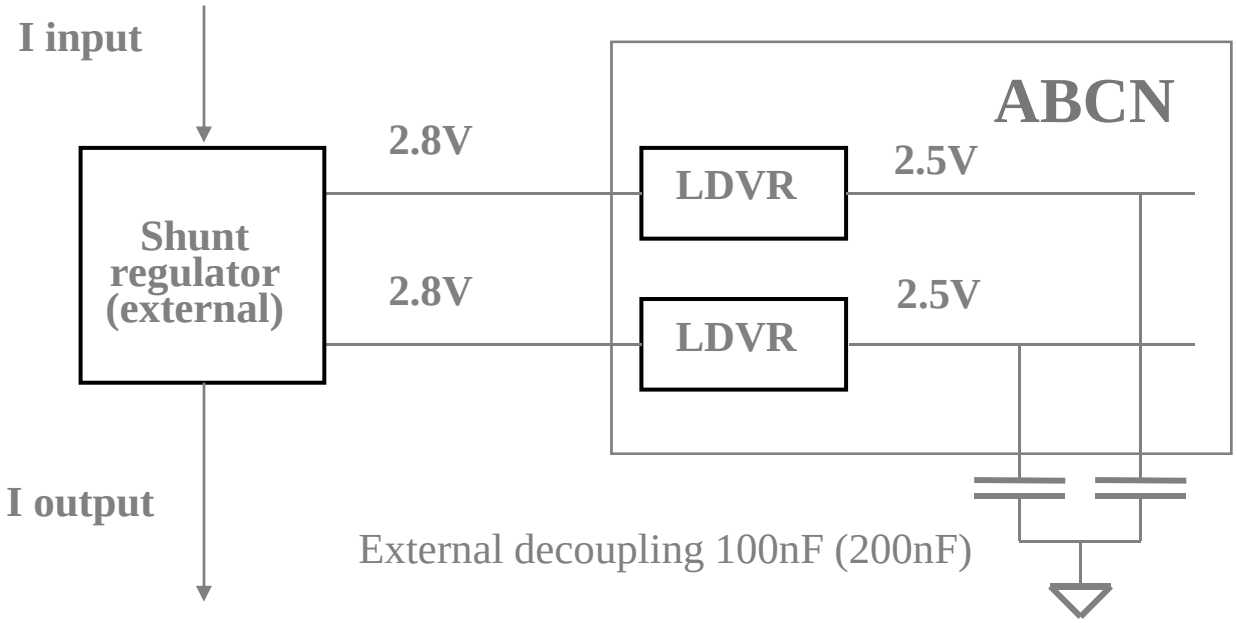
Command protocol

The command protocol as defined for the ABCD3TA does not need to be changed. Within the present protocol there are ~10 bits which are not affected. These bits can be used (for example to add new settings for the front-end) without modification of the present SCT DAQ hardware.

For the update functionality, the following features are considered:

- **Option for DC balanced transmission line coding (like bi-phase mark coding)**
- **Option to use a different fast L1 code for better error code immunity**
- **Separate slow control from L1 line and add an I/O channel in case large amount of slow control data related to SEU treatment may introduce additional dead time on L1**

Powering scheme

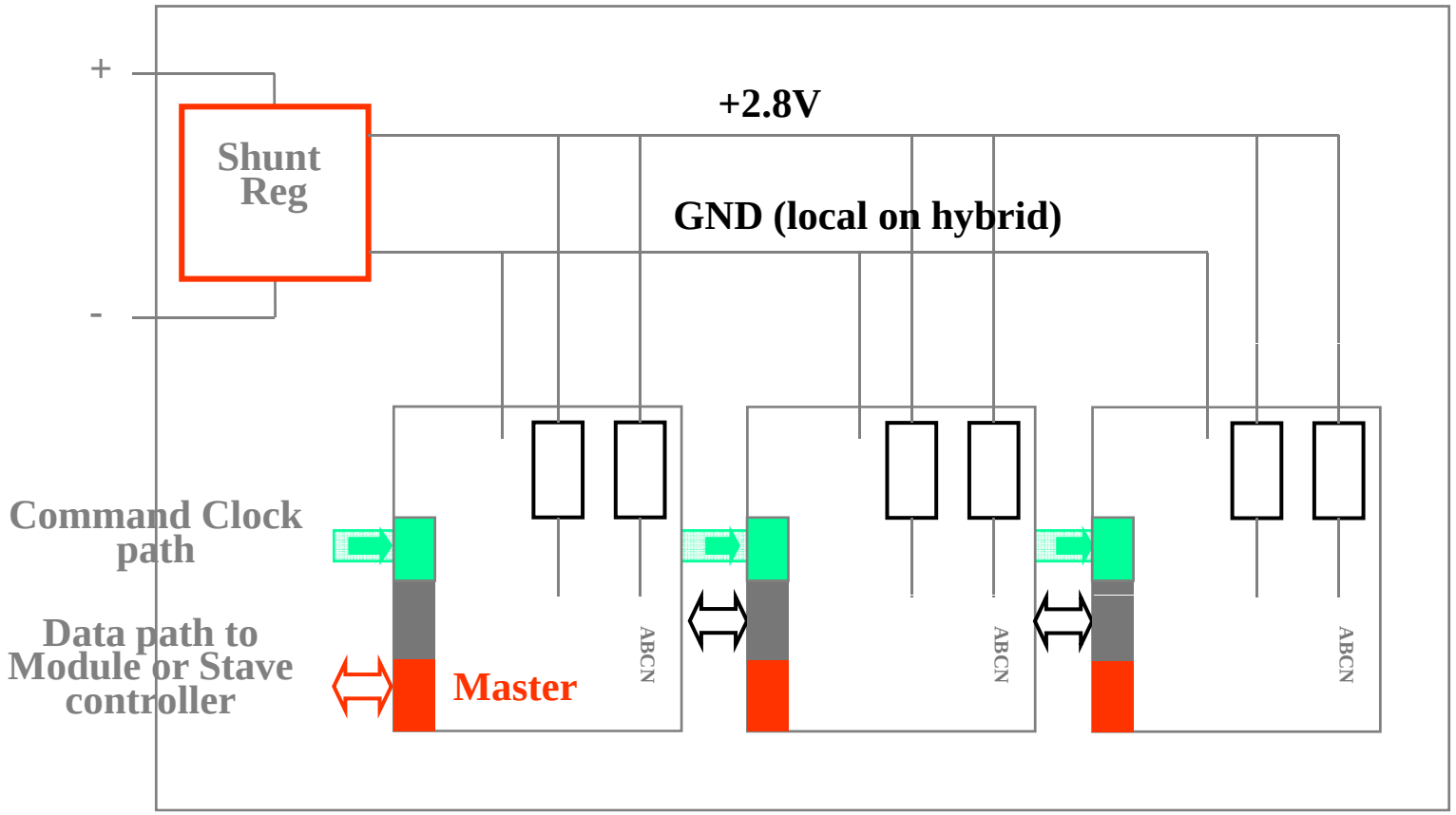


Each ASIC equipped with two linear regulators (for analog and for digital power)

External shunt regulator – one per module

External decoupling capacitors

Module internal connectivity



Physical requirements

There are two reasons to consider alternative floor-plans compared to the conventional ABCD-like one:

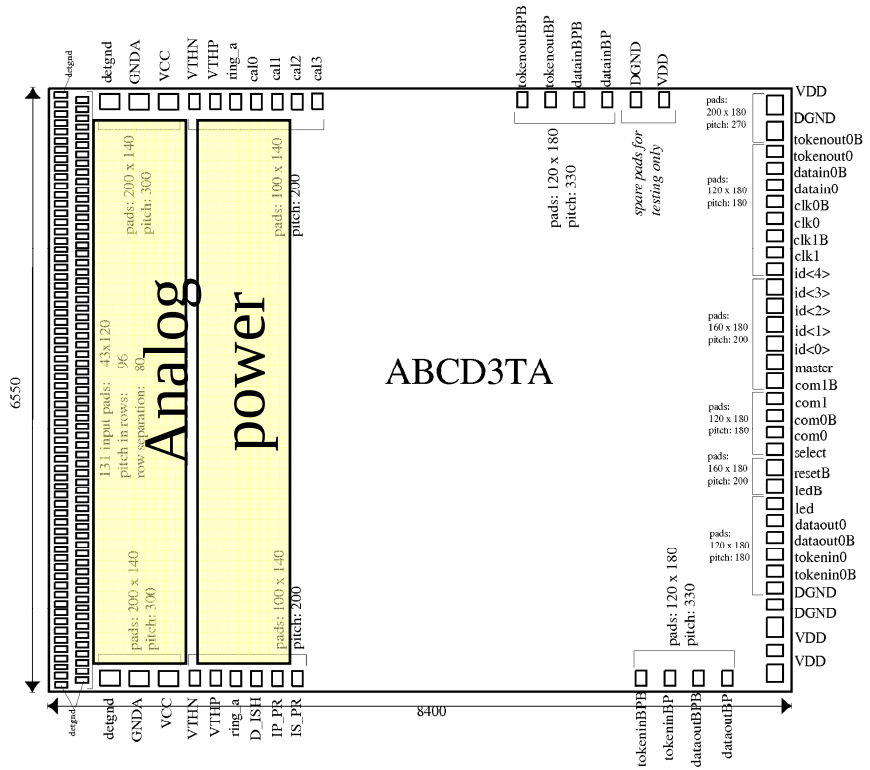
• Increasing the number of channels per chip, e.g. up to 256 would provide some power saving in common service blocks, digital blocks and I/O circuits.

• Hybrid developers would like to eliminate pitch adaptors and bonding pads on the sides.

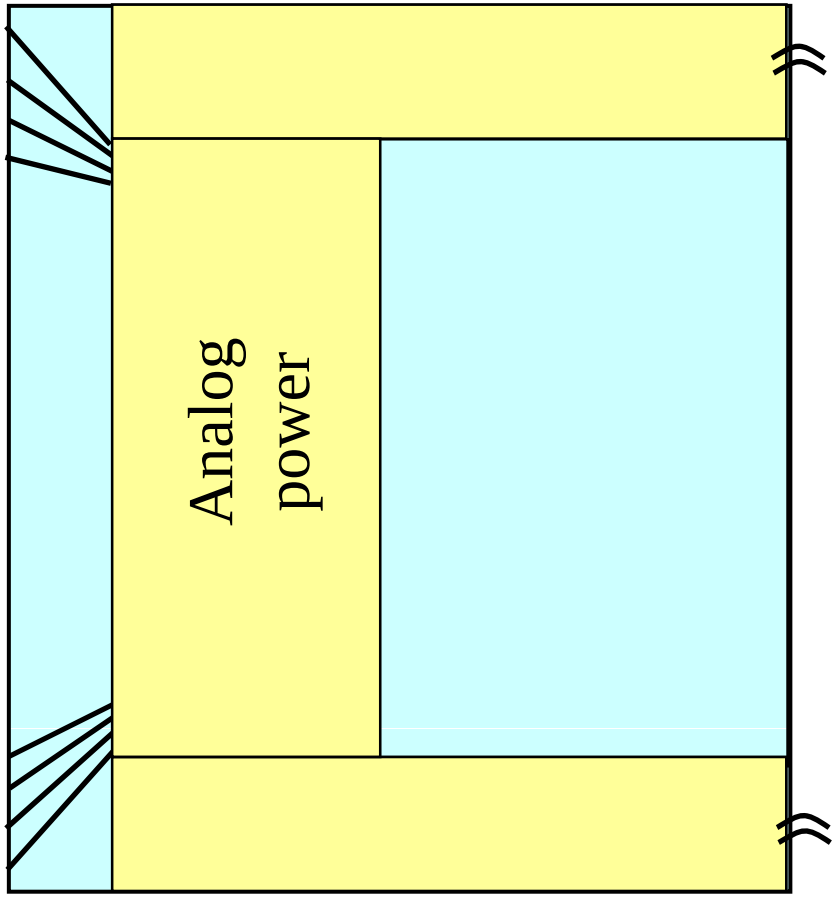
Distribution of analog power is critical – experience with SCT hybrids/modules shows that quality of analog power system should not be compromised.

Floor-plan

Floor-plan of present ABCD



Possible floor-plan of ABCNext



Towards 130 nm (digital)

- **The description of digital part of ABC-N is done in Verilog RTL code valid for 130 nm**

- **The main work when moving to 130 nm will be to expand the internal protections against SEU errors : all registers (incl. Test/Mask, TrimsDAC ?) triple vote logic, error detection with parity bit, Hamming code, etc …**

- **Other improvements are possible, like de-activation of clock on unused logic when in data taking mode, to reduce digital power**

Towards 130 nm (analog)

- **Analog blocks are :**
  - **Front-end amplifiers and discriminator**
  - **Calibration circuit**
  - **DACs**
  - **PLL and or DLL**
  - **Specific I/O**
  - **Regulators**
  - **Bandgap voltage reference**

- **Each of these blocks should be developed and understood before integration within a complete ABC-N 130nm chip.**

- **Some blocks are suitable candidates for being common projects between ATLAS and CMOS**

Towards 130 nm (analog)

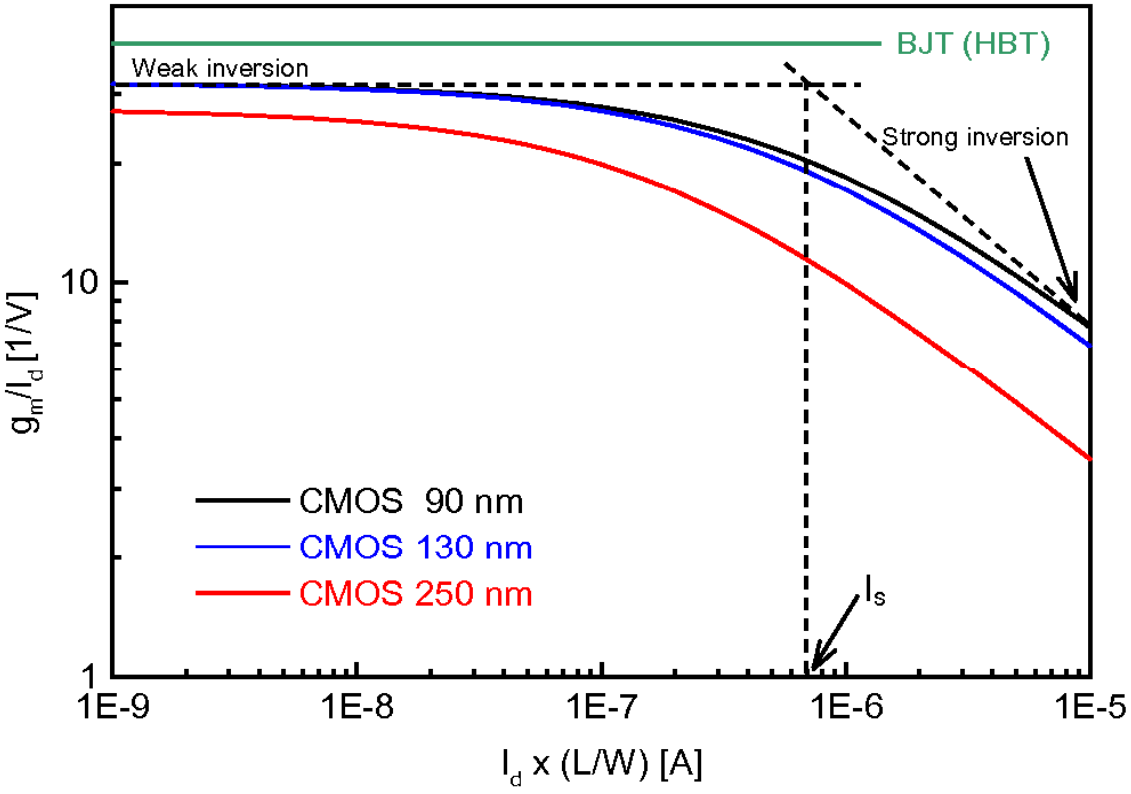
Front-end

- **MOSFETs in weak inversion are similar to BJTs**
- **Noise and radiation effects to be understood**

(these are obvious subjects for common projects)

$$\frac{g_m}{I_d} = \frac{1}{\sqrt{\frac{I_d}{I_s} + \frac{1}{2}\sqrt{\frac{I_d}{I_s}} + 1}} \frac{1}{nV_t}$$

$$\frac{\left.\frac{g_m}{I_d}\right|_{MOSFET}}{\left.\frac{g_m}{I_d}\right|_{BJT(HBT)}} = \frac{1}{n} \approx 0.77$$



SiGe Bipolar Option

Along with the 130 nm CMOS technology, IBM offers two silicon-germanium (SiGe) bipolar options (CMOS8HP and CMOS8WL) to allow full biCMOS ICs.

If these technologies are sufficiently radiation hard, a SiGe bipolar front-end may significantly reduce the power dissipation of the readout IC.

The 8WL is a less expensive option and may provide sufficient performance.

Bipolar specifications (nominal)

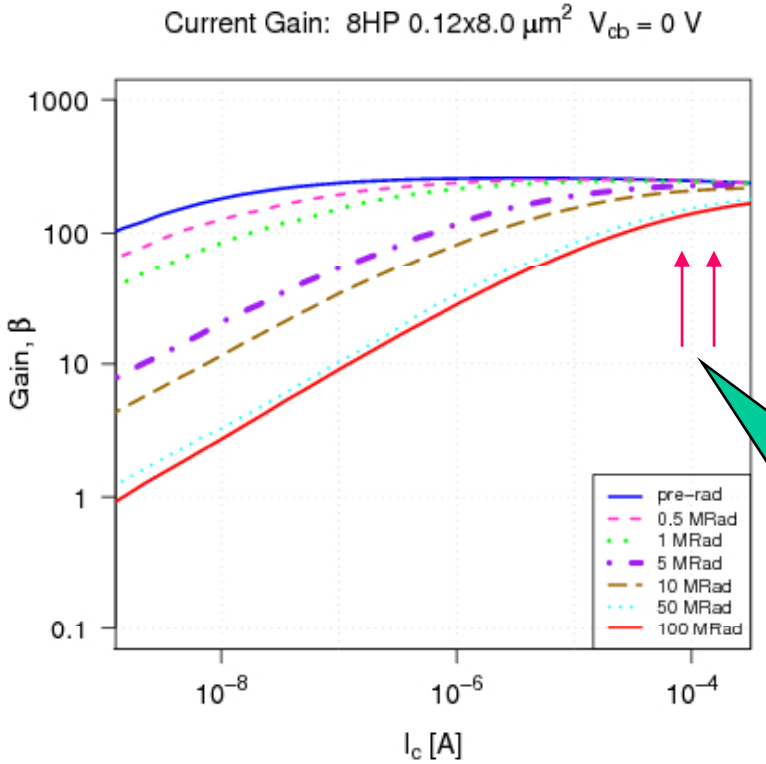
Process	SiGe 8WL			SiGe 8HP	
Device type	High performance	Medium performance	High breakdown	High performance	High breakdown
Beta	230	230	230	600	470
fT	100 GHz	65 GHz	45 GHz	200 GHz	57 GHz
BVcbo	8 V	13.5 V	15 V	5.9 V	12 V
BVceo	2.5 V	3.3 V	4.5 V	1.77 V	3.55 V

BNL, CNM Barcelona, IN2P3, UC Santa Cruz and U of Penn are jointly studying the radiation hardness of SiGe technology. There is interest for both the upgrade silicon tracker and the LAr calorimeter.

SiGe Radiation Studies

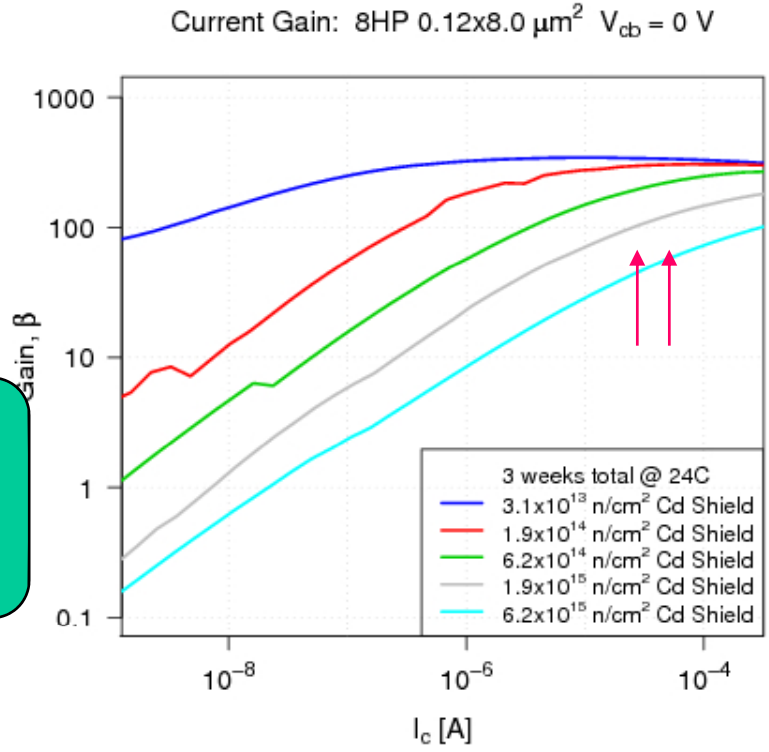
Irradiation studies of the IBM 8HP technology are in progress along with comparison studies of earlier generations and a separate German vendor IHP.

Gamma Irradiation



Arrows show typical bias for this large front transistor

Neutron Irradiation

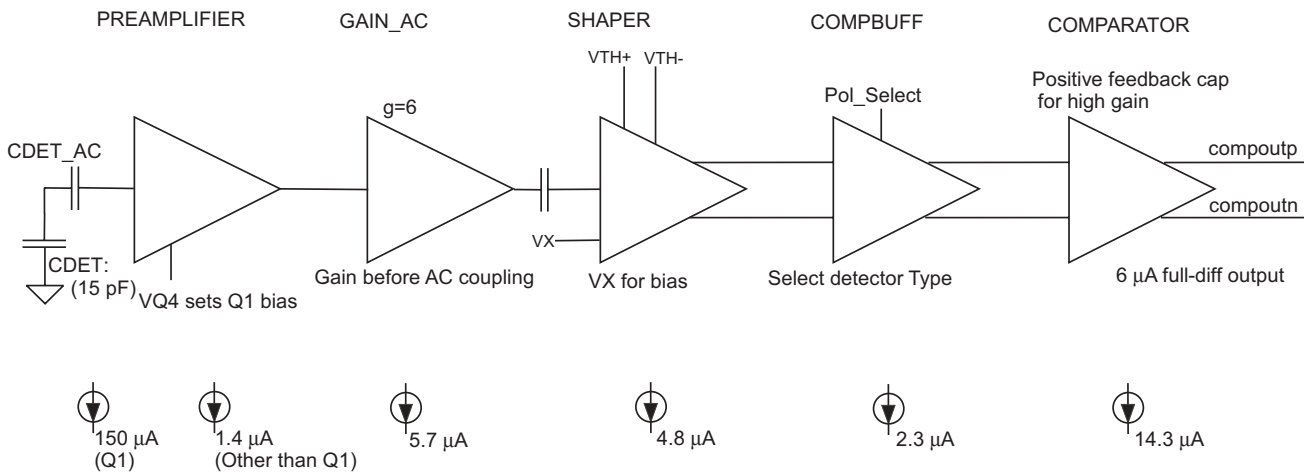


We are awaiting some 8WL parts for similar radiation studies.

Front-End SiGe Test Chip

To gain some experience designing with SiGe technology, UCSC designed a small test IC (the HRFE) using the IHP SG25H1 SiGe BiCMOS process through Europractice. This was an inexpensive test vehicle and roughly equivalent to IBM's first generation SiGe technology married to 0.25 μm CMOS.

HRFE ANALOG POWER SECTION

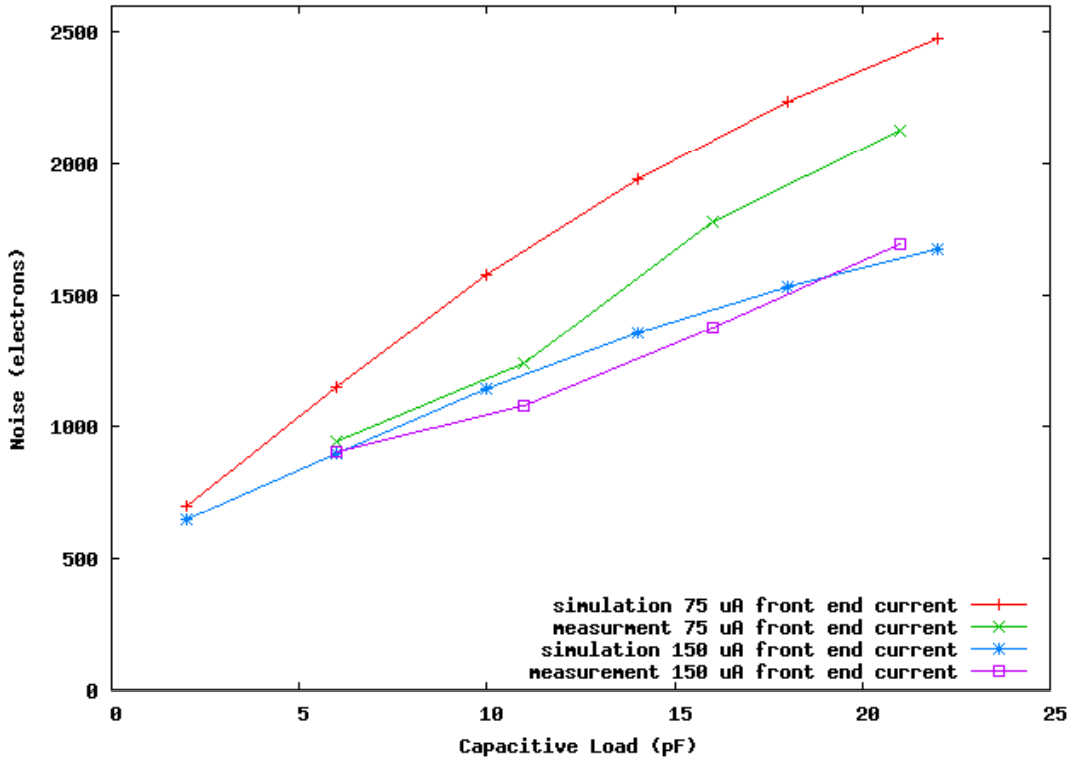


Total Current: 178.5 μA (1340 e- @ 150 μA and 15pF detector)
Total Power: 360 μW

Ned Spencer
UCSC, May 9, 2006

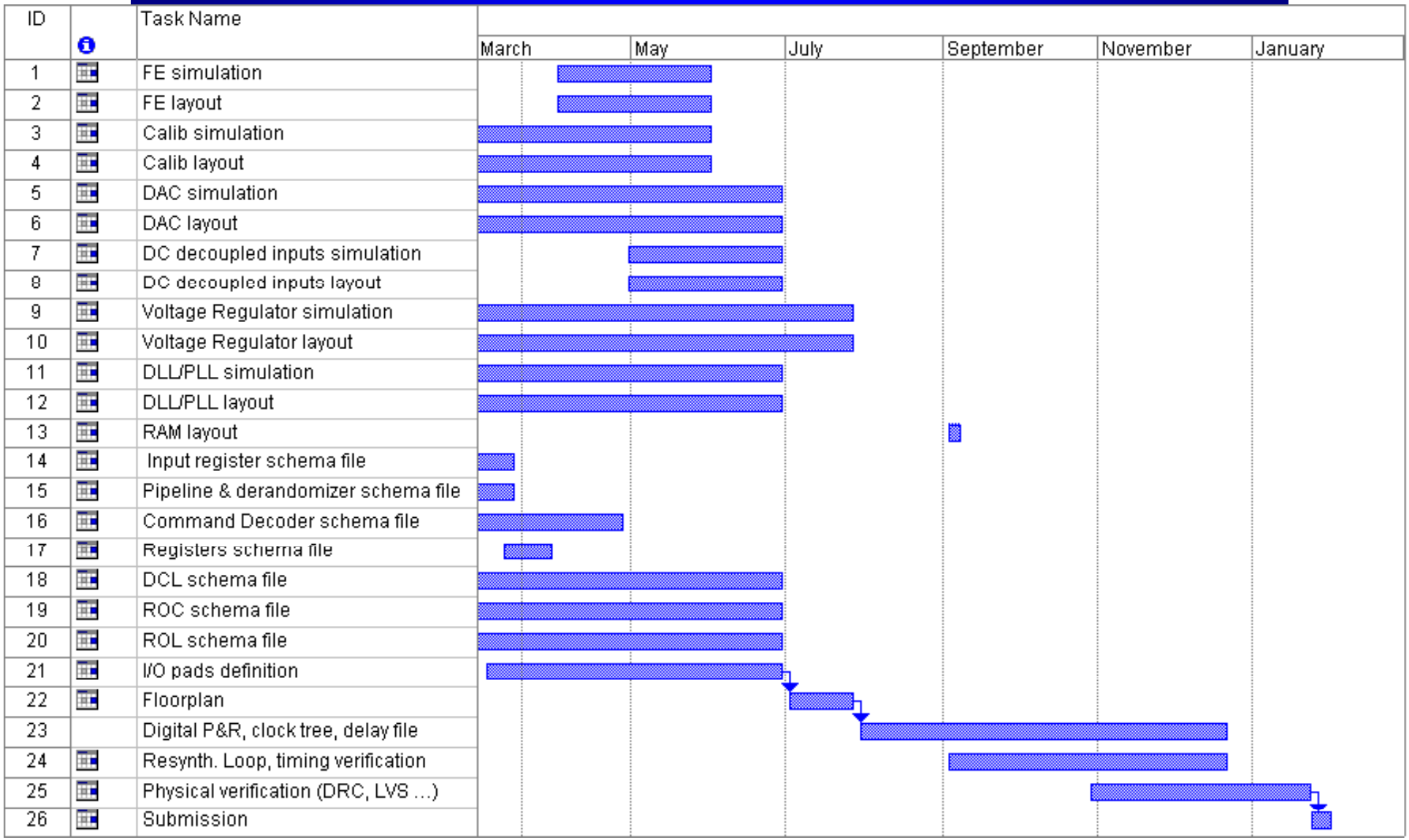
Measured vs. Simulation Results

Noise vs. Front-end Load was simulated and measured using two different bias settings for the front transistor as might be used for short and long strips of the upgraded silicon tracker.



The measured noise tracks (and is somewhat better than) the simulations showing that acceptable noise can be achieved at these very low power levels.

Short term schedule



Long term schedule

0.25um ABC-Next					
Step		Year 1	Year 2	Year 3	Year 4
1	0.25 μm ABC-Next design				
2	0.25 μm ABC-Next Availability				
0.13um Evaluation					
Step		Year 1	Year 2	Year 3	Year 4
3	0.13 μm CMOS selection				
4	0.13 μm Standard Cells				
5	0.13 μm Digital Design Tools and Design Flow				
0.13um ABC-Next					
Step		Year 1	Year 2	Year 3	Year 4
6	0.13 μm FE Prototypes				
7	0.13 μm Back End Prototypes				
8	0.13 μm ABC-Next design				
9	0.13 μm ABC-Next Availability				