The GBT

A single link for Timing, Trigger, Slow Control and DAQ in experiments

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CERN/PH-MIC

Project Participants

- CERN: PH-MIC & ED & ATE
- INFN: Bari, Bologna, Torino
- IN2P3: Marseille

Background & motivation

For the first generation of LHC instrumentation PH-MIC has participated in three projects:

- TTC
- GOL
- CMS Tracker & Ecal Slow Control

all using different optical links.

The expertise gained in these projects convinced us that a single optical link is possible and actually desirable to simplify systems, reduce costs and streamline maintenance and operation

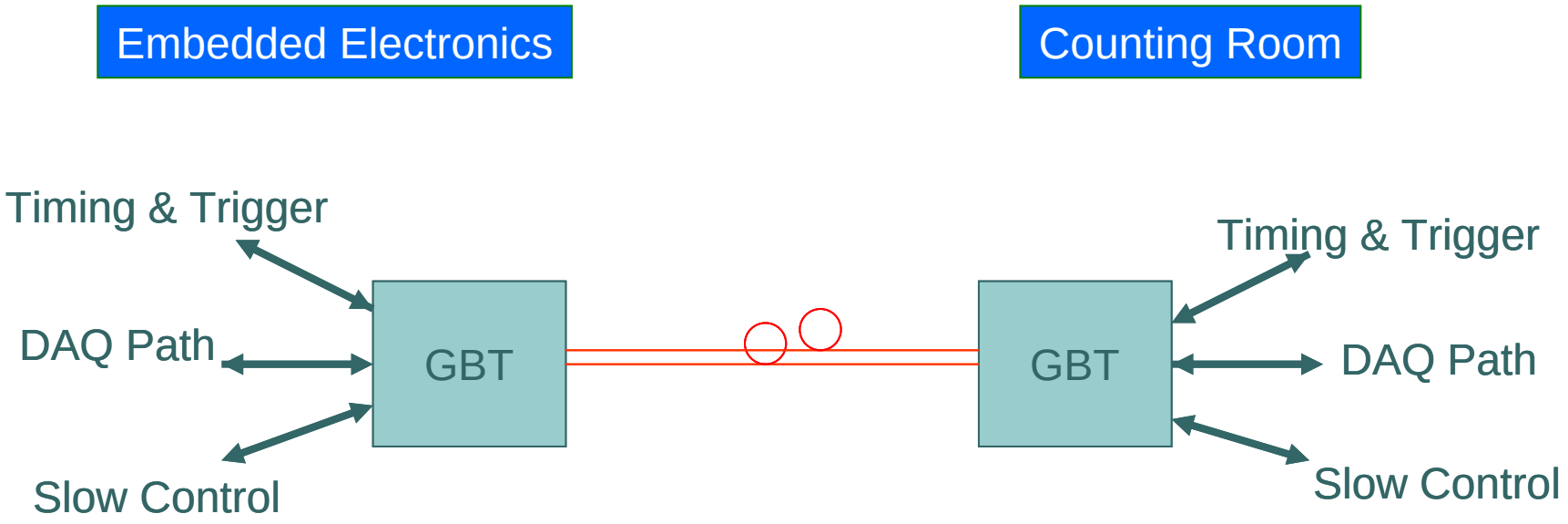
Rationale

- Cost of optical transmission system is largely dominated by the opto components (and their installation) and NOT by the electronic components
- Cost changes moderately when increasing speed
- Therefore: increasing design cost of electronic components has small if any impact on overall system cost but can lead to many advantages in terms of:
  - functionality
  - overall cost reduction
  - compatibility with industrial standards
  - simplification of long term maintenance
  - reduction of number of links

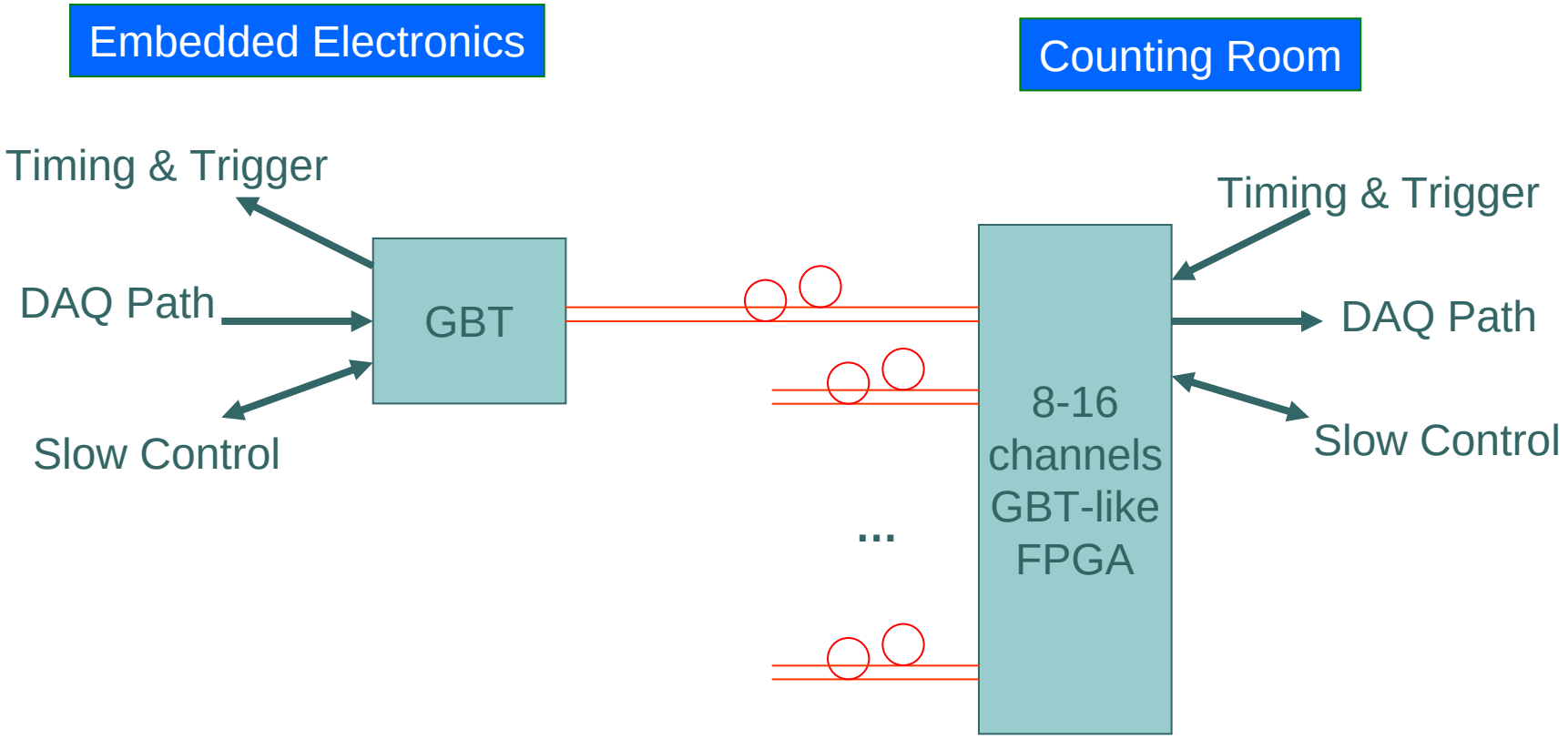
Outline

- General Aim of the Project
  - Architecture
  - Proposed TTC functionality
- Some details on proposed Error Correction
- Proposal for interface to Slow Control
- Progress & Plans

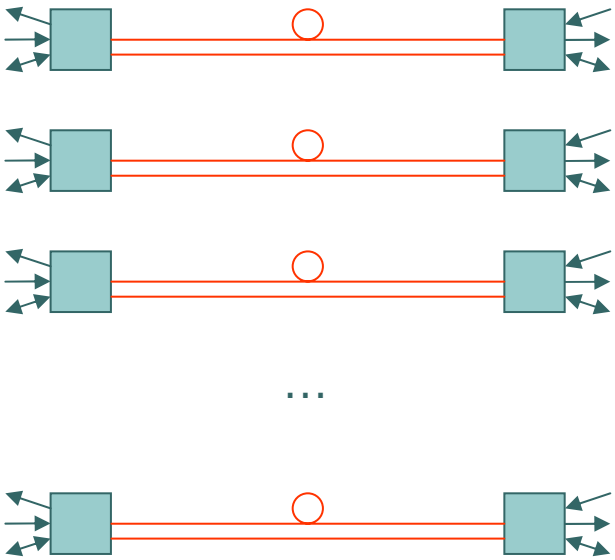
General aim


Embedded Electronics
Counting Room
Timing & Trigger
DAQ Path
Slow Control
GBT
GBT
Timing & Trigger
DAQ Path
Slow Control

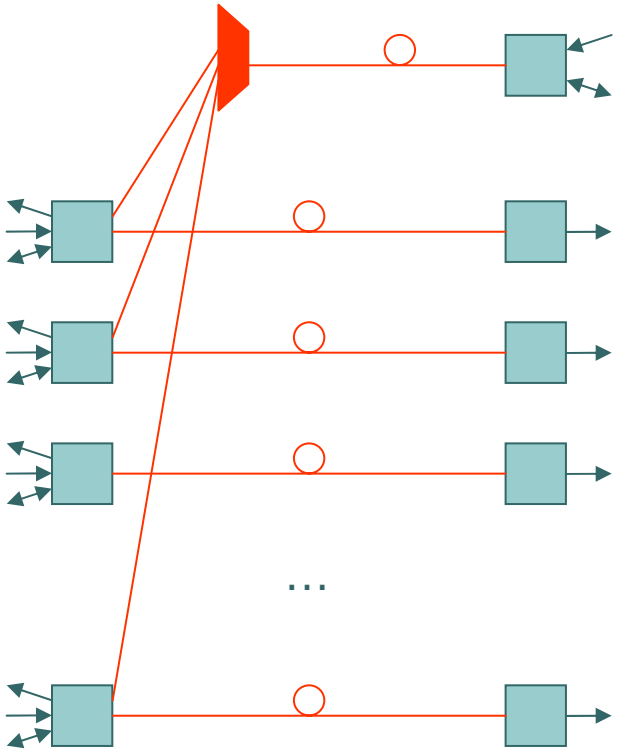
General aim++


Embedded Electronics
Counting Room
Timing & Trigger
DAQ Path
Slow Control
GBT
...
8-16
channels
GBT-like
FPGA
Timing & Trigger
DAQ Path
Slow Control

Architectural Options

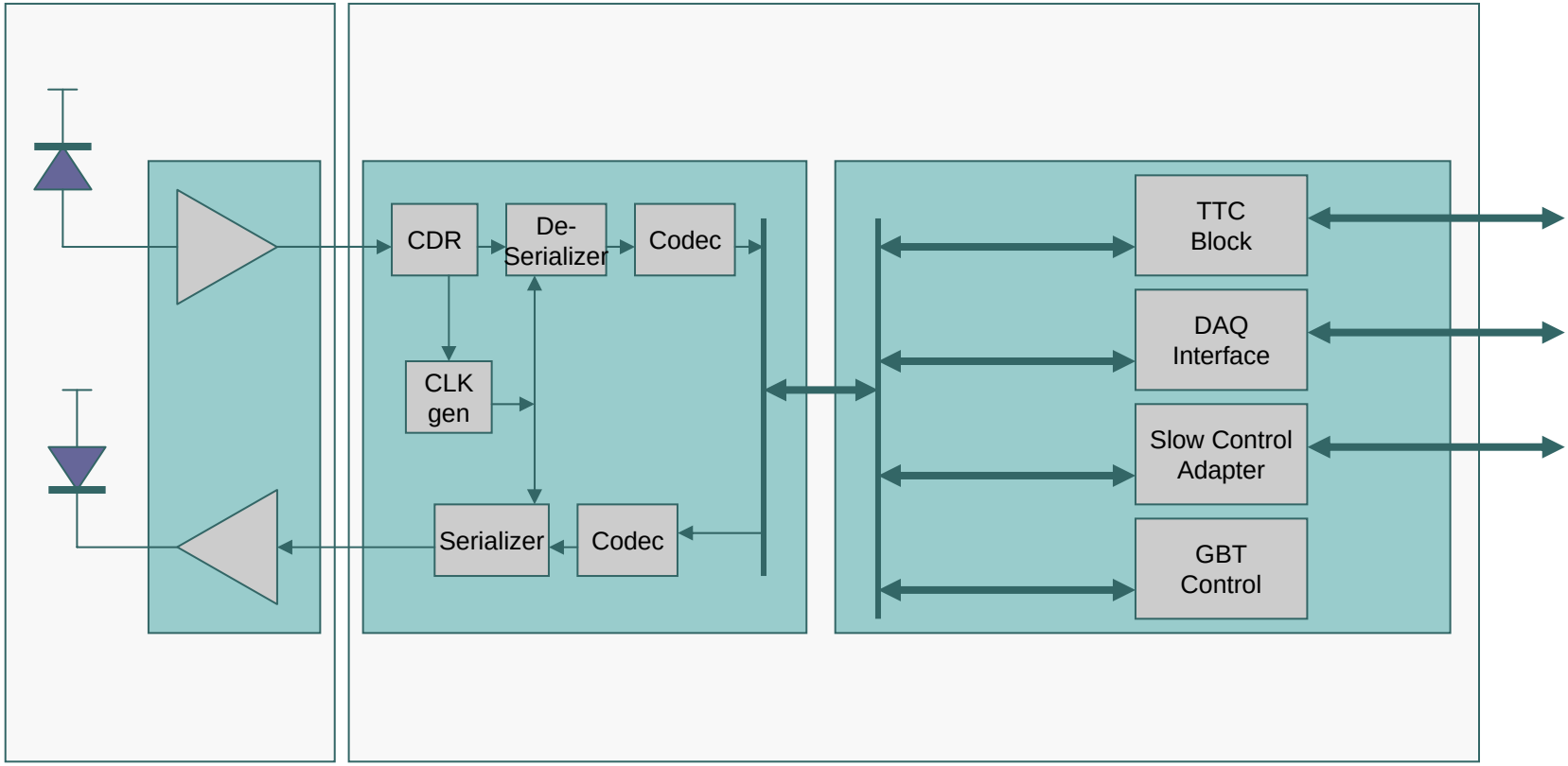


Straightforward P2P
Architecture +Technology

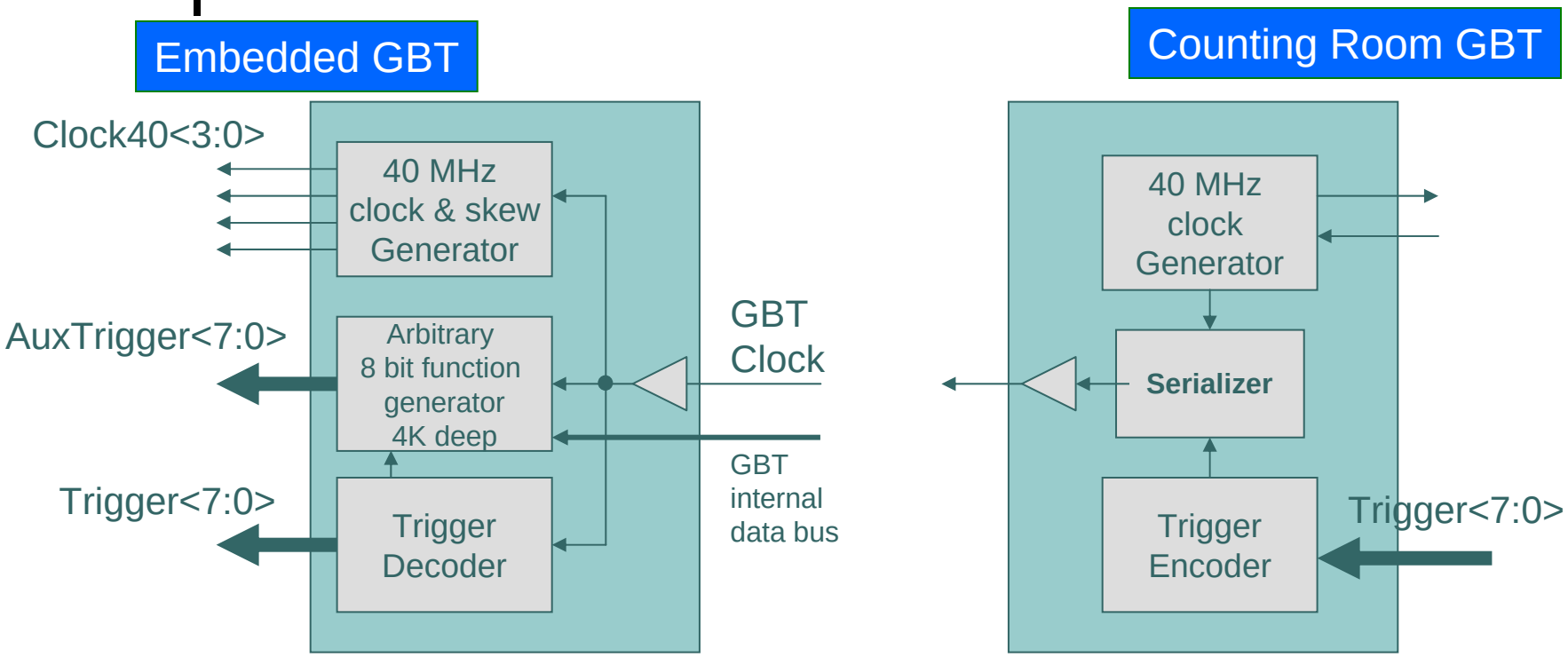


PON Derived
Architecture +Technology

GBT block Diagram



TTC Functionality



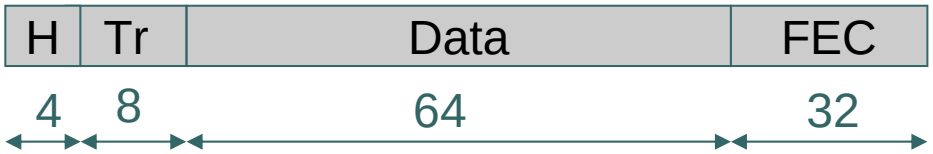
If the SLHC will finally run @ 20 MHZ, a function will be provided to gate the 40 MHz in a programmable manner

Error Correction in GBT

Objective for FEC

- Correct burst errors in link
  - Generated on the p.i.n. diode
  - Generated by particles hitting receiving PLL or any other circuitry causing momentary phase error
  - Generated in the receiver S/P register (which cannot be triplicated)
- Do this with minimal latency
  - Excludes certain FEC methods
- Achieve good efficiency
- Merge nicely with line-coding

Packet format



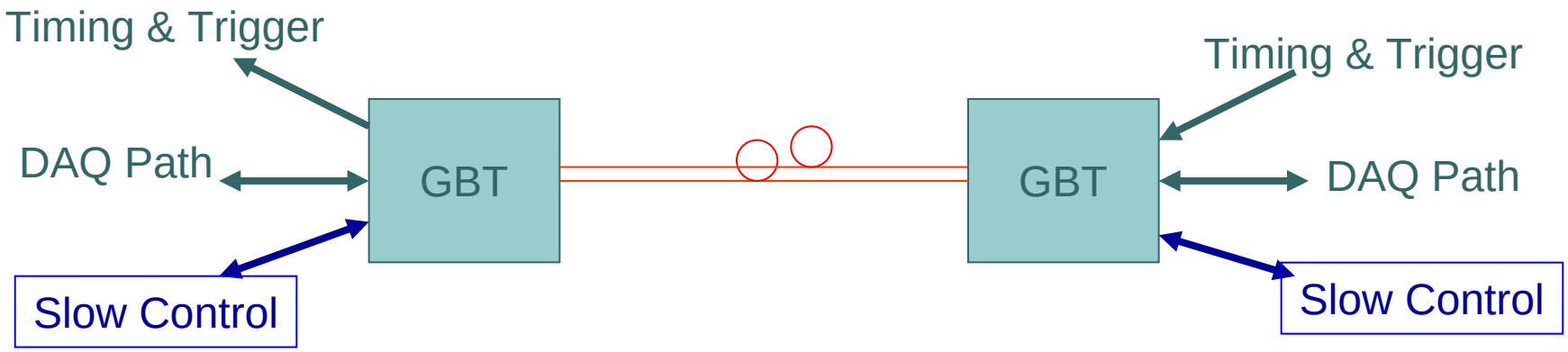
Coding proposed

- Fully FEC coded
  - 64 data bits, 8 trigger bits -> Total user bits 72
- Not coded
  - 4 header bits -> Total 76 bits
- RS(15,11) with symbols of 4 bits
- Coding/Decoding latency: one 25 ns cycle
- Interleaving: 2
- Error correction capability:
  $2_{Interleaving} \times 2_{RS}$ = 4 symbols, i.e. 16 bits
- Total bits used: 108 (= 76 + 32)
- Code efficiency: 73.3%
- Line speed @ 40 MHz/word = 4.32 Gbit/s

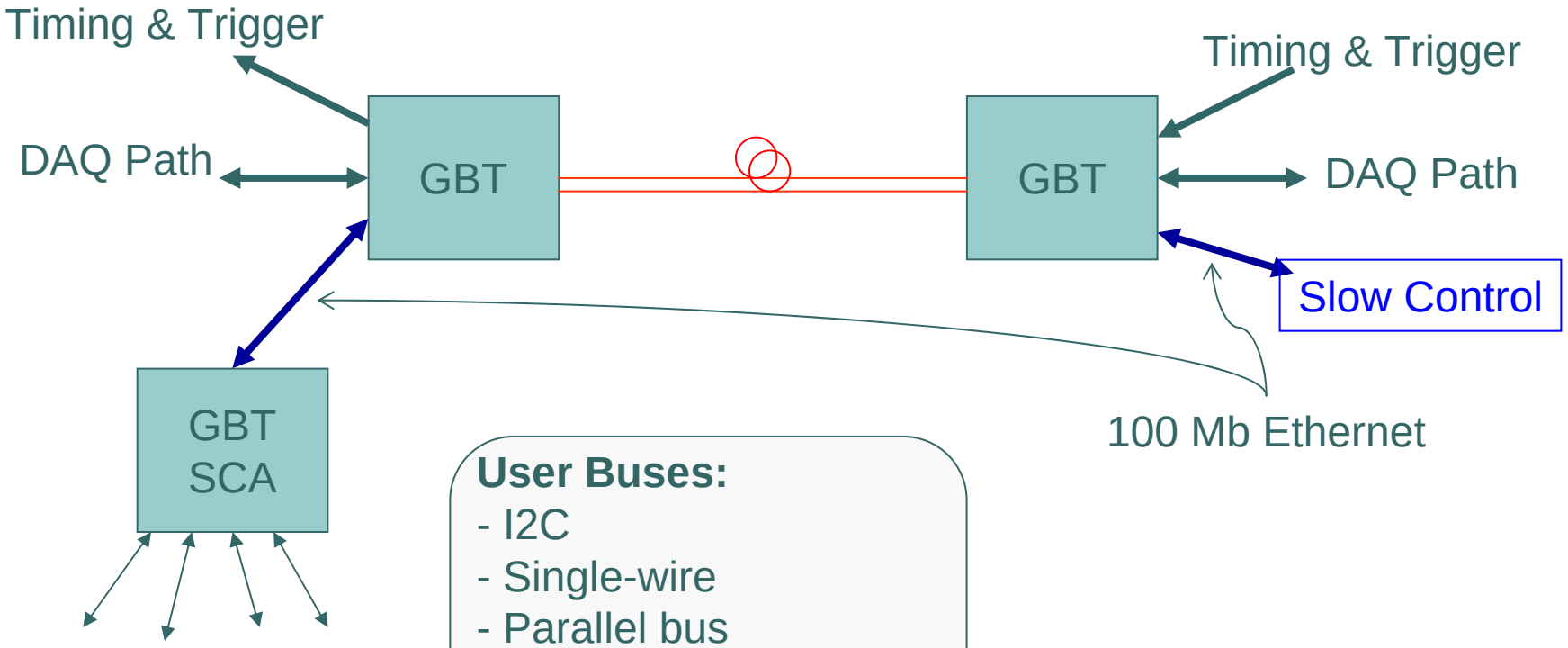
- Problem : does not match nicely with FPGAs, changes are likely, other similar schemes under evaluation

Interface to Slow Control

Slow Control Architecture

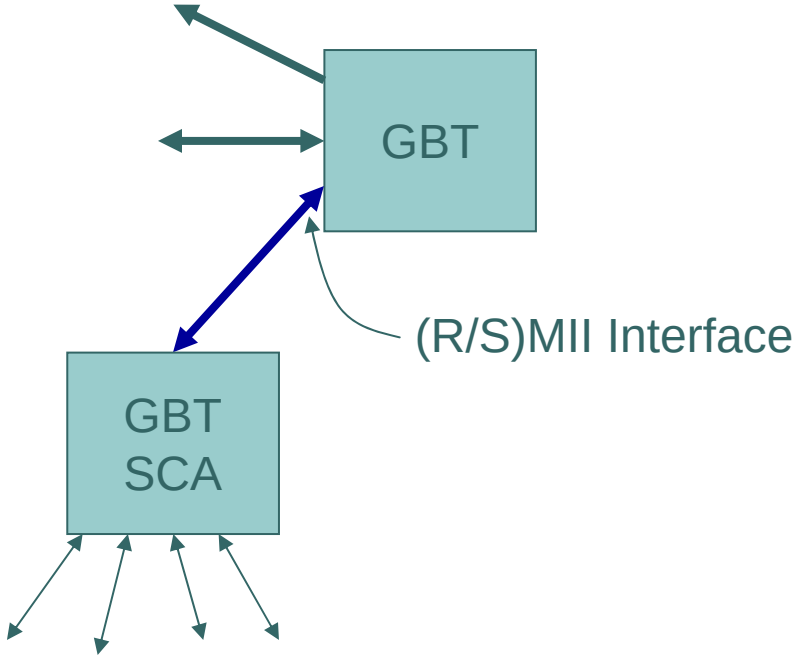


Two Chips Solution



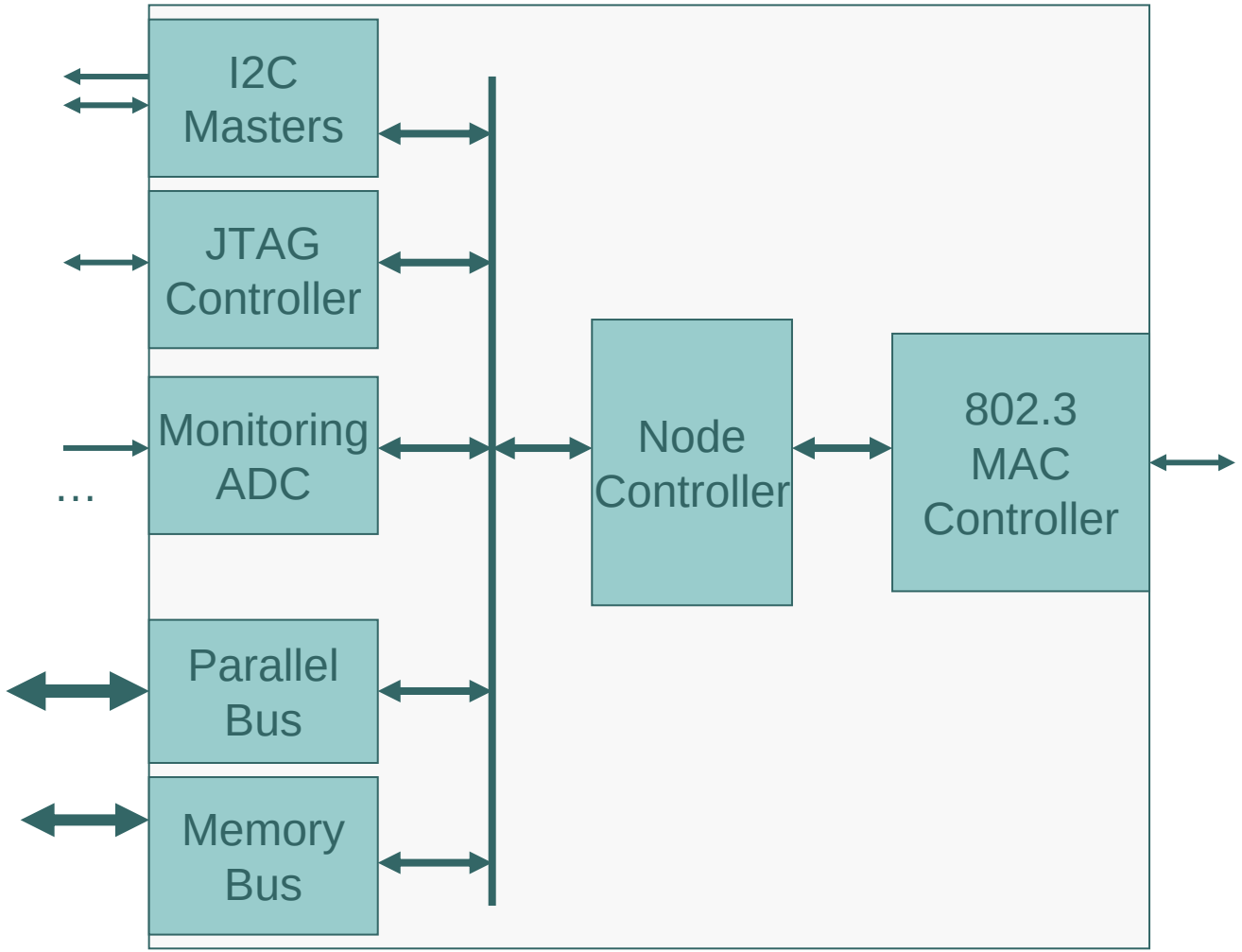
User Buses:
- I2C
- Single-wire
- Parallel bus
- JTAG
- Memory
- Monitoring 12b ADC

802.3-TX Interface Detail



- Protocol between GBT and SCA same as between MAC and PHY
  - Several versions exists (only pin count changes)
    - MII, RMII, SMII,…
- GBT looks like the "PHY" to the slow control system
  - It carries the Ethernet protocol across

GBT-SCA


I2C
Masters
JTAG
Controller
Monitoring
ADC
...
Parallel
Bus
Memory
Bus
Node
Controller
802.3
MAC
Controller

User-side buses

- 16 x I2C master with extended addressing capability
- Simple memory bus:
  - Non-multiplexed, 16 address, 8 data, RW
- 4 x Parallel ports: 8 bit wide, programmable bi-directional
- 1 x JTAG: master
- 1 x Single wire protocol (as in Dallas serial chips)
- 12/14 bit Double Ramp ADC used for local monitoring with 8 muxed inputs
- On chip Thermal Sensor readable from ADC

User side ports

- Each bus adapter is seen under the same philosophy of a "port"
- Slow control system sends "commands" to ports
- Buffering is foreseen for one command per port
- Ports acknowledge operation by replying with an ACK
- Same model applied successfully to CMS tracker and Ecal slow control system (more than 5,000 chips in operation)

Why 100 Mb Ethernet?

- Well documented and extremely popular standard
- Easy to connect to PC (requires PHY interface only)
  - GBT to PC
  - GBT-SCA to PC
- Easy protocol implementation
  - GBT will transparently carry the 802.3 protocol
- Development of GBT and GBT-SCA can go on in parallel with a minimum of interference
- Almost 'all-digital' chip for the GBT-SCA

Progress

- Overall architecture:
  - P2P vs. Mixed P2P+Passive Optical Distribution are being evaluated
- Transceiver blocks are defined to sufficient level to allow design to start for:
  - Clock and Data Recovery Circuit
  - TransImpedance Amplifier
  - Laser Driver
  - Full Coded
- First version of FEC chip was presented at LECC 2006

Plans

- Phased approach is very likely
- By end of 2007
  - Converge on Final System Architecture and technology choice
  - Full front end Serializer demonstrator submitted in 130nm
  - Modeling of complete Slow Control Chip well advanced