ATLAS Pixel Architecture

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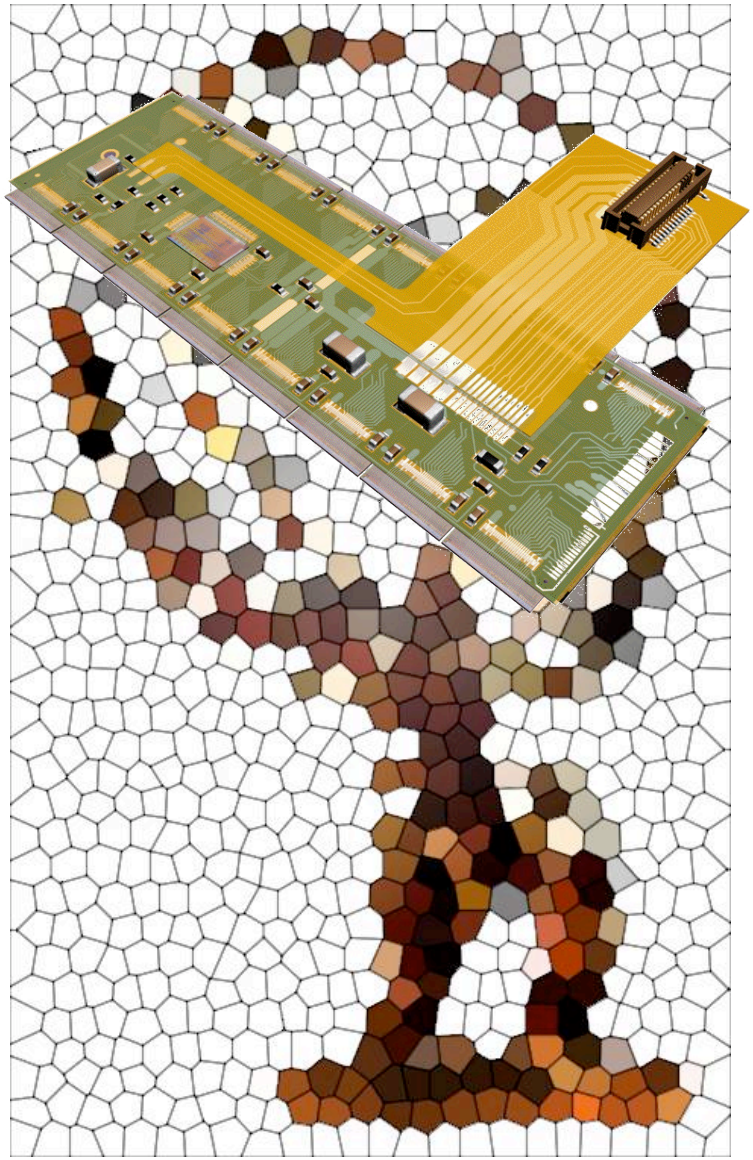


Talk Content

Today Pixel architecture is presented. The analysis of today pixel design together with new technological trends give indications on what are the weak and strong points for selecting new system architectures.

Some of these points are discussed and analysed in this talk.

Workshop page:

http://aces.web.cern.ch/aces/

Preamble

- *Most of the considerations that will follow are made for B-layer architecture where conditions are more challenging.*
- *Analysis starts from today design and try to extrapolate the parameters to the SLHC case study.*
- *R/O Architecture & Layout optimization need simulation. This work is starting now. Results reported in here are extrapolation from old simulations made to optimize the present design scaled for the increase in event rate.*
- *The machine scenario considered in here is the 50ns bunch crossing, that is today preferred by ATLAS and CMS and also from machine people.*

SLHC - Parameters for Pixels

SLHC opt.1 looks (today) the most probable scenario: best for both machine design (lower beam-pipe electro-cloud heating) and experiment (no machine elements inside ATLAS/CMS detectors).

Essential parameters for Pixel FE and Architecture design are:

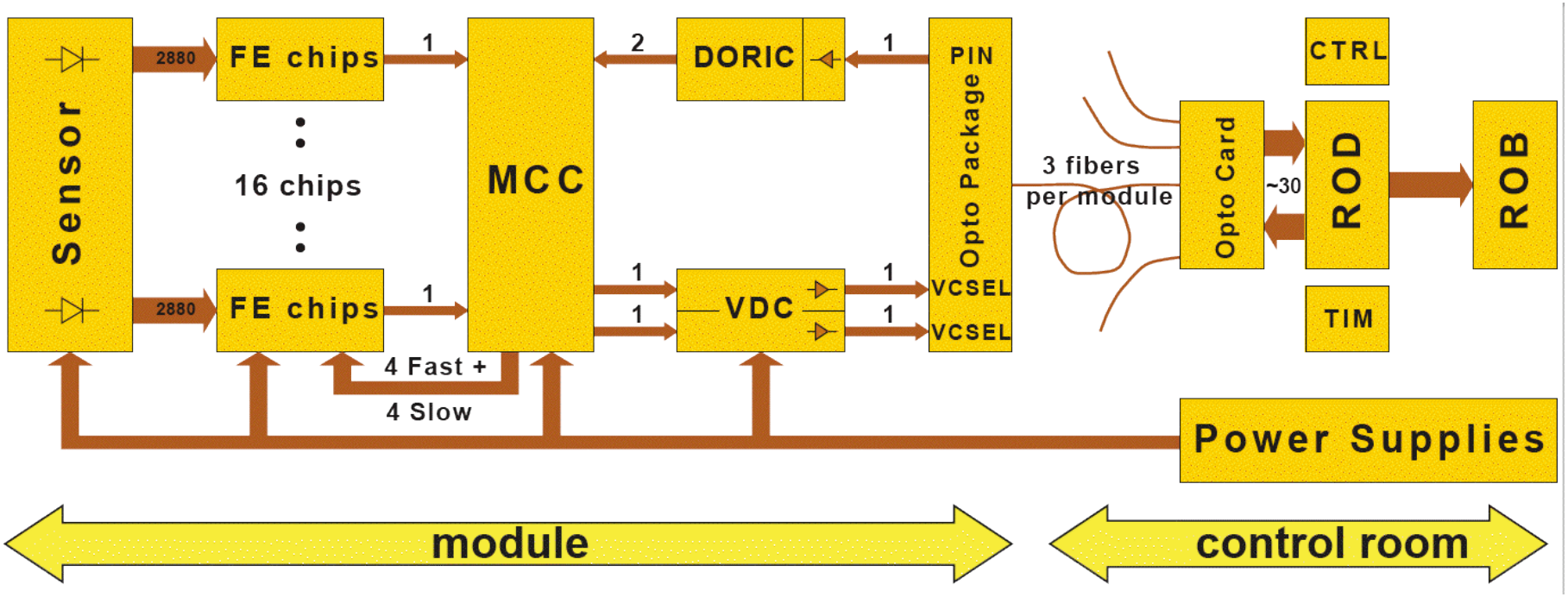
- *Bunch spacing → time resolution, time-walk, preamplifier speed, power consumption of analog front-end.*
- *Peak events per crossing → Buffer sizes and bandwidth inside and outside chips.*
- *Ionization damage, expressed here in kGy deposited in Si, and displacement damage, expressed in ATLAS in 1 MeV n equivalent (NIEL) fluences → Very high rad-hard devices (and also SEU immunity)*

Parameter	Sym. [Unit]	LHC	SLHC op.1	SLHC op.2
Bunch spacing	Δt_{sep} [ns]	25	50	25
Peak events per crossing	-	24	403	294
Peak luminosity	L [10^{34} $cm^{-2}s^{-1}$]	1	10.7	15.4
Effective luminosity ($T_{turnaround}$=5h)	L_{eff} [10^{34} $cm^{-2}s^{-1}$]	0.5	3.5	3.6
Design radiation dose (B-layer@3Years, Layer1@10Years)	[kGy]	500	3500	3600
Design fluence for NIEL effects (B-layer@3Years, Layer1@10Years)	[1 MeV n/cm^2]	$1x10^{15}$	$7x10^{15}$	$7x10^{15}$
Luminous region length	σl [cm]	4.5	5.3	3.7

Pixel Global Architecture - Today

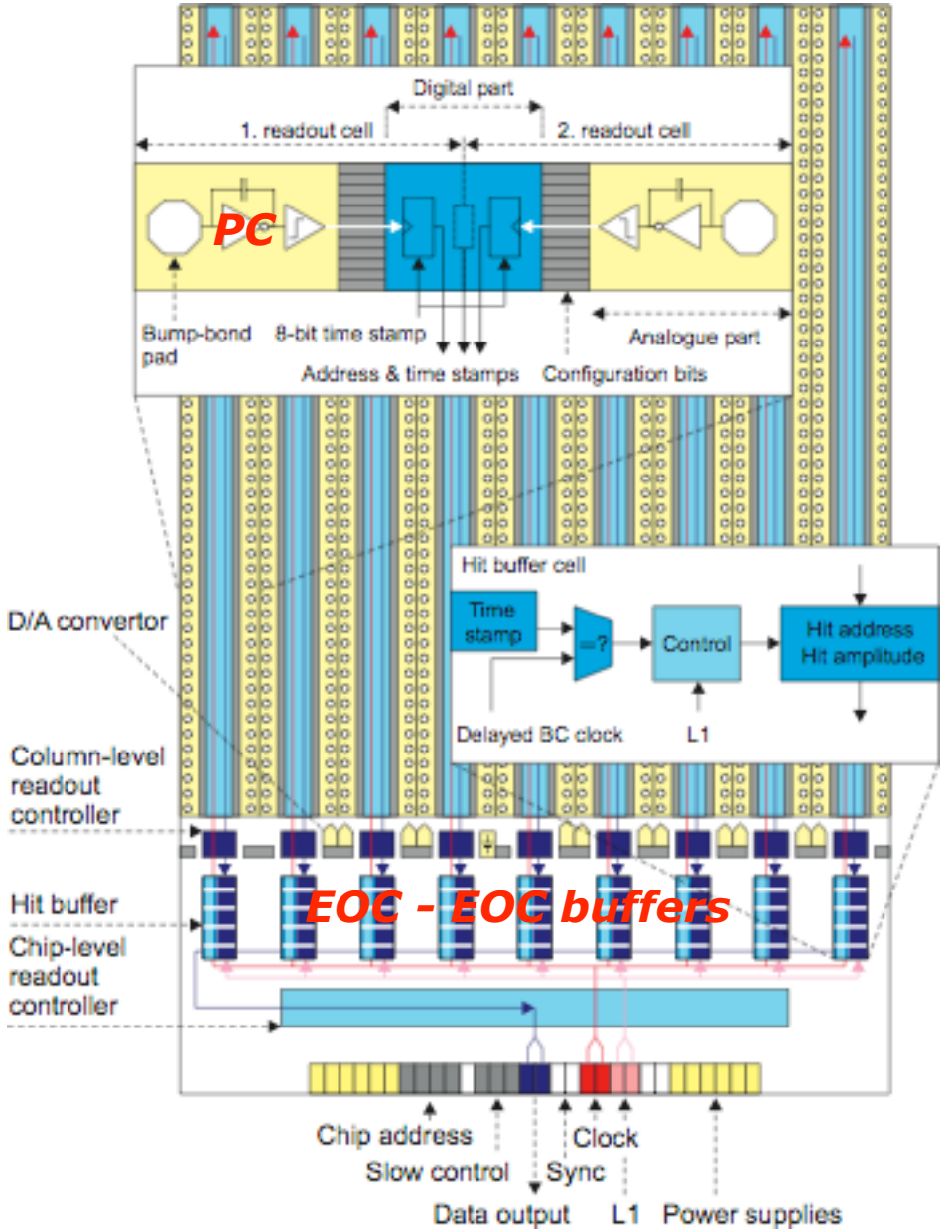
Pixel Global architecture:

- *R/O in 3 steps: FE, MCC, ROD*
- *Data Push: data always flows without backpressure busy*
- *Serial Links: LVDS between FE-MCC / LVDS+OPTO between MCC-ROD*
- *Link topology: star-topology.*
- *Buffers: Pixel Cell, FE end-of-column, MCC input FIFOS, ROD input formatter*



FE R/O Architecture - Today

- *R/O FE Architecture is based on dual column readout. Hits in the Pixel Cell (PC) are associated with 8-bit time stamp distributed along the column by an 8-bit bus.*
- *All hits are transferred to large content-addressable memories at below each column-pair. There are 64 end-of-column (EOC) buffers for 320 pixels. PC R/O uses sparse scan with token-passing scheme.*
- *Hits in the EOC buffers are associated by their time stamp with L1 triggers.*
- *Hits associated with L1 are serialized, ordered by (only) column pair and transmitted out of the chip.*



FE Architecture - Towards SLHC

Extrapolation of current R/O architectures impacts into some bottlenecks.

End-Of-column Buffers: 64 EOB for a dual column, having to store all the hits till L1 comes (3.2µs) are already for LHC luminosity a major contribution to hit loss for the B-layer.

Column-bus bandwidth: Sparse scheme used requires high bandwidth on the bus. This conflicts with heavily loaded bus with sense amplifiers that today can transfer 20Mhit/s using significant power.

- *Both issues have to be scaled for the expected SLHC peak occupancies normalized at 25ns bunch x-ing. → x7.5. Longer columns in a bigger chip would worsen both.*
- *Furthermore, the large buffer pools at the bottom of the chip are the major contributors to dead area on chip.*

Alternative new approach is to store data in pixels until L1 trigger decision is made (essentially move part of the EOC buffers into individual pixels). This will require double-buffering to allow overlapping hit acquisition and hit readout in each pixel.

- *The storage already present (LE timestamp, TE timestamp) needs double buffering. In addition to address ROM it will need logic for BCID comparison. This circuitry could be x2.5 the present. It could be achievable in 0.13µm but will have to fight for a request of smaller pixel size.*

FE Analog Cell - Today Design

- *The amplifier is optimized for a nominal capacitive load of 400 fF and designed for negative signal expected from $n^+-on-n-bulk$* detectors.
- Special attention was put in the design of the charge amplifier to the requirement of irradiated sensors, where the leakage current (50 nA) is two order of magnitude bigger than the signal (5000 *e*), which is reduced by carrier trapping inside the silicon.
- The preamplifier has roughly 5 *fF* DC feedback design, 15*ns* risetime.
- *An important property of the feedback circuit is that the time to return to baseline is nearly linear with released charge. From the comparator a pulse width proportional to the input charge is obtained (Time-over-Threshold -ToT). Feedback current is 4nA* for 1μs return to baseline and 20*ke* input charge. Measuring the difference between Leading (LE) and Trailing (TE) Edges in CK units gives the charge. ToT is also a source of dead time, being the input blind until discriminator output returns to 0.
- *The total analog FE (preamp. second stage, and discriminator) has a bias current of about 24μA per pixel for the default DAC settings of 64.*

Pixel Cell - SLHC (Critical) Issues

Charge collection - critical issue.

- *Difficult design a system running a threshold below 3ke.*
- *For B-layer there is the possibility to use not-fully depleted or thin-detector (MPI R&D) that will give a substantially low collected charge.*
- *3D-sensors (ATLAS R&D) can provide an higher than 2D charge: 7.1ke at $8.6x10^{15}$ (ref. C.DaVià / Liverpool Dec'07).*

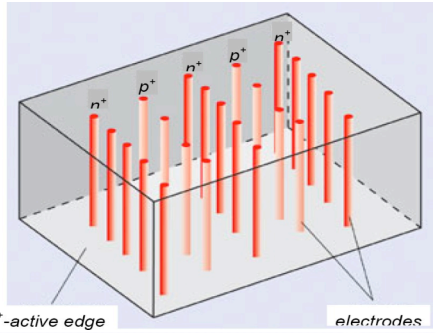
Noise - critical issue - depends on sensor leakage current (increasing with dose) and input capacitance (higher on not-fully depleted/thin sensors or 3D sensors)

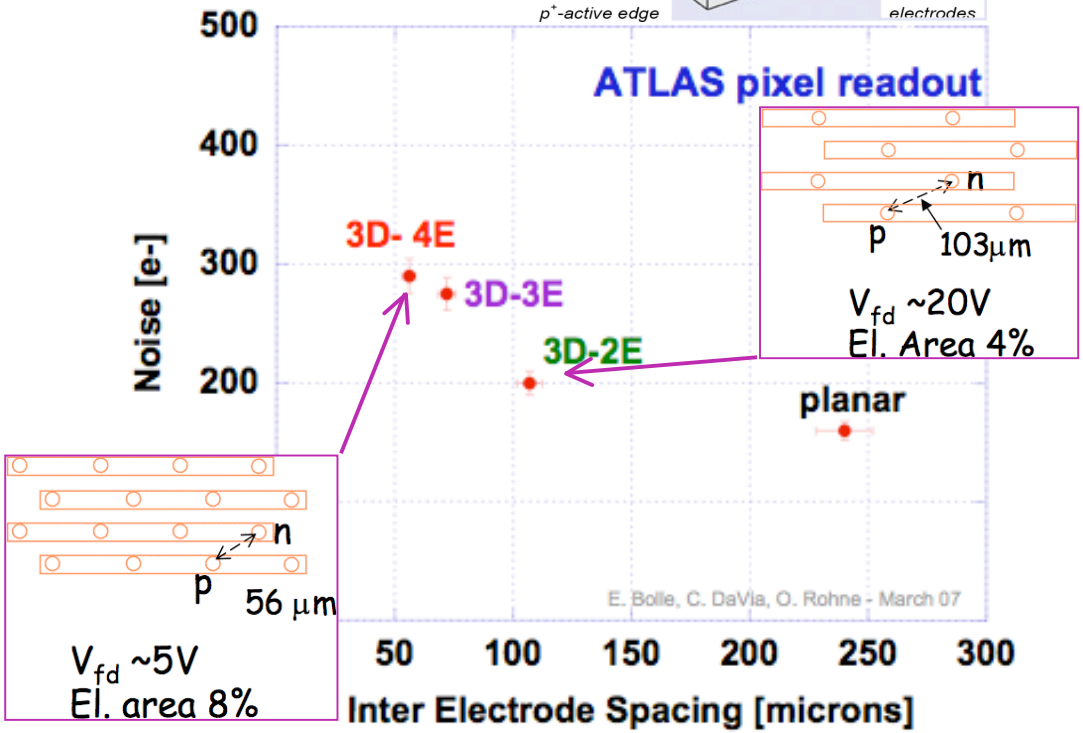
- *In the plot preliminary unpublished results of 3D-sensor noise measures made with standard ATLAS FEs.*

Time walk - Critical for a target 25ns B-layer design. More relaxed with 50ns.

Power consumption - Will increase with smaller pixels. Also more critical for digital part (leaking transistors and larger logic)

3D sensors and planar (2D) noise measurements made with ATLAS R/O FE chip.





Ref.: Preliminary measurements - ATLAS 3D R&D

Full-3D active edge sensors fabricated at Stanford by J. Hasi (Manchester), C. Kenney (MBC)
Measurements performed by E. Bolle, O. Rohne (Oslo University)
Boards from Bonn University
Setup and discussions C. DaVia (Manchester), M. Garcia-Sciveres, K. Einsweiler (LBL)

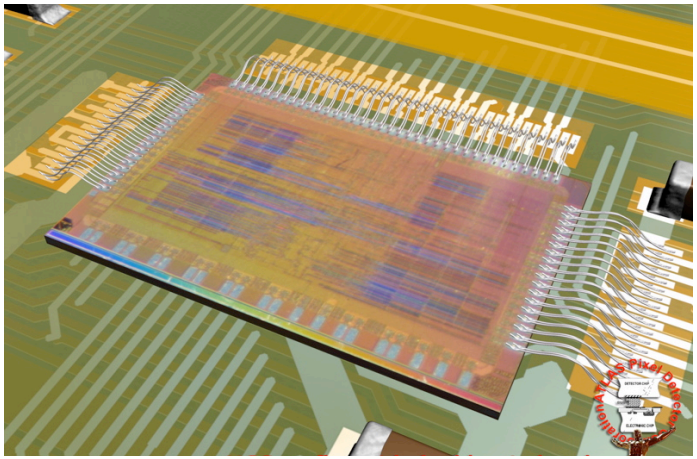
Module Control Chip (MCC) - Today

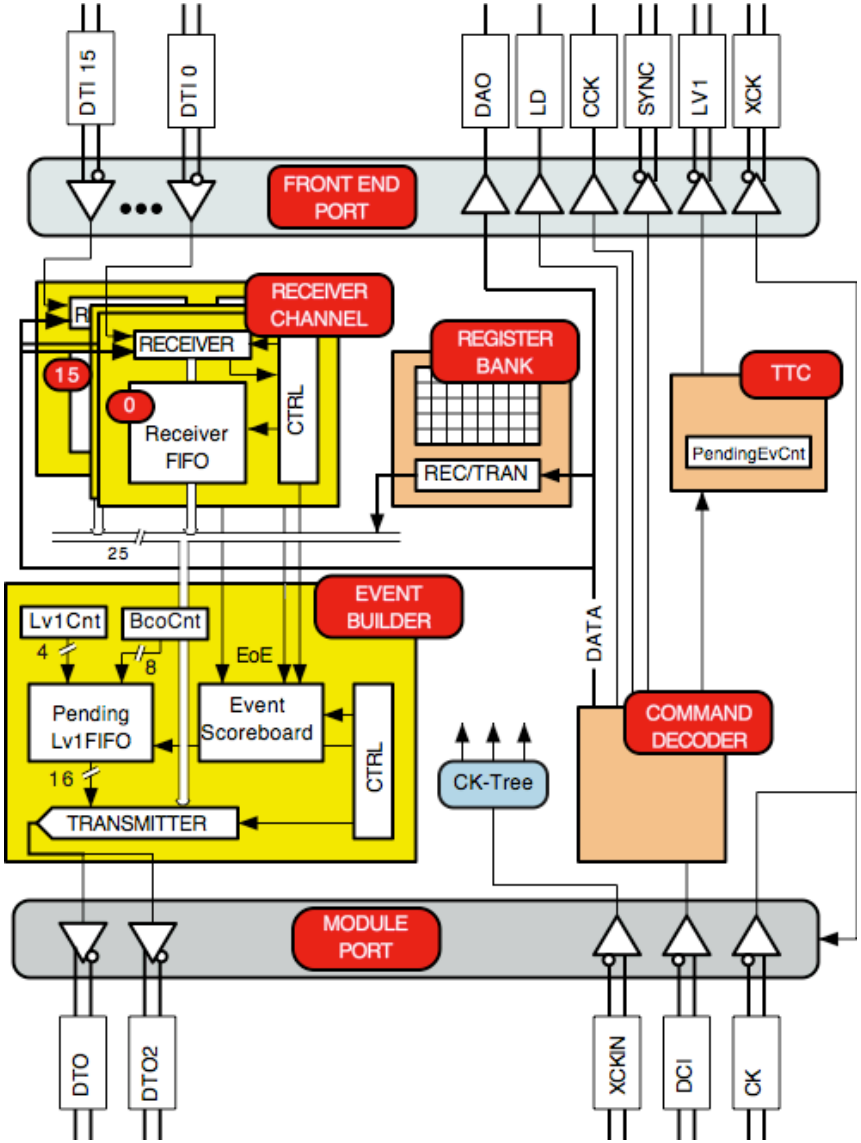
Functions: Event R/O, Trigger, Timing & Control (TTC), R/W module configuration.

Event R/O: 16 serial LVDS links from FEs (DTI0-15). 128-words at input from each FE to store hits (ReceiverFIFOs). Track of 16-L1 events (PendingLv1FIFO). Status of completely received events (16x16-bit EventScoreboard). Even is transmitted to the out-link(s) when corresponding Scoreboard row is complete.

Configuration: 3 single-bit bus lines to configure FEs. Data&Command (DCI), Load (LD) to separate command from data, 5MHz Validation Clock (CCK). Data are R/O using DTI lines.

TTC: L1 trigger to FE (LV1), Reset & Synchronization (SYNC), 40 MHz clock to FEs (XCK)





Ref.: R. Beccherle, NIMA 492(2002)117-133

Architecture Simulation

- *The current R/O architecture was simulated using SimPix framework in 2002-03. SimPix is a time driven simulator (P.Morettini et al.) that uses Geant3 input physics events and has "architecture plug-ins" for the hardware to simulate/emulate: C++, Behavioural, Verilog or hardware MCC (connected by interface module or pattern generator/logic state analyzer).*
- *From 2003 SimPix results extrapolated to SLHC:*

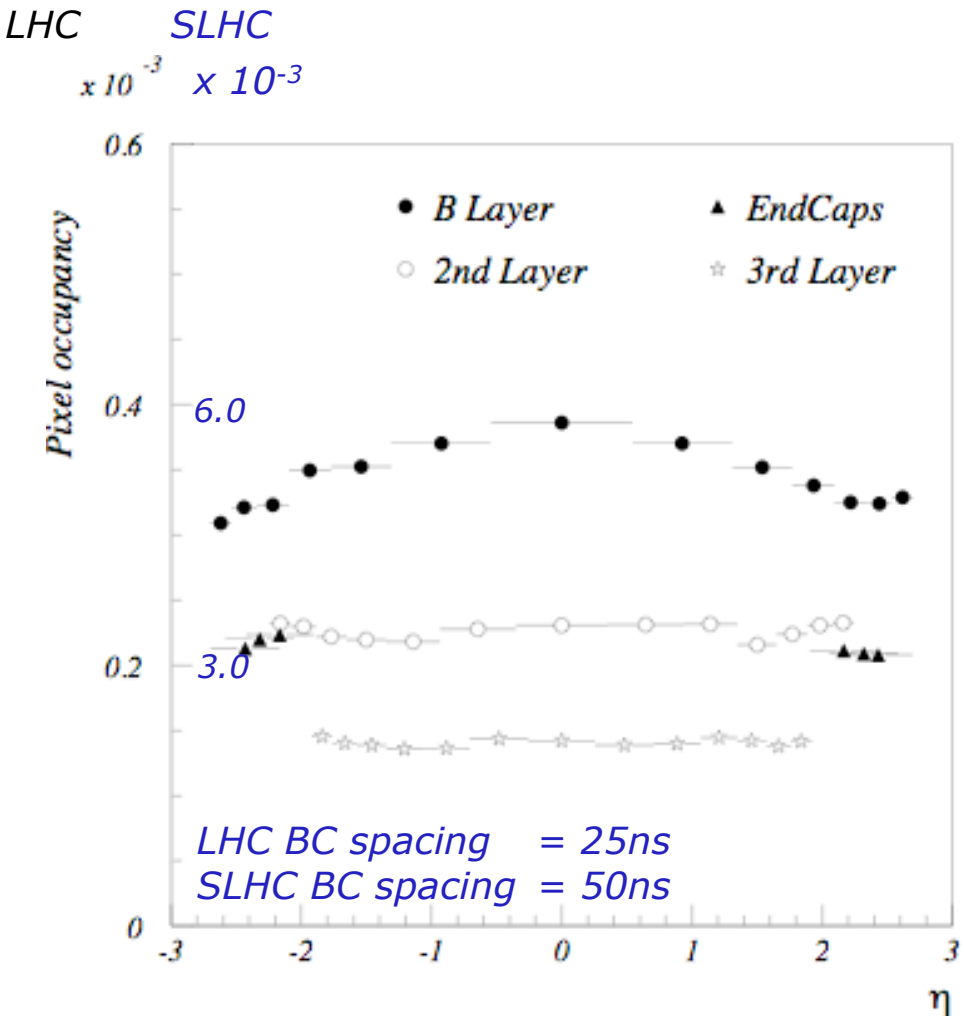
LHC: Maximum pixel occupancy per beam crossing (BC) is 0.4×10^{-3} at LHC for B-layer (BL) and 100kHz L1.

SLHC: (50ns BC): naively for same geometry of B-layer, by scaling x15 (peak luminosity ratios):

- *Single Pixel occupancy = 6×10^{-3} (or 3x10-3 scaled to 25ns BC)*
- *Module hits per BC = 345*

New R/O architecture simulation is ongoing…

Pixel Occupancy at LHC/SLHC per BC



FE & MCC Out Links

From today Pixel architecture (see plots) we can extrapolate link parameters for SLHC.

- *FE to MCC links for 18x160 pixels of 50x400μm^2 (or for same sensitive area) the mean bandwidth used is 50 Mb/s.*
  To avoid too large FE buffers at least x2 is required as available bandwidth.

- *MCC to ROD would use 500 Mb/s bandwidth*

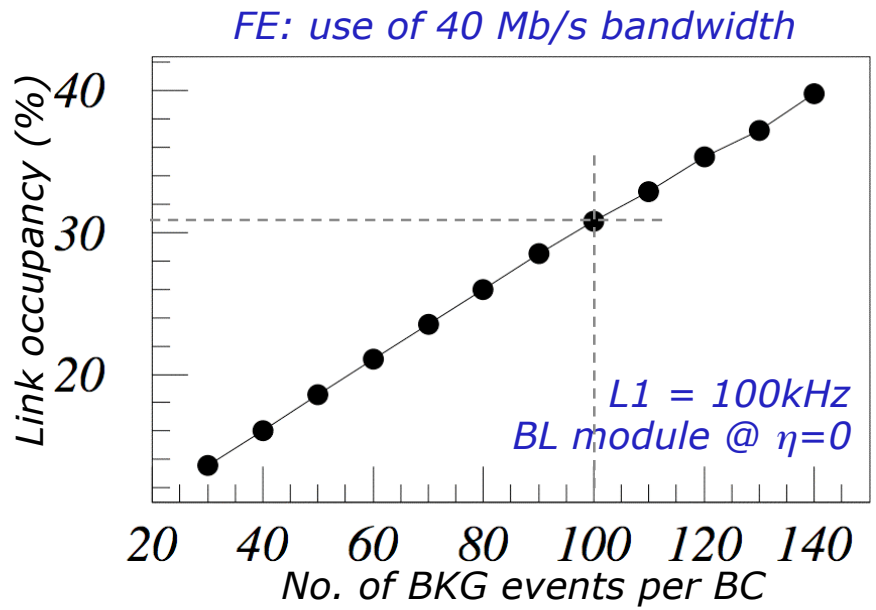
Note: factors from LHC to SLHC must be scaled by BC occupancy and L1 rate (assumed 100kHz) i.e. x15.

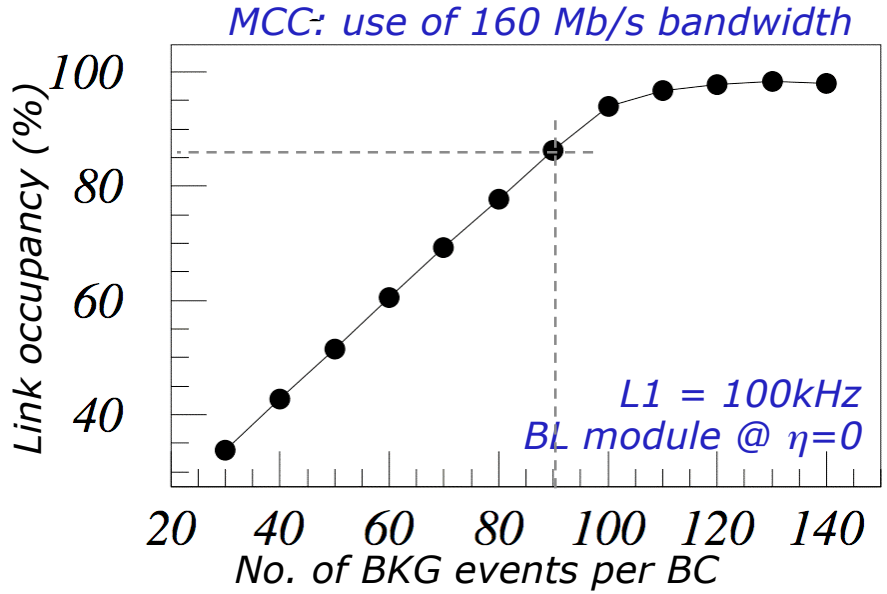
In conclusion for a SLHC module with 16 FE and same size as today the naïve analysis gives:

- FE to MCC → 100 (160) Mb/s
- MCC to ROD → 1.0 (1.28) Gb/s

Note:

80 Mb/s can be made using a 40 MHz clock without the need of analog circuitry for clock multipliers (PLL/DLL).

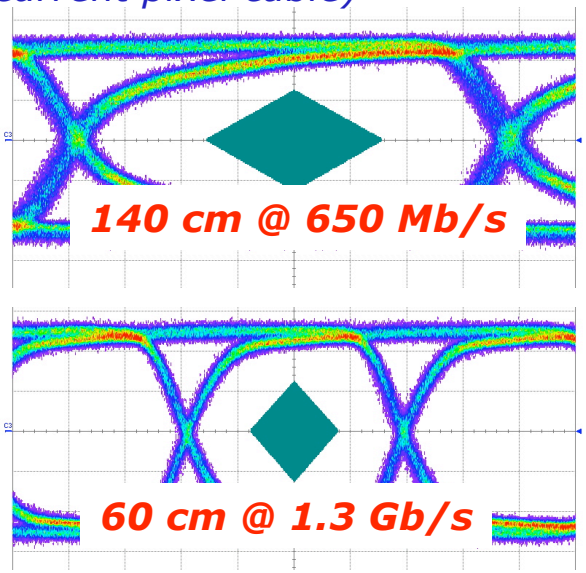




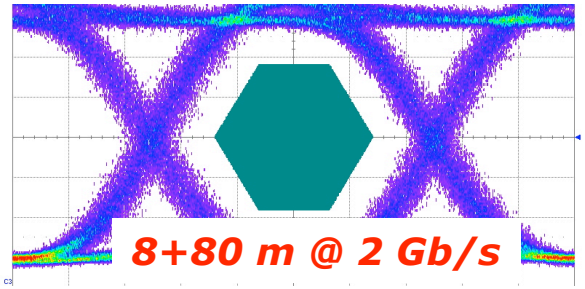
How Extract Signal from Module

- *Today: opto-link separated from module by ~1m and mount PIN/VCSEL array on patch panel*
  SLHC: adopt same solution → much reduced radiation level compared to B-layer:
  - Si PIN : 114 Mrad for 24 GeV protons
  - GaAs VCSEL : 70 Mrad fo 24 GeV protons
- *Preliminary test made from Ohio State Univ. and Oklahoma University:*
  - Micro TP are OK up to 1 Gb/s
  - SIMM/GRIN fiber can transmit up to 2 Gb/s
  - PIN responsivity decrease by 65% at SLHC dosage
  - VCSEL (from Optowell) survive SLHC dose
- *VCSEL Issue. Requirements of 2.5 V to operate at 10mA. Standard 0.13µm technology use 1.2V of PS. Implementation of opto-driver in the MCC would require different technology.*
- *Architecture for SLHC:*
  - For B-layer we probably have to combine Twisted Pairs with Fibers.
  - For outer layers we may consider to drive opto-links from module

Bandwidth of Micro Twisted Pairs
38 AWG/100 µm, 2 turns/cm
(current pixel cable)



Bandwidth of Fusion Spliced Fiber
8+80 m spliced SIMM/GRIN fiber



Ref. R.Kass et al., IEEE-NSS 2006

Module SLHC Alternative - MCC

Module System Architecture with "standard MCC", star-link topology and data push R/O is a solution that still work for the SLHC.

Advantages*:*

Simplify FEs → minimum FE buffer size (estate area), "low" link bandwidth, simple command decoder.

Optical link → robust and error check encoding, (some) data compression, sharing and optimization of the bandwidth.

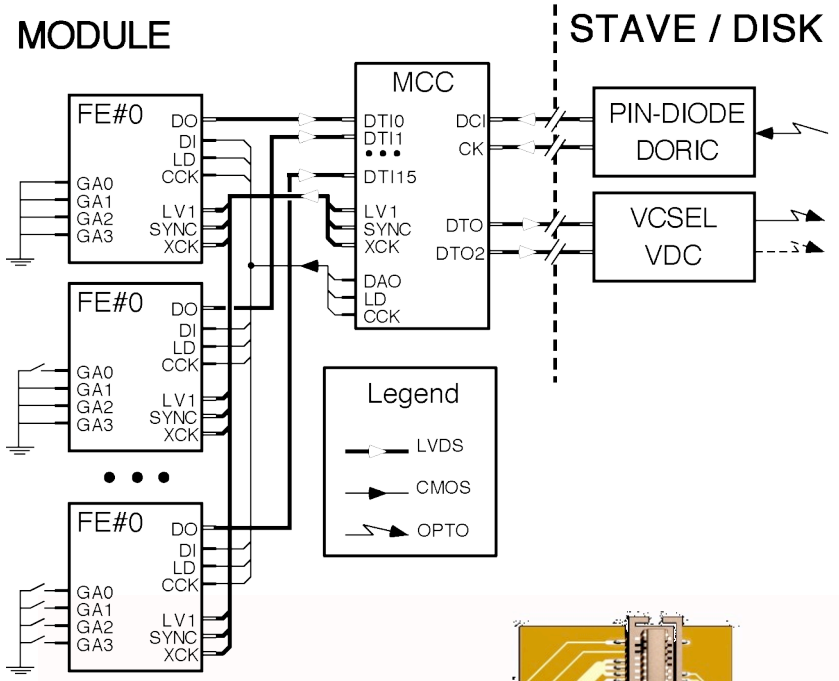
Fault tolerance → dead FE (usually) do not kill operation of the rest of the module. (MCC remains single point failure, as other upstream components)

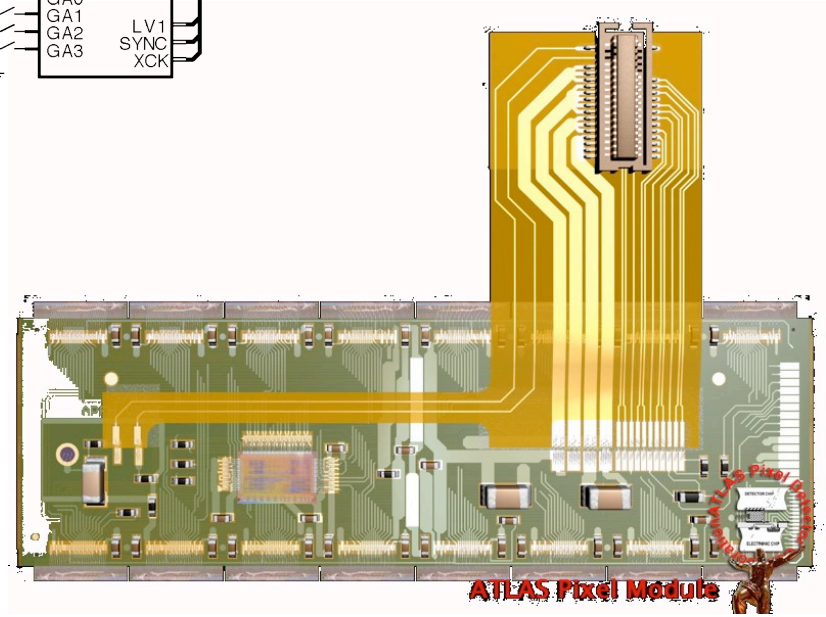
Error check → Missing events or truncated events are flagged.

L1 trigger throttling → reduce L1 backpressure to FE by dropping trigger and track missed events.

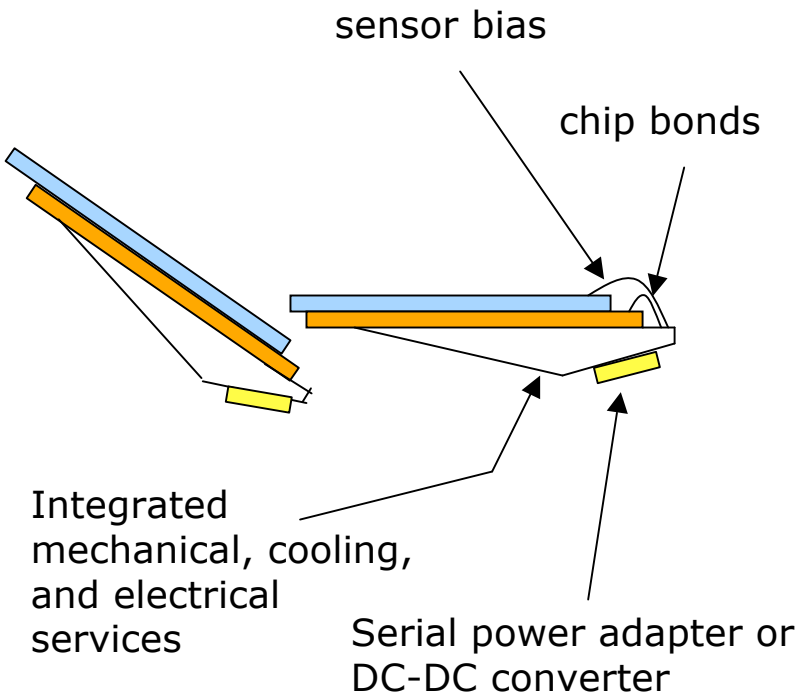
Disadvantages*:*

A FE giving to many hits (noise) can saturate and finally reduce the module hit efficiency. → More refined algorithms can be studied





Module SLHC Alternative - No MCC

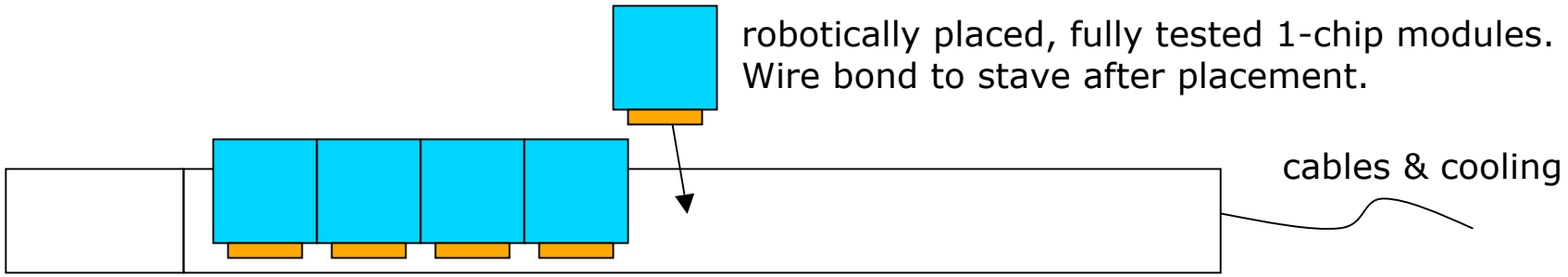


For B-layer an alternative could be a single chip module (what is the optimal size? And yield?):

- *FE with 4x area (reticle for IBM 0.13µm is 19.5 x 21.0 mm^2) and 8x pixel (200µm) requires a 320 Mb/s bandwidth.*
- *3D-sensor with active-edge technology could reduce the dead area between chips*
- *The stave (instead of the module) is the building block structure with integrated power and signal lines in addition to cooling and mechanical support.*
- *Material with this design can be reduced.*

Note:

Module test (before loading), handling and loading on stave more difficult than with standard design.

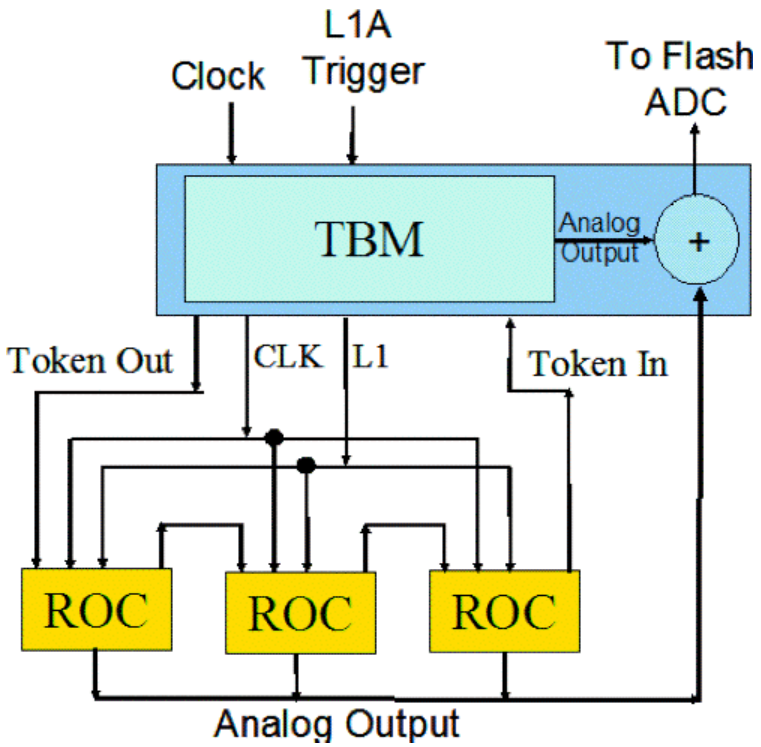


Pre-tested stave structure with integrated bus and integrated, burned-in power adapters

Ref. M.Garcia-Sciveres, Liverpool/Dec 2007

Module SLHC Alternative - ???

- *Alternative solutions could be a simple MCC (or no MCC at all) with FE connected in daisy chain. This was made by CMS.*
- *This solution reduces the interconnection on module level.*
- *Still necessary to distribute (at least) CK and L1.*
- *FEs have to transmits data to maximum bandwidth (use time sharing), more complicated FE and need of more buffer space (wait longer to start transmission).*
- *More complicated logics in the FE to deal with buffer overflow, L1 throttling, fault tolerance (skip dead FE), etc. → Bigger chip periphery (3D electronics could help?!)*



CMS uses a Token Bit Manager (TMB) chip to control the front-end Pixel chips (ROC). A token is distributed and each ROC receiving it put its hits, using analog coding, on the output bus.

Ref. E.Bartz, LECC 2005

Common Developments - Macro Blocks

- *SEU tolerant memory elements in 0.13µm technology: RAM, FIFO, FF*
- *High/medium speed transmission links (160 Mb/s, 320 Mb/s, 640 Mb/s and 1280 Mb/s) should be developed in common project.*
- *LVDS drivers optimized for speed or for power*
- *Clock multiplier to run serializers (or internal part of the chips) at higher speed (also the downlink could run at higher speed)*
- *DC-DC or Serial Powering components (see other talks this Workshop)*
- *A "super module controller" to interface several modules (in the outer pixel layers) to high-speed optical links (ref: P. Farthouat & A.Grillo - ATLAS R&D). Already at the origin of the Pixel project (ID-TDR) we planned a third level of chip in the System Architecture, called LCC (Ladder Control Chip).*

Conclusions

- *In this talk I have reviewed the ATLAS Pixel Module System Architecture. A similar architecture (FE, MCC, Opto-link) could be used for SLHC, some basic R&D are necessary.*
- *Single chip modules (maybe with 3D active-edge sensor) is an option for B-layer. Other solutions could be envisaged.*
- *System Architecture needs to be simulated to tune parameters in the FE and MCC (buffer sizes, links, busses, etc…). Work is ongoing.*
- *B-layer replacement (2012) will be a case study as intermediate solution for SLHC.*