ATLAS trigger upgrade overview

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- Requirements and constraints
- TDAQ architecture
- LVL1 issues
- TTC system
- HLT/DAQ issues
- Summary

BMBF-Forschungsschwerpunkt ATLAS Experiment

Physics on the TeV-scale at the Large Hadron Collider

FSP 101 ATLAS

Physics requirements on TDAQ

- to exploit physics potential of SLHC, need
  - → triggers for discovery physics
    - (very) high p_T objects (thresholds increased wrt LHC)
    - as inclusive as possible (e.g. also inclusive W/Z selection)
  - → triggers for precision measurements
    - high p_T objects (with similar thresholds as for LHC)
    - use more exclusive / multi-object selection to control rate
  - → monitor and calibration triggers
    - low to high p_T thresholds (will be pre-scaled)
- conditions at 10^{35} will impact trigger rates
  - → higher rate for fixed threshold and efficiency
    - trivial increase by corresponding increase in luminosity
    - further increase due to less effective isolation criteria, increase in fake rate, …
      - ➔ due to the 80 – 500 inelastic pp interactions per crossing

Example SLHC trigger menu

from hep-ph/0204087

	LHC		SLHC	
Selection	Threshold (GeV)	Rate (kHz)	Threshold (GeV)	Rate (kHz)
inclusive single muon	20	4	30	25
inclusive, isolated e/gamma	30	22	55	20†
muon pair	6	1	20	few
isolated e/gamma pair	20	5	30	5
inclusive jet	290	0.2	350	1
jet + missing ET	100+100	0.5	150+80	1-2
inclusive ET			150	<1
multi-jet triggers	various	0.4	various	low

Note that inclusive e/γ trigger dominates rate. *(†Added degradation from pile-up not included above)*

TDAQ upgrade parameter space

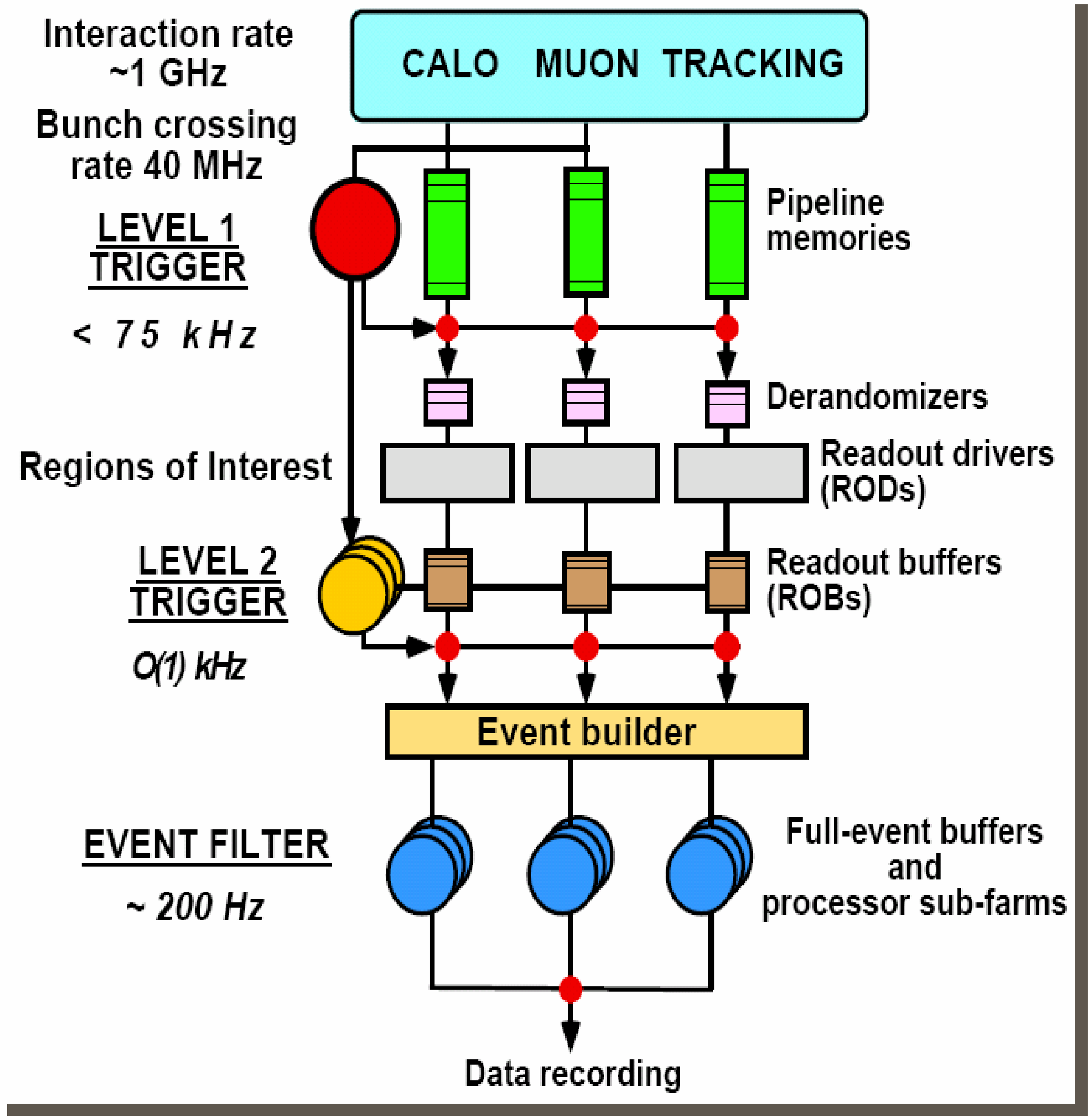
- upgrades of the trigger and DAQ system are influenced (driven) by several constraints and requirements, from
  - → physics goals
    - objects, algorithms, p_T thresholds, …
  - → machine parameters
    - bunch crossing frequency,
      # of simultaneous inelastic pp interactions, …
  - → sub-detector changes
    - number of channels, occupancy,
      signal formats for LVL1 (analog vs. digital), …
  - → technology evolution
    - availability of performing commodity items, …

Impact of luminosity upgrade

- increased radiation for on-detector trigger electronics
  - → permanent damage, single event upsets, …
- change in the bunch crossing rate ?
  - → tight coupling of LVL1 to this quantity
    - for 20/40 MHz scenario explore which parts could be kept …
- changes in the detector signals available for LVL1 ?
  - → more granular information (possibly better rejection)
    - e.g. possibility of having digitized LAr cell information

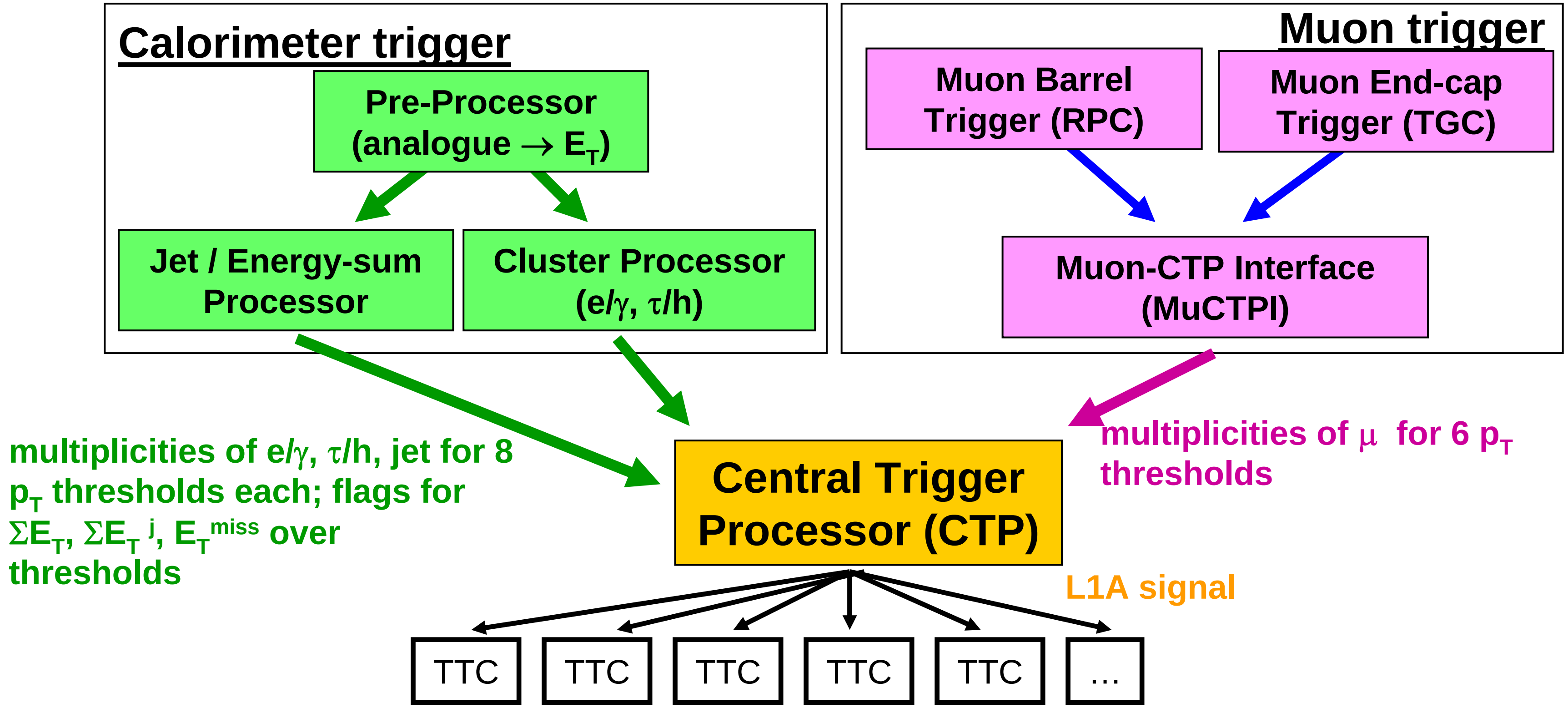
- increased number of electronic channels
  - → larger bandwidth needs
- increased occupancies, pile-up noise, …
  - → degradation of algorithm performance
    - isolation cuts, fake objects, …
  - → increased trigger rates
    - for fixed thresholds and efficiencies
  - → larger bandwidth needs

ATLAS TDAQ system architecture



- LVL1:
  - → synchronous
  - → algorithms in firmware
  - → maximum latency of 2.5 μs
- HLT:
  - → asynchronous
  - → algorithms in software
  - → processing time of
    - ~ 10 ms (LVL2)
    - ~ 1 s (EF)

LVL1 trigger overview



- input: coarse calorimeter information, muon trigger chamber signals
- central trigger processor decision based on
  - → multiplicities of (high) p_T objects and energy sums
- major challenge: data movement
  - → very high density backplanes (fanout and data sharing)

LVL1 upgrade issues

- performance degradation of present algorithms
  - → compensation by refined algorithms and/or more granular data
  - → need for detailed full simulation studies
    - technical challenge to handle 500 pile-up events
- number of p_T thresholds (sets) sufficient ?
- need for truly topological criteria to be used in LVL1 trigger decision?

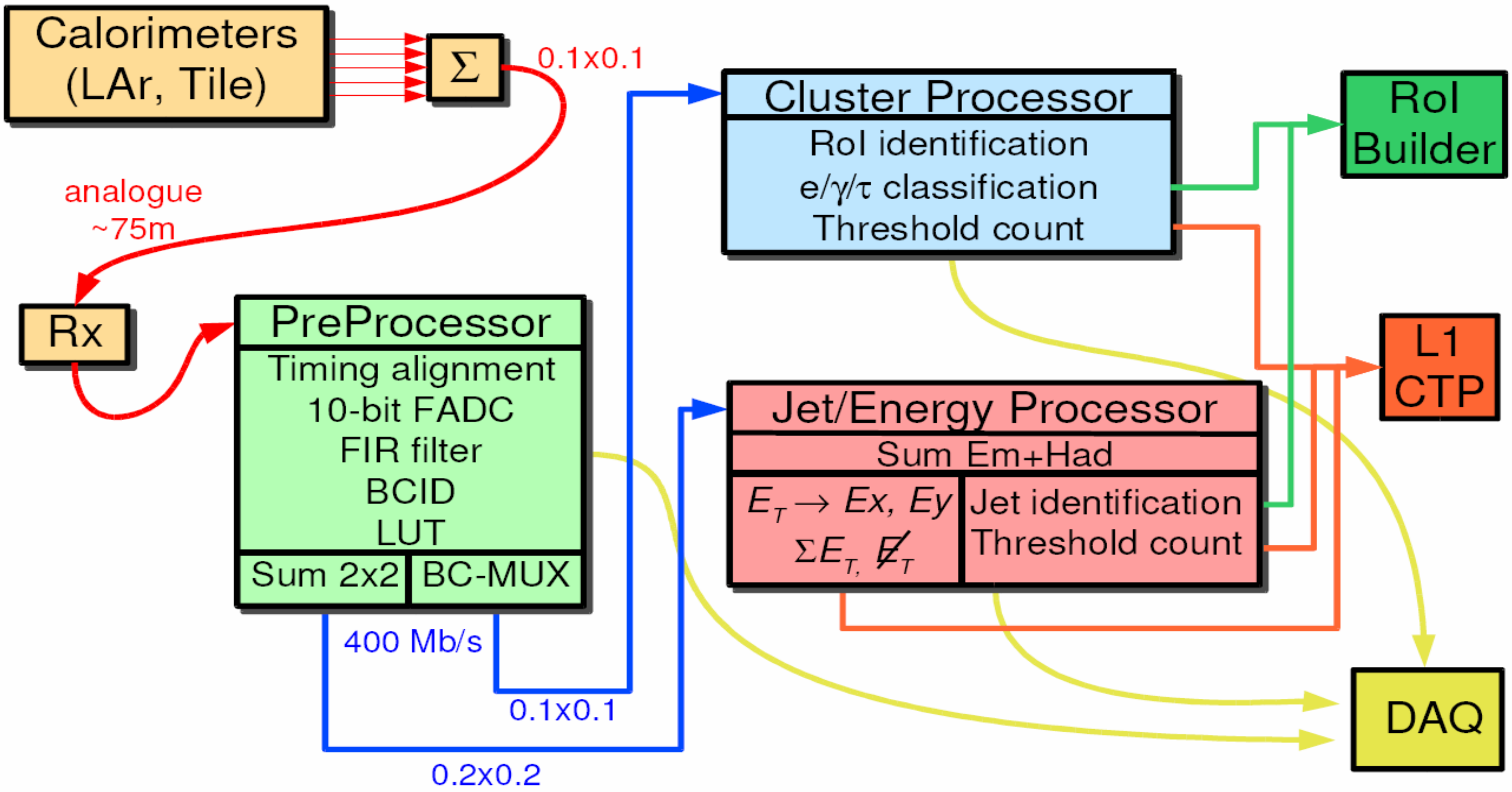
- possible change in input signals from detector front-end electronics
  - → number of channels, analog vs. digital calorimeter data, …

LVL1 upgrade issues (2)

- radiation tolerance of on-detector components
- maximum LVL1 accept rate
  - → keep present limit of maximum 100 kHz (?)
- maximum LVL1 latency
  - → determined by sub-detector with smallest depth of pipeline memories
- bunch crossing frequency
  - → seem to be less critical (at least today)

- LVL1 upgrade impacts on
  - → front-end electronics
    - if different bunch crossing frequency or LVL1 accept rate above 100 kHz
  - → HLT/DAQ: bandwidth and processing needs

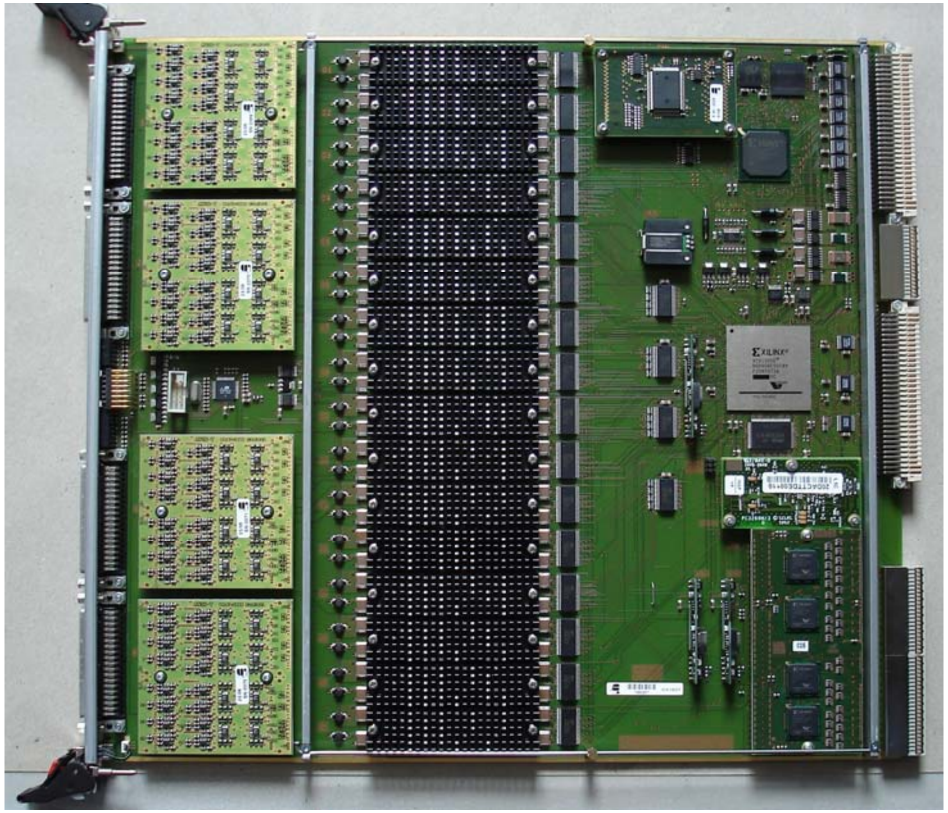
LVL1 calorimeter trigger overview

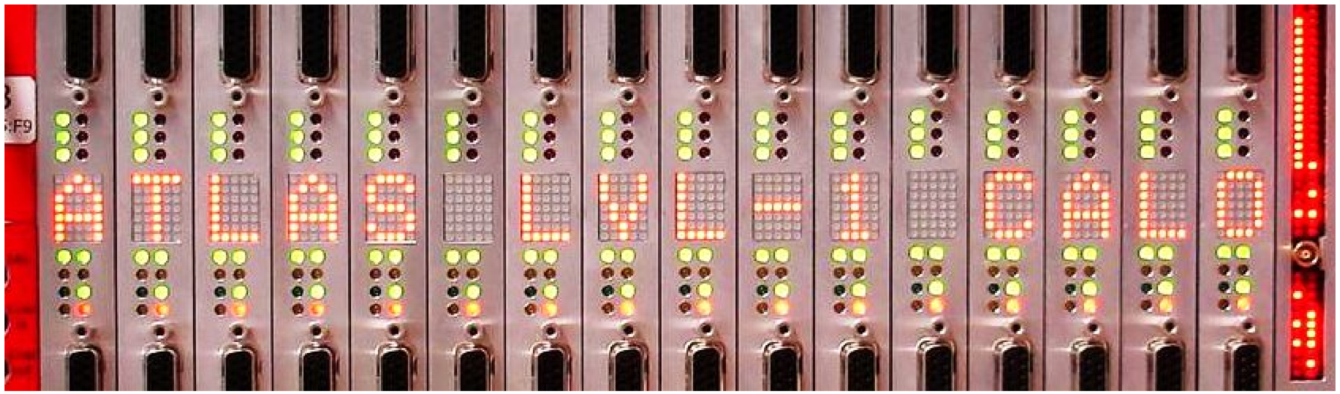


- Custom backplanes for 9U boards with ~800 pins per board
  - → preprocessor to cluster processor: 2000 Gbit/s (5000 links)

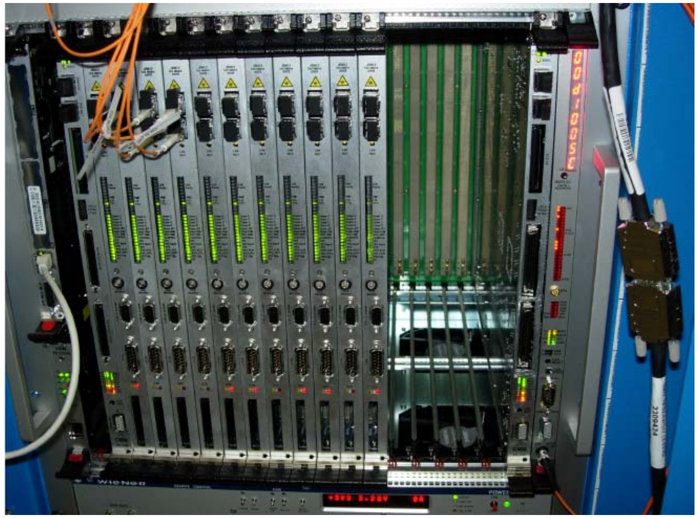
LVL1 calorimeter trigger status

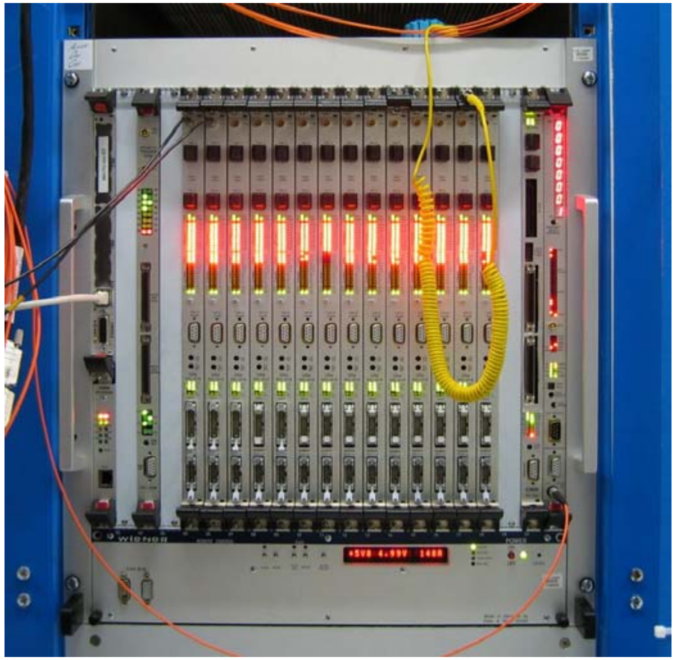
- analog signal cables
  - → in USA15
- PPM: pre-processor
  - → digitize analog signals



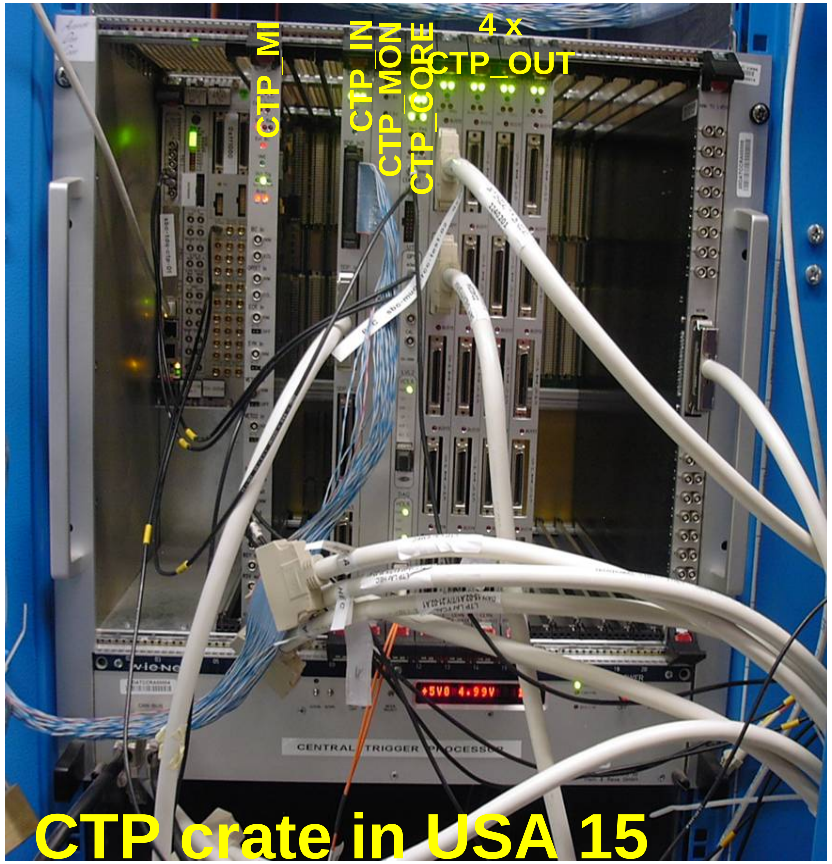


LVL1 calorimeter trigger status (2)



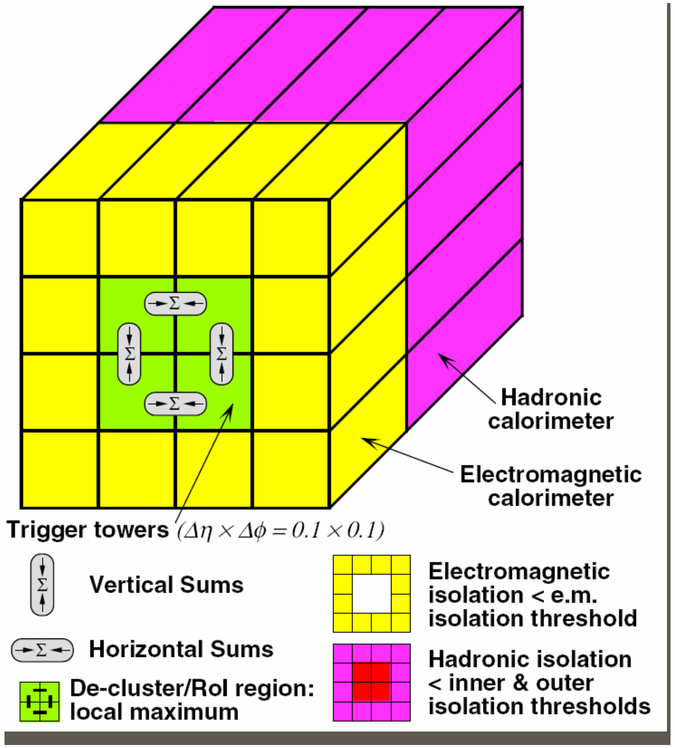


- digital processor systems
  - → em/had and jet/energy sums
- central trigger processor (CTP)



LVL1 calorimeter trigger issues

- presently using analog energy sums (trigger towers) as input
  - → refined granularity?
    - reduce occupancy, better background rejection capability?
  - → use (digitized) cell information?
  - → need to perform quantitative study
  - → need to consider issue of demands in data movement and fan-out

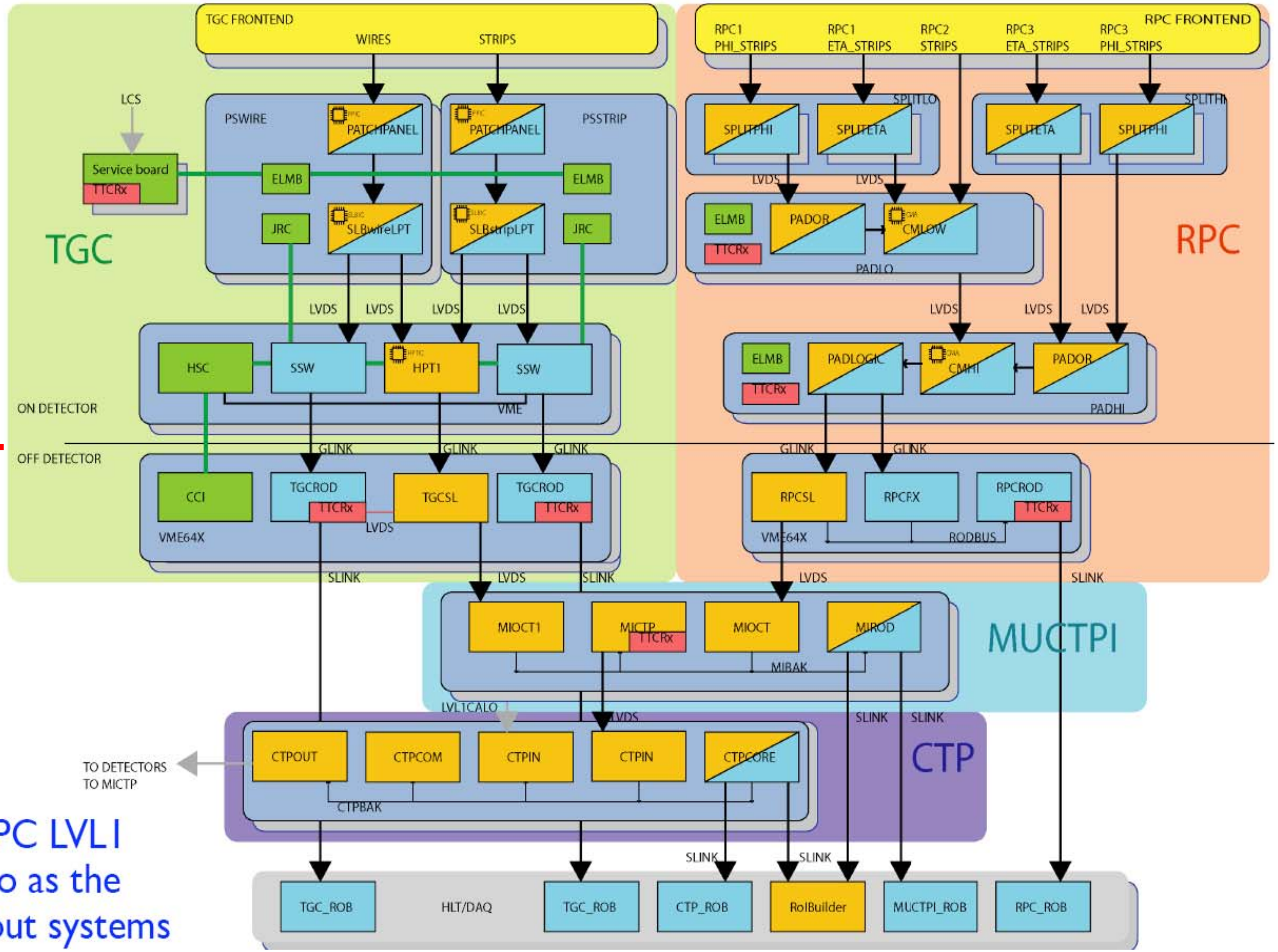


- preprocessor will only operate at 40 MHz
  - need to rebuild for shorter bunch crossing frequencies
    - ➔ same holds for processors (em/had (CP) & jets/energy sums (JEP))

LVL1 muon trigger scheme

on-detector

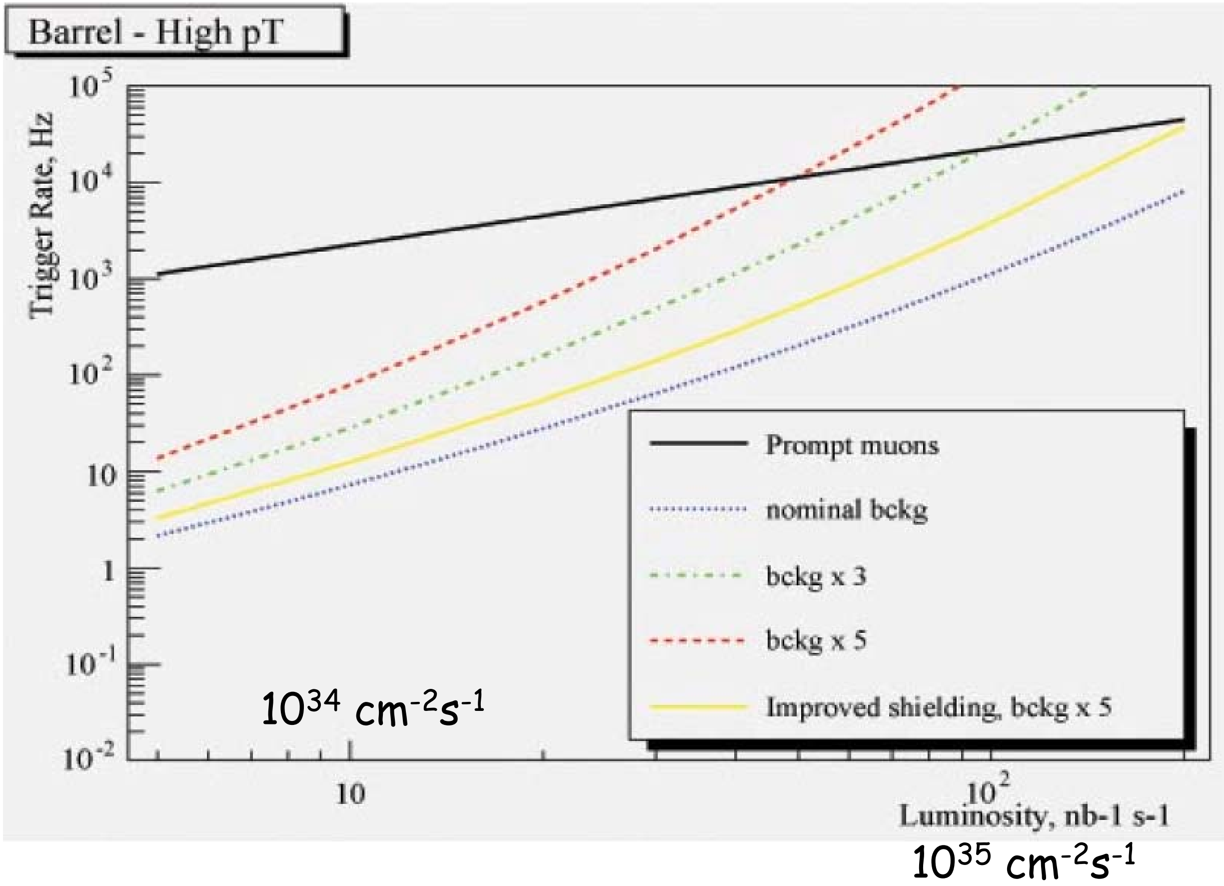
off-detector



TGC and RPC LVL1 perform also as the detector readout systems

LVL1 muon trigger issues

- dependence on performance of trigger chambers
  - see talk by G. Mikenberg
  - → understand situation with first collision data



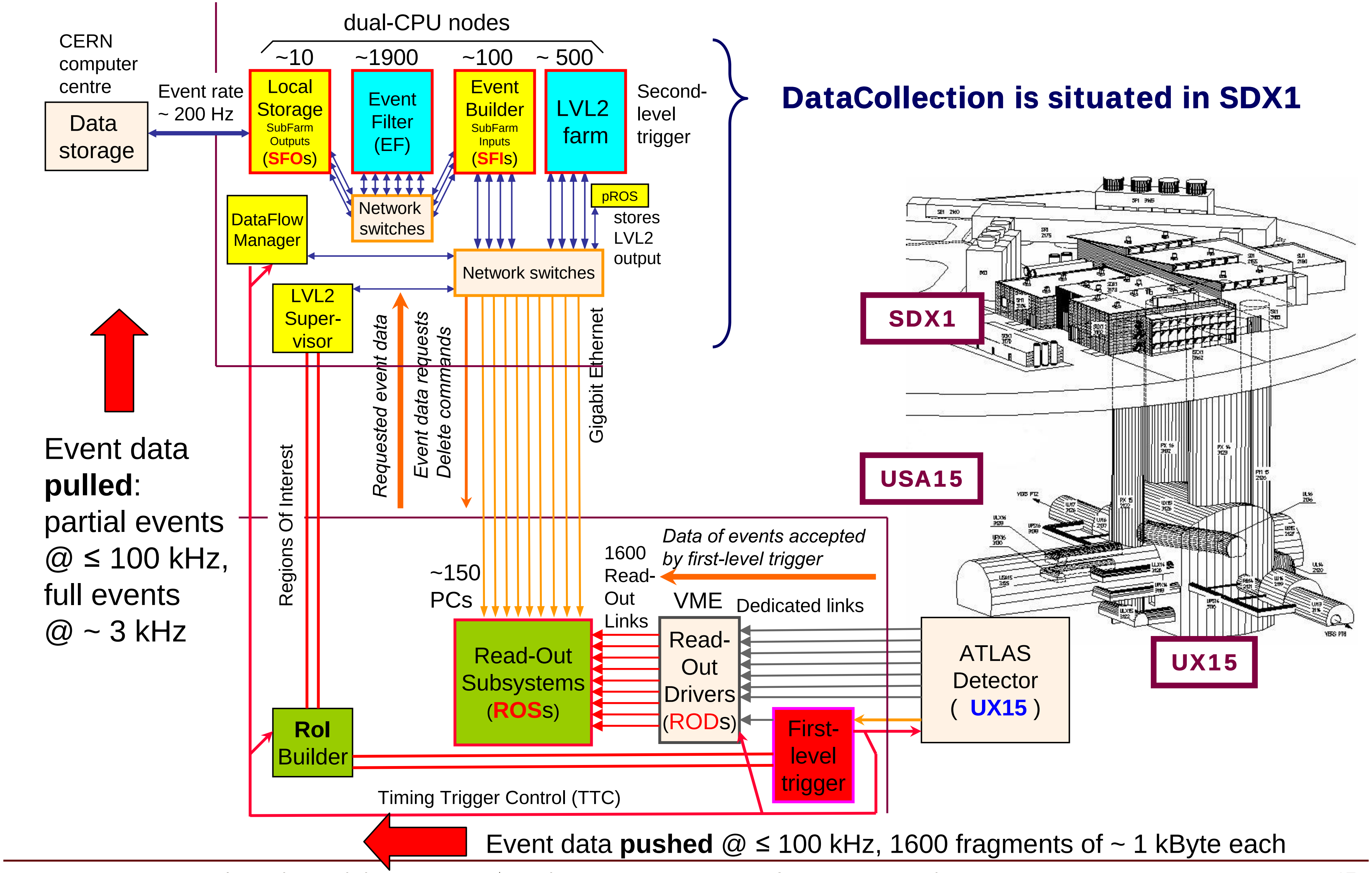
- important issues
  - → radiation tolerance
  - → background hits giving fake tracks (→ higher trigger rate)
    - via accidental coincidences
  - → restriction of pseudo-rapidity coverage – shielding improvement

TTC system

- possible improvements/extensions in functionality
  - → distribute LVL1 trigger type with LVL1 accept
    - to allow for different readout schemes ?

- today not on the agenda anymore: how to cope with change in bunch crossing frequency?
  - → generate higher frequencies locally ?
  - → modification of QPLL crystals on all FEE boards
    - maybe not sufficient enough
  - → replace by a system running at higher bunch crossing frequency
    - with very good jitter performance (peak-to-peak) to drive next generation links

HLT and DAQ deployment



DAQ: present event size

Detector	Channels	Fragment size [kB]
Pixels	$1.4*10^8$	60
SCT	$6.2*10^6$	110
TRT	$3.7*10^5$	307
LAr	$1.8*10^5$	576
Tile	10^4	48
MDT	$3.7*10^5$	154
CSC	$6.7*10^4$	256
RPC	$3.5*10^5$	12
TGC	$4.4*10^5$	6
LVL1		28

- total event size of about 1.5 MB

- custom made buffer card ROBIN

- 153 ROS systems installed (with 4 ROBIN's each)

HLT/DAQ overview and issues

- HLT and DAQ mostly using commodity components
  - → processors, network, …
  - → one custom component: readout buffer (RoBIn) to store fragments after LVL1 accept
- HLT and DAQ to first order not influenced by value of bunch crossing frequency
  - → buffers see only fraction of full event data (at full rate)
  - → processor see only fraction of events (partially at full size)
- expect further technology advances to fulfill the needs
  - → R&D effort on data links, readout buffer and algorithms
- demands on processing power depends also on occupancy and other factors
  - → compensate (partially) by increase in CPU capacity (Moore's law)

HLT/DAQ upgrade issues (cont'd)

- performance of selection algorithms will degrade
  - → in addition: if more powerful algorithms at LVL1
    - possibly less rejection capability at HLT
    - part of the fake/background signatures are gone already
- how can better (tracking?) performance of an upgraded detector be utilized in the HLT?
  - → already presently very good online selection expected
    - e.g. <50% of fake electrons in the inclusive electron trigger
- data links (FEE to DAQ/trigger)
  - → higher bandwidth needs, radiation effects
- networks
  - → influence amount of data movement to HLT processors
  - → increased demand for networking bandwidth
    - again due to higher occupancies (and channel counts)
- Readout-Subsystem (ROS)
  - → operate already at highest rates
    - further increase of (internal) bandwidth demands expected

Summary

- TDAQ system depends strongly on several external parameter (areas)
  - → upgrade (and R&D) needs to be defined iteratively
- still need for R&D on non-custom components (e.g. LVL1)
  - → using advances in FPGA's and memories
- further progress in commodity components (driven by mass markets) should allow to address some of the issues
  - → increased need for data transfer and data processing
- need to ensure to have an even more flexible system
  - → and handle its even further increased complexity
- need experience / measurements from first pp collisions
  - → validate MC rate estimates for background processes (fakes)
  - → normalize cavern background simulations (muon trigger)