


Round Table discussion

- We prepared single slides covering
 - Power
 - Control/links
 - Tracker Architectures
 - Technologies
 - Trigger/DAQ
 - Design Libraries
 - Frameworks for collaboration
 - Tests/Validation/Design Requirements

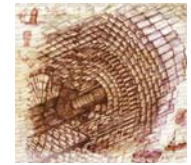
Power

- Clear candidate for a joint activity where everyone should profit
- Existing activities
 - Serial power (RAL, Bonn)
 - DC-DC
 - Switched Capacitors (LBL)
 - Air Core (CERN, BNL, Yale)
 - LDO in DSM (CERN, PSI, LBL)
- R&D proposals
 - Existing proposal for an R&D in ATLAS
- Common Working Group ” à la opto ”
 - Making available devices
 - DC-DC
 - Shunt regulators for serial power (like SMARP chip)
 - Making available blocks to be integrated in FE designs
 - Tests and Validation procedures
 - Common set of measurements to characterise a device
 - Radiation tests definition and organisation
 - Tests with existing FE systems
- Chairing
 - ATLAS CERN CMS (??)

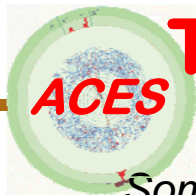
	Research and Development of Power Distribution Schemes for the ATLAS Silicon Tracker Upgrade			
	<i>ATLAS Upgrade Document No:</i>	<i>Institute Document No.</i>	<i>Created: 2/11/2006</i>	<i>Page: 1 of 2</i>
		<i>Modified: 13/03/2007</i>	<i>Rev. No.: 0.4</i>	



Control & links issues



- Common projects
 - Two models so far:
 - GBT - CERN group defines, then what follows?
 - Optical links: Democratic organisation, how to match needs of CMS/ATLAS?
 - How are goals set / who defines them/ who responsible for delivery?
 - Where do experiments provide their input / how are objectives & progress reviewed?
 - How do they contribute? What commitments are needed?
 - Specifications - When are they distributed and agreed?
 - What flexibility for long term projects?
 - Some decisions appear imminent - eg GBT technology - compatible?
 - Qualification - who is responsible, in common projects?
- Standards
 - How much are commercial standards and protocols needed in custom systems?
 - Are they compatible with need to reduce power
- Request for low power, short distance electrical links - other examples?
- Precise timing requirements for high speed links.



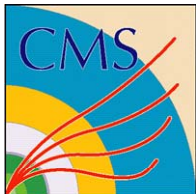
Tracker/Architecture - Common Developments

Some of the needs that are seen from a Tracker Architecture designer are (some covered already in other slides):

- **Opto Links:** use a general chip covering all the needs or design library of blocks that could be implemented depending on needs in FE/Control chips.
- **Serial Protocol:** define protocols for serial communication (Commands/Event Data) and hardware implementation blocks qualified for SEU to encode/decode/compress the info.
- **Super Module Controller:** can we have a super-module controller (High/Lower bandwidth router) common for ATLAS/CMS or common for Pixel Strips? GBT?
- **Macro Blocks:** library of macro block in 0.13 μ m qualified for SEU and radiation dose. Memory elements (FF, RAM, FIFO), LDVS/LCVS drivers optimized for different speed/power. DLL/PLL circuits to use for clock multiplier inside chips, etc...
- **Power Supply:** on-detector (DC-DC, serial [what for electrical link DC shift?], LDO regulator), off-detector PS.
- **IC design "Grid" framework.** What could be made similar to Grid offline software architecture to more tightly collaborate on projects from remote sites.

Technologies

- **IBM 25 nm CMOS -> IBM 130 nm CMOS**
 - Apparently 25 nm won't be available for SLHC.
 - Many applications: CERN, LBNL, ...
 - There are several variations of CMOS08, e.g. RF
- **90 nm or 65 nm CMOS?**
 - **No use planned as of now. Is this correct?**
- **Silicon-Germanium bipolar**
 - Potential power savings option
 - ATLAS Strips and LAr: BNL, CNM Barcelona, IN2P3, UCSC & Penn
- **AMS 50V 35 nm HV CMOS 0.35**
 - DC/DC converter: LBNL
- **AMIS I3T80**
 - DC/DC converter: CERN
- **Peregrine 25 nm SOS**
 - “Link on Chip”: SMU
- **OKI and ASI SOI**
 - 3D chips: Fermilab
- **3-D Processing – MIT Lincoln Labs (with Fermilab) & MPI**
- **Licensing issues**
 - CADENCE/Mentor



SLHC Trigger/DAQ Discussion



Trigger:

- **Algorithms degrade with occupancy = design x 20**
 - What happens to isolation in calorimeter?
 - What happens to accidentals/occupancy in muon system?
 - What could having all of the calorimeter sample information do for the trigger?
- **Level-1 Tracking Trigger**
 - Do you believe it will work?
 - Do you believe you can trigger without it?
 - Where: outer (associative memories), inner (staggered pixels), both?
- **Is it reasonable to hold L1-Accept rate at 100 kHz?**
 - Latency at 6.25 μ s?
- **How do we test all of this?**
 - Heavy Ions?

DAQ:

- **Can we combine Global L1 and Event Manager?**
- **Will the GBT work for this?**
 - Trigger synchronous data (20 MHz) (\sim 100 bit/LV1)
 - Event synchronous data packet (\sim 1 Gb/s, few thousands bits/LV1)
 - Needs to be part of GBT requirements.
- **Can we use commercial network hardware everywhere for readout?**

Joint projects:

- **Advanced networks, links, TCA backplanes**

Common Design Libraries

■ Digital

- Memories (SEU tolerant), serializers
- PLL, DLL frequency multipliers
- Slow control protocol (target low power + SEU tolerance)
- LVDS drivers : customized for minimal power / standard ?
- Codecs :

■ Analog

- Bandgap, voltage regulators, DAC, temperature monitoring
- ADCs : what power/#bits/speed ?
- For when the Universal preamp, tunable by slow control ??

■ Consensus to carefully minimize power

- Is it compatible with « standard » cells?

■ Based on IBM 0.13 μm . Portability to other technologies ?

■ IP documentation, responsibility, maintenance ??

- Regular workshops



Frameworks for collaboration

- ACES: Should we continue?
 - If so How Often, What topics? What fees!
- Joint Working Groups (ala opto group)
 - How to organize, chose leaders, review progress
- Joint Steering Group meetings
 - ATLAS/CMS Peer Review
- EU Projects
 - Long complicated process, how to organize, timescales
- CERN Projects
 - Peer review process for CERN projects? How do outside institutes collaborate and help in setting directions?
- LHCC
 - Peer Review process - at what stage do we involve external peer review
 - LHCC to designate a specialist review panel : involvement of experiments
- DRDC Type Framework
 - Any funding available or just peer review



Tests/validation/requirements Definition

- Clear agreed requirements defined
 - Change control procedures
- Qualification/validation process agreed and monitored by users/developers
 - Sign-off and participation by users
- Regular oversight of progress
- Long term maintenance and support.