# ECFA R&D Task Force 7: Electronics and Processing

## Request for community input to the TF7 R&D roadmap

The TF7 remit includes on-detector ('front-end') electronics (ASICs, services and integration), off-detector hardware, firmware and software ('TDAQ') and all elements required to integrate these elements into an overall detector system.

This document outlines some specific questions to stimulate input from the community, with the intention of identifying:

- Key needs for R&D in electronics and data processing, driven by proposed projects to realize future facilities in a timely fashion
- Ideas on how to better organise R&D, collaboration and production efforts in order to maximise efficiency and minimise turnaround time and costs
- R&D developments already under way, foreseen, or considered by the community

The TF7 remit covers a broad and diverse set of topics, encompassing many potential R&D developments, and the work of many groups with specialised interests and skills. *We therefore do not ask for a complete set of inputs from any individual or group.* Please provide information to whichever questions you feel relevant to your work and expertise. The Task Force will then attempt to synthesise a complete view for further consideration by the community. Please also indicate any further points or considerations that are not captured by the questions below.

Please send responses to: Questionnaire-TF7-ECFA-DetRDRMap@cern.ch by 28 Feb 2021 if possible.

## I. On-Detector ASICs

1. What are the most important new **functionalities and performance improvements** required of front-end ASICs?
2. Which **technologies** should we target for future ASIC developments, bearing in mind both cost issues and performance requirements?
3. **How many different technologies** should be targeted, taking into account the different requirements of tracking, calorimetry, timing detectors, etc?
4. What new design and **verification** approaches are required to address the complexity of larger and higher-performance devices?
5. How can more **intelligence** and data processing capacity be integrated into the front end, and how can the additional complexity be best managed?
6. How can **interconnection** density be improved? What is the scope for high levels of integration (e.g. 3D interconnect)?
7. How should the ASIC development community **organise** itself for maximum efficiency? How can expertise and IP best be shared between us?
8. How can **testing** and validation of complex ASICs be best facilitated / organised?

# II. Off-detector electronics

9. **FPGAs** continue to increase steadily in processing power / throughput, albeit using increasingly specialised architectures. How close to the front-end can such components be used in the future? What are the challenges involved?
10. Apart from FPGAs, what are the key **other COTS** components that should be investigated? Are there future applications for **custom** off detector processing components, i.e. ASICs?
11. How can very **high power** density processing elements be included in future electronics designs? What new techniques for module, board and system-level packaging may be needed? Should we be targeting new industry-standard form factors, and which ones?
12. What will be the challenges in the design and testing of **very-high-performance circuit boards** and assemblies? How should we evaluate new materials and design techniques?
13. How can very high performance (commercial or custom) **link and network** designs be best used in future readout systems? Where is the best place for data aggregation? What will be the challenges in the use of commercial networking equipment?
14. How can future very large instruments be **time-synchronised**? Can precision time-stamping replace or complement synchronous readout systems?
15. How can robust **control and monitoring** of on-detector systems be achieved in very harsh and inaccessible environments, for long periods of time?
16. What specialised or new (to the field) **software and computing techniques** are required for the control and monitoring of large and complex detector systems? How would this be affected by a move towards COTS-based / software-centric TDAQ designs?
17. What are the advantages and disadvantages of pushing **more intelligence towards the front end** (i.e. onto the detector)? What types of processing should be done on the detector? Does this need to be integrated into front-end ASICs, or in some additional layer?
18. How can very complex software and firmware developments be best **managed**? Can methodologies from industry be used effectively?
19. How can hardware, firmware and software **verification** at sub-system and global level be improved and made more effective? How can systems be most effectively maintained over the long term?
20. How should we reduce the development **overheads** of off-detector electronics, taking into account the effects of complexity, long-term maintenance, and the benefits of design re-use? How can costs be minimised?

## III. Links, powering and packaging

21. How will the **number of electronics channels, and their density**, change in future generations of detectors, and what challenges will this present to match the available link capacities?
22. What **data rate improvements** are required in data links to support new experiments, for data movement on- and off-detector? How can very-high-data-rate links be used in detectors?
23. What are the most promising routes to achieve **maximum performance** and radiation hardness, and minimum power, cost, footprint and material budget?
24. **Apart from optical link** technologies, what other ideas should be investigated (including galvanic and wireless links), and with what priority? What are the target applications for these technologies?
25. What is the required future evolution of GBT-like technologies? How can advanced signalling / protocols be used **in concert with off-detector COTS transceivers**?
26. What will be the **on-detector powering** requirements of future detectors? Where do the challenges lie?
27. Which **powering techniques** (e.g. DC-DC conversion, serial powering, unconventional techniques) are likely to be needed, and what new R&D is required?
28. What are the prospects for GaN, SiC, or **other materials or technologies for powering** of future experiments? What are the most promising techniques to achieve efficiency, low material budget and radiation hardness?
29. Are new technologies required to **cool future front-ends** (e.g micro-channel cooling)?
30. Which **interconnect and packaging** technologies (e.g. high-density wire bonding, tab bonding, flip chip, through-silicon vias, ACF, bumpless, etc) will be needed, and what new R&D is needed?
31. What will be the **use cases** for advanced interconnect technologies, tiling and stitching technologies and redistribution layers in future CMOS sensors?
32. Are new techniques / architectures required for **movement and aggregation** of data on the detector (e.g. radial data flow) and what are the relevant technologies?
33. What should the **focal points for R&D** in links, power and packaging be, and in which cases are these issues potential ‘show stoppers’?

# IV. Collaborative Issues

34. What new **training and skills** development is important and specific to the particle physics electronics community? What skills are we missing as a field?
35. How can we build and **maintain expertise** in increasingly complex device technologies, design processes, and COTS systems? What is the correct approach to specialisation / cooperation / consolidation between labs and institutes?
36. How can the community better coordinate and collaborate with **industry**? In what aspects would this be most beneficial?
37. How can the level of **design reuse** and common standards be improved, and parallel developments minimised, in the community? How can we facilitate and build confidence in this approach?
38. What **R&D efforts are underway** at your institution with relevance to this questionnaire?

# V. Technology evolution

Can you please estimate, as a function of time over the next 5 to 20 years (for instance at +5years and +10years), the *required* and *anticipated* improvements in performance in the following key technologies?

A. ASIC performance parameters: hit rate (GHz/cm2), power density (W/cm2), timing precision (ps), hit threshold (fC)
B. Interface speed of COTS network equipment (Gb/s)
C. Cost of COTS network links of 10Gb/s @ 10km, 10Gb/s @ 100km, 100Gb/s @ 100m ($)
D. Serial IO throughput per FPGA device (Tb/s)
E. Number of equivalent logic gates per FPGA
F. Radiation tolerance of relevant “mid-range” and “small” FPGA families (Mrad)
G. Cost and performance of ‘mid-range’ RAM, flash storage, and bulk storage ($/TB, GB/s/GB or TPS) – plus any other emerging storage technology
H. CPU and GPU cost-performance ratio relative to 2020
I. Cores per CPU device
J. Memory bandwidth per CPU / GPU device (GB/s)
K. Throughput of ML inference engines (or any other relevant specialised processor) relative to 2020
L. Throughput (Gb/s) per link, for on-detector and readout links
M. Power consumption (pJ/b) of link transceivers
N. Interconnects per front-end ASIC (connections per cm^2)

- In which areas do we expect a continuation of current trends, in which stagnation and in which step-changes in performance ?
- In which cases will the expected improvements result from commercial / industrial drivers, and in which cases will new developments be required through R&D within the field?
- What is your confidence level in your estimates?